The Road to better Reliability and Yield
Embedded DfM tools

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Abstract

This paper gives an overview of the different tools, needed for accomplishing optimal IC manufacturability and rapid technology learning during the successive phases of process maturity. The paper then describes two specific DfM tools that are in use within Philips Semiconductors.

Keywords: DfM, yield improvement, yield prediction, wire spreading.

1 Introduction

Manufacturability of VLSI designs is determined by both the design itself (inc. design procedure/flow) and the fabrication process. The essence of Design for Manufacturability [DfM] is in optimisation of the fit between design and technology, in which the design will be fabricated, from the angle of Profit Maximisation.
Because of down-scaling of feature size in semiconductor structures, brought about by following the path of 'Moore's law' into the deep submicron region, sensitivity of product manufacturing to variations in design and process parameters has risen dramatically. Furthermore shortened product life cycles and the accelerated rate of introduction of new products and processes have changed the interface between Design, Test and Manufacturing. Only a close co-operation between design, test and manufacturing will lead to rapid learning in new technologies, which is essential for the profitable production of future integrated circuits. [Ref. 1]
The overall DfM and Rapid Technology Learning strategy at Philips Semiconductors, MOS4YOU, is depicted in fig. 1. The feedback paths from the DfM to design, process and test technologies are the main outcomes of this strategy. In many cases the endresults will be tools, embedded in the design or test flow. Domains like DfT (Design-for-Testability), DfA (Design-for-Analysability), DOT (Defect-Oriented-Testing), MfD (Manufacturing-for-Designability) are included in the strategy.

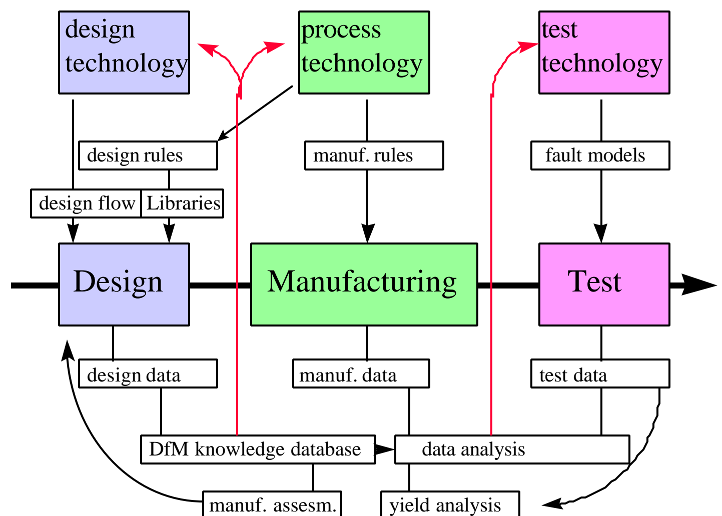

Figure 1: *DfM & Rapid Technology Learning strategy at Philips Semiconductors, MOS4YOU.*

The outline of this short paper is as follows. Section 2 gives an overview of DfM tools for improving IC manufacturability. Section 3 describes the MARYL tool, used within Philips Semiconductors, MOS4*YOU,* as part of the manufacturability assessment of new IC products. In Section 4 a description of a layout postprocessing tool is given, that can be applied to enhance the yield of any product.

2 DfM tools for improving IC manufacturability

When looking at tools for achieving IC manufacturability one can distinct between 3 phases of process maturity:

1] New Process Developments
Process and Device simulators, used by process engineers. These TCAD tools can be used by a DfM engineer to

study the relationship between process parameters and electrical parameters of the IC devices.

2] Design phase [front-end part of the design flow]

Tools that will help mixed-signal designers to perform statistical simulations and process-design centering (robust design). Within Philips Sc so-called Process Blocks are used as statistical design tools that can help the designer to minimise parametric yield loss. These statistical design tools are applied in combination with simulation tools like Spectre, Spice or PSTAR (Philips Semiconductors simulator).

Design phase [back-end part of the design flow]

Tools that will assist the designer to minimise the sensitivity of his design for process disturbances, e.g. random defects, more robustness with respect to critical process steps. Tools like constraint-driven place & routers and layout post-processing tools like wire-spreaders can help here. Some of the issues involved concern: OPC, antenna effect, placement of metal filler cells ("tiles"), critical area reduction and more design related topics like cross-talk reduction, IR-drop, power, EMC,…..

For designers of basic building blocks (library cells, embedded memories) the use of a Compactor tool, driven by a set of preferred process rules, is necessary for constructing DfM-optimised IC's.

Design phase [test-program development]

All 'traditional' DfT (Design-for-Testability) tools should be applied. However for rapid technology learning of deep submicron processes DfT-tools are not able (or only very limited) to achieve tasks like fast fault diagnosis and localisation of visible and 'non-visible' defects.

Testing should supply information about process quality as well as information about product and process debug. Tools that assist designers with Design-for-Debug, Design-for-Analysability and/or Design-for-Failure Analysis are now being developed.

3] Manufacturing & Yield Ramping phase

Yield analysis and optimisation tools are used by product and yield engineers in the waferfab. Design parameters (extracted from the design database), E-sort data and waferfab data (like Do, lot history, PCM data) are the inputs for such a yield management system. An important DfM tool for both designer and waferfab is an accurate yield prediction tool.

As mentioned above the quality and analysability options of the test program plays an essential role in fast identification of the root cause of yield busts.

For process control in the waferfab tools are available which assure optimal process settings to stabilise the process.

Specific reliability tools are not discussed here. In general there is a direct relation between yield and reliability [Ref. 2]. Some simulation tools are being developed that can be used during the design phase (to simulate the hot electron and electro-migration effect)

3 MARYL tool

The MARYL (Manufacturability Assessment and Rapid Yield Learning) tool has been developed at Philips Semiconductors, MOS4*YOU* as a manufacturability sign-off tool to minimise the risks involved with starting high volume manufacturing of new, non proven products in the waferfab. Besides a risk assessment for product-process sensitivities, the tool also provides yield predictions for the product, split-up per functional block and per 'design parameter'. The tool contains an extraction engine that extracts a large number of design parameters, like number and type of library and memory cells used, number of contacts and via's, gate oxide area, critical areas of all metal and poly masks and many other parameters from the design database.

A new project is looking at implementation of the yield prediction part from the MARYL tool in the design flow.

4 Layout post-processing yield enhancement tool

A large percentage of the yield loss in advanced deep submicron IC's can be contributed to defects that occur during the metalization stages of the process. Standard routers introduce minimum spaced tracks by default, because they only take into account minimum values and not the target values. Furthermore yield loss due to charging effects and marginal planarization can also be influenced by the router. Constraint-driven routers could solve these problems, however because these routers are fed with many other constraints as well it is doubtful if they are suited for yield optimization for multi-million transistor designs (at short notice).

A better solution is routing the chip for minimum area using the 'standard' routing tool and do the yield optimization (e.g. by wire-spreading, wire lifting/burying, antenna removal, via doubling,…) by a postprocessing tool. In this way the area of the chip remains unchanged and impact on IC performance will be minimized.

References

[1] W. Maly, "The future of IC design, testing, and manufacturing", *IEEE Design & Test of Computers*, pp. 8, 89-91 Winter 1996

[2] F. Kuper, J. van der Pol, E. Ooms, R. Wijburg, W.Koster, D.Johnston, "Relation between yield

and reliability of integrated circuits*", Proceedings IRPS*, pp. 17-21, 1996.