A Hierarchical Approach for the Symbolic Analysis of Large Analog Integrated Circuits

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Abstract*

This paper introduces a new hierarchical analysis methodology which incorporates approximation strategies during the analysis process. Consequently, the circuit sizes that can be analyzed increase dramatically, without suffering from the combinatorial explosion of expression complexity. Moreover, the interpretability and usability in practical applications is enabled by providing analytical models that keep complexity at a minimum with the prescribed accuracy.

1. Introduction

Symbolic analyzers are aimed to analyze circuits in which part or all their parameters are symbols. The generated expressions provide the keys to understanding the intricate mechanisms underneath the circuit operation. Its applications to providing insight in interactive circuit design, generating behavioral models for library characterization, generating design equations for synthesis or optimization tasks, are obvious [1].

However, the tremendous explosion of expression complexity with circuit size makes necessary the use of approximation techniques. The aim of modern symbolic analyzers is, thus, to provide usable analytical models by generating the simplest expression that represents the dominant behavior of a circuit in the shortest time.

The most recent symbolic analysis approaches calculate the symbolic expressions by applying Simplification Before and During Generation approaches (SBG, SDG), which perform approximations during the equation formulation and generate only the dominant contribution of the solution of the symbolic equations [2]-[4].

Although these approaches have dramatically enlarged the application range of symbolic analysis, there is a limit for their applicability for flat circuit analysis. This limit depends, not only on the circuit size (number of devices/nodes; together with the complexity of the device models used), but also on the circuit connectivity and tightness of the error specifications. When the circuit size grows beyond the limits of flat analysis capabilities, new methods for the analysis and symbolic generation of expressions are needed.

Divide-and-conquer approaches are commonly used by designers when facing the design of complex functionalities. Thus, hierarchical symbolic analysis techniques, that can get benefit from the inherent hierarchy present in large circuits, may enable their symbolic analysis.

However, previously reported approaches for hierarchical symbolic analysis [5]-[7] are not appropriate for the analysis of practical large circuits. No approximation is applied and, consequently, the expression complexities grow exponentially. Then, interpretability is drastically reduced and, more importantly, analyzable circuit sizes are strongly limited unless extremely simple models are used. This is corroborated by the fact that reported experimental results use extremely simple block models; i.e. filters using ideal models for the opamps.

This paper overcomes this problem by introducing a new hierarchical analysis methodology for analog circuits which incorporates error-controlled approximation techniques. The introduction of a modeling strategy in terms of (trans)admittances at each hierarchical level allows to combine very efficient graph methods for the generation of the symbolic expressions and numerical solution of system matrices for error evaluation and control.

2. Hierarchical analysis techniques

2.1. Basic analysis steps

The hierarchical analysis process is usually divided into three main parts (see Chapter 5 in [1]):

A)Circuit Partitioning: the circuit is divided into blocks, preferably in such a way that elements in the same block are strongly interconnected while those in different blocks are weakly interconnected.

B)Terminal Block Analysis: each block is analyzed symbolically. The goal is to model each block only in terms of its inputs and outputs. Since internal nodes mean variables that are eliminated from the equations, this yields a simpler description for the entire circuit.

C)Middle Block analysis: the procedure is to combine blocks that share one or more common *terminal nodes*. This step is performed iteratively while ascending levels in the hierarchy until the complete circuit, described in terms of the global inputs and outputs is reached.

2.2. Previous approaches to hierarchical analysis

For Terminal and Middle Block Analysis, three approaches have been reported: Coates flowgraph, Mason flowgraph and direct network methods.

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Coates flowgraph method

Based on the enumeration of the multiconnections in a block and the successive elimination of some nodes [5]. The method requires to build the Coates graph for the entire circuit, and only then the partitioning is possible. On the one hand, this means that user-defined circuit partitions cannot be handled. On the other hand, since nodes and branches in the Coates graph do not correspond directly with circuit nodes and branches, partitioning information is not clearly mapped to the circuit level.

Mason flowgraph method

Circuit partitioning can be done at the circuit level. Then, Mason signal flowgraph techniques are used to analyze each partition yielding a description in terms of Mason's graphs [6]. This leads to a signal-flowgraph description based only on input and output nodes for each block. Finally, a recombination of the blocks is made applying reduction techniques until a description for the entire circuit is reached.

Direct network method

Partitioning on the circuit level is also possible, enabling to handle pre-partitioned circuits. This method operates by reducing the *Modified Nodal Admittance (MNA) Matrix*, representing each subcircuit into a *Reduced Modified Nodal Admittance Matrix*, which only depends on terminal nodes of the block. Afterwards, a successive recombination of such matrices is performed to obtain a reduced matrix representing the entire circuit [7].

2.3. Comparison of available methods

The hierarchical Coates flowgraph method is not useful to our purposes due to its inability to handle pre-partitioned circuits. Moreover, this method does not show any significant advantage over the other two.

Neither the Direct Network method, nor the Mason flowgraph method incorporate approximation techniques. This exceedingly hampers their application to large practical circuits. Moreover, the result of node reductions in the Mason flowgraph method and matrix operations in the Direct Network method is usually a large sequence of small expressions. This hinders the approximation of an expression of the sequence by pruning its least significant parts, especially if the error committed has to be controlled. Given the capabilities of existing approximation techniques to extract only significant portions of large expressions, on the one hand, and the difficulties associated to propagation of errors introduced by approximation through lengthy sequences of expressions, on the other, it would be more convenient to operate on smaller sequences of formally larger expressions.

3. Hierarchical analysis approach and approximation strategy

A nice characteristic of the hierarchical analysis techniques in Section 2 is that, after matrix recombinations or node reductions, blocks are described using terminal node variables. In our methodology, the blocks at each hierarchical level will also be modeled in terms of their terminal nodes.

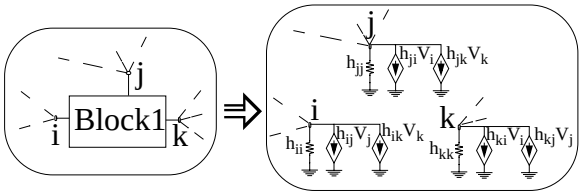

Figure 1. (Trans)admittance description of blocks.

When symbolically analyzing a circuit, a set of network equations (topological and constitutive relationships) has to be solved. For the approximate symbolic solution of a set of linear equations, graph methods have proven to be superior [2]. At any intermediate hierarchical level, the circuit is composed of an interconnection of devices and blocks which are modeled as in Fig. 1. Conventional graph-based flat analysis techniques, like the two-graph method, can be used at this hierarchical level because once the corresponding (trans)admittances replace each block, the circuit is a flat interconnection of basic circuit elements, but with a much smaller number of nodes and devices than a flattened approach.

However, an approximate symbolic solution must be accompanied of an evaluation of the committed errors, which must be performed numerically. But for a numerical error evaluation, the equations must also be solved and this is performed much more efficiently using sparse matrix techniques. An MNA matrix description of the circuit at any hierarchical level can be easily formulated using stamps, as Fig. 2 shows for a circuit containing the block in Fig. 1. Therefore, our hierarchical strategy will be based on graph techniques for the solution of symbolic equations and matrix techniques for the solution of numerical equations in error control tasks. The practical implementation of the methodology is composed of several component modules. The flow diagram of the module structure is shown in Fig. 3.

$$
\begin{array}{c}
\\
n \\ \ldots \\ k \\ \ldots \\ j \\ \ldots \\ i \\ \ldots \\ 2 \\ 1
\end{array}
\begin{array}{c}
\begin{array}{cccccccc} 1 & 2 & \ldots & i & \ldots & j & \ldots & k & \ldots & n \end{array} \\
\begin{bmatrix}
\ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\
\ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\
\ldots & \ldots & h_{ii} & h_{ij} & h_{ik} & \ldots \\
\ldots & \ldots & h_{ji} & h_{jj} & h_{jk} & \ldots \\
\ldots & \ldots & h_{ki} & h_{kj} & h_{kk} & \ldots \\
\ldots & \ldots & \ldots & \ldots & \ldots & \ldots
\end{bmatrix}
\end{array}
$$

Figure 2. MNA matrix of circuit containing Block1.

The needed input data are a hierarchical circuit description, network function to calculate, error constraints and frequency ranges. First, a circuit reduction that imitates the simplifications commonly performed by designers when facing a complex analysis task, is carried out.

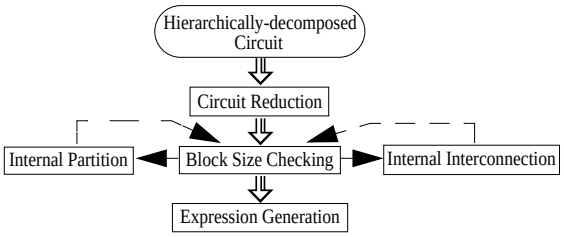

Figure 3. Module structure.

Now, the sizes of the resulting blocks after the circuit reduction step are checked to detect posible non-optimal structures.

Then, the hierarchically decomposed circuits are ready for symbolic generation of the network functions (admittances, transadmittances) of each block. Such network functions are not fully generated but only the dominant part of them. The result of this step is the required network function in SOE format. The main characteristics of the component modules are discussed below.

3.1. Circuit reduction

This module performs node contractions and device removals whose contribution to the global circuit behavior is negligible. Obviously, the error introduced by these circuit transformations must be carefully controlled; this is accomplished by using control algorithms based on interval analysis techniques able to guarantee that the error specifications are fulfilled within the specified frequency range [4].

This circuit reduction technique is applied to the complete flat circuit, although the predefined partitions are formally kept, so that they can be rebuilt when the process is finished. The reason behind is that very efficient sparse matrix techniques are used in the error evaluation; thus, no significant advantage is gained from applying the technique to the component blocks separately.

Moreover, a separate application to each block would require an error propagation mechanism at this early stage of the analysis process. This necessarily yields more conservative results (less reduced circuits) and, consequently, has a negative impact on the global performance of the analysis methodology.

3.2. Internal partition/interconnection

After the circuit reduction process, the hierarchical structure is reconstructed. Then, all blocks are checked to detect too simple or too complex ones.

If a simplified block contains a too reduced number of devices or internal nodes compared with its terminal nodes, analyzing it as an independent block may become inefficient; then, an interconnection is started to look for the best operation: to join it to its best neighbor or incorporate it into the immediately upper hierarchical level.

On the contrary, even after the circuit reduction, some block may still contain too many nodes/devices for an efficient symbolic expression generation (the complexity of the best generation algorithms grows exponentially with the circuit size). In this case, an internal partitioning is provided which finds optimal blocks for the subsequent expression generation module.

To decide if an internal partitioning is needed, three characteristics of the subcircuit after the circuit reduction are taken into account:

- The number of devices.
- The number of nodes.
- The number of capacitors, which is related with the highest power of s in the coefficients of the corresponding transfer function.

This internal partitioning mechanism provides the solution for the case in which no pre-defined partitioning is given: after the circuit reduction strategy, the circuit at hand is internally partitioned to generate a number of blocks that enables an optimal result in terms of computational time and expression complexity.

To preserve user requirements, both processes, interconnection and partitioning, can be controlled by the user.

3.3. Expression generation

Once the hierarchical block structure has been rebuilt and checked, a circuit where blocks are modeled in terms of the (trans)admittances is built-up. Then, appropriate analysis algorithms generate approximate expressions for each (trans)admittance of each block in the hierarchical structure as a function of the component devices of that block. Analogous analysis algorithms are applied to obtain the desired network function (defined by the global input and output signals of the circuit) in terms of the (trans)admittances modeling the blocks at the uppermost hierarchical level.

Each of these term generators operates on a flat circuit. Therefore, the efficient analysis techniques available for flat circuits (based on the two-graph method [2],[3]) can be applied.

An error control mechanism to decide which term generators must become active, is needed to ensure that the resulting expression meets the prescribed accuracy. Its operation is illustrated in Fig. 4

Initially, a frequency value is chosen. Each element has its admittance as associated weight. The weight of each (trans)admittance is a complex number because it functionally depends on all devices composing such block.

The contribution of each (trans)admittance to the global circuit behavior is then numerically evaluated. This is efficiently done using the hierarchical MNA formulation and sparse techniques to solve the MNA matrices. The magnitude of these contributions indicates which term generator must become active. The introduced errors are a combination of the error in each (trans)admittance (only part of it has been generated) and the contribution of such (trans)admittance to the global behavior.

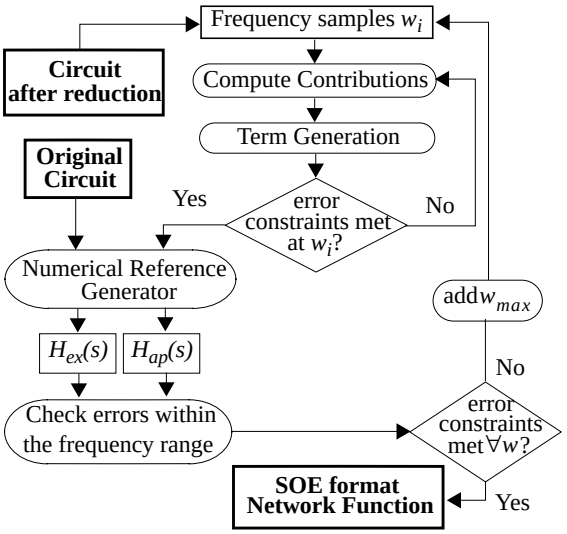

Figure 4. Error-controlled term generation

The generation process continues iteratively until the error criterion is met. Obviously, this is guaranteed only at the selected frequency sample. An algorithm for maximum error detection, which relays in a robust numerical reference generator, [8], and interval analysis techniques are used to detect frequency values within the frequency range where the errors are exceeded [4]. Then, the process is repeated until the error criteria are met in the required frequency range.

4. Experimental results

In this section, two examples are analyzed using the proposed technique. Each is representative of quite opposite application scenarios: a circuit inherently composed of blocks and so provided by the user, and a building block described at the transistor level.

4.1. A band-pass filter

The first example is a decision band-pass filter used in an FSK modem and shown in Fig. 5(a),where the transistor-level schematics in Fig. 5(c)-(d) were used for the OTAs, and the small-signal model in Fig. 5(b) for the transistors. The magnitude / phase error constraints are $|\Delta_{Mag}| \le 1$ dB , $|\Delta_{Phs}| \le 5$ degrees in $10^4 \text{Hz} \le f \le 10^7 \text{Hz}$.

Previously existing hierarchical approaches did not incorporate approximation strategies and, therefore, could analyze the circuit in Fig. 5(a) only if very simple macromodels instead of transistor-level descriptions for the OTAs were used. On the other hand, the flattened circuit is clearly out of the capabilities of flat approaches.

The small-signal expansion of the circuit yields a circuit model with ***618*** devices and ***45*** nodes. After the circuit reduction step, the expanded model contains ***67*** devices and ***26*** nodes, which means a large reduction, but not enough for a flat SDG algorithm.

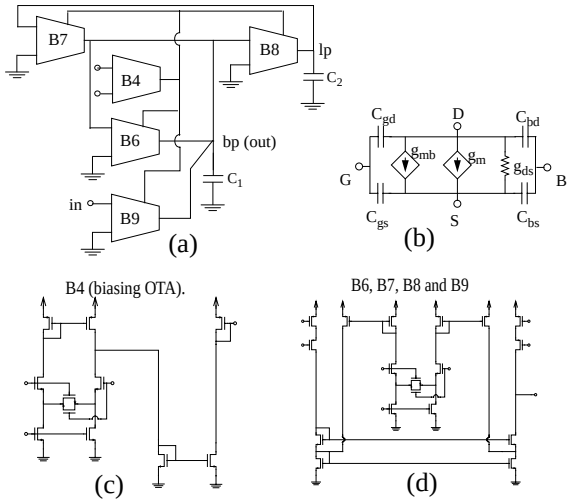

Figure 5. (a) Band-pass filter; (b) small-signal model; (c) biasing OTA; (d) OTA schematics.

Applying our hierarchical approach, the following transfer function is obtained in 100 seconds of CPU time:

$$Tf = \frac{taB9.bp.in \cdot (aB8.lp.lp + C_2 \cdot s)}{-taB7.bp.lp \cdot taB8.lp.bp + aB8.lp.lp \cdot C_1 \cdot s + C_1 \cdot C_2 \cdot s^2} \quad (1)$$

where the (trans)admittances are symbolic expressions with the following composition:

$$\text{taB9.bp.in} = \frac{(gds_2 + gds_3)(gm_{11}gm_{14}gm_{17} + gm_{12}gm_{13}gm_{18})}{gm_{12}gm_{17}(gm_{11} + gds_2 + gds_3)}$$

$$\text{aB8.lp.lp} = \frac{gds_{42}gds_{57}}{gm_{57}}$$

$$\text{taB7.bp.lp} = \frac{(gm_{11}gm_{14}gm_{17} + gm_{12}gm_{13}gm_{18})gds_2}{gm_{12}gm_{17}(gm_{11} + gds_2)}$$

$$\text{taB8.lp.bp} = \frac{(-gm_{11}gm_{14}gm_{17})(gds_2 + gds_3) - gm_{12}gm_{13}gm_{18}gds_2}{gm_{11}gm_{17}(gm_{12} + gds_2 + gds_3)}$$

After substituting each (trans)admittance by its symbolic expression, the transfer function can be evaluated. The error committed when such expression is compared with the magnitude and phase behavior of the original circuit is shown in Fig. 6.

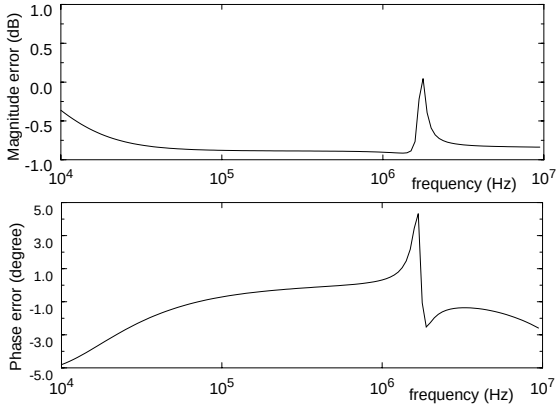

Figure 6. Magnitude and phase errors.

4.2. Rail-to-rail amplifier

Now, the rail-to-rail operational amplifier in Fig. 7 will

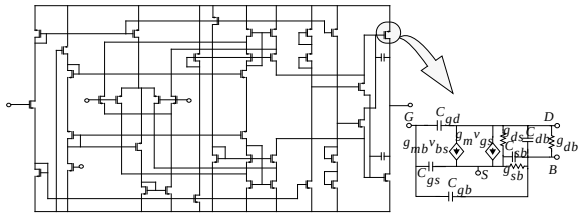

Figure 7. Rail-to-rail operational amplifier and small-signal model for transistors.

be analyzed. The magnitude / phase error constraints are $|\Delta_{Mag}| \leq 3$ dB , $|\Delta_{Phs}| \leq 10$ degrees in $1\text{Hz} \leq f \leq 10^7\text{Hz}$, to include the complete gain-bandwidth product of the amplifier. For that purpose, the netlist is input directly into the hierarchical tool, without any predefined partitioning. The internal checking detects that the flat schematic, after the circuit reduction step, is still too large to be efficiently handled by the expression generation module.

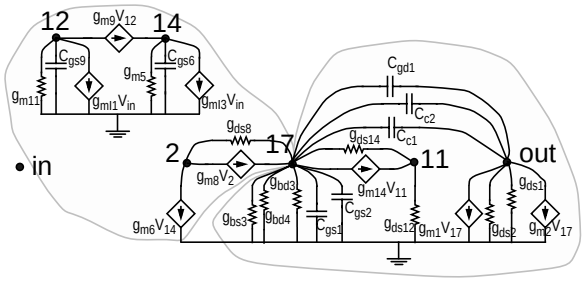

Figure 8. Internal Partitioning selection after Circuit Reduction step.

Therefore, it provides an internal partition, shown in Fig. 8 that yields the following voltage gain:

$$H(s) = \frac{ta2.\text{out}.17 \cdot ta1.17.\text{in}}{a2.\text{out}.\text{out} \cdot a2.17.17 - ta2.\text{out}.17 \cdot ta2.17.\text{out}} \qquad (2)$$

where the (trans)admittances of the blocks are

$$\begin{aligned}
a2.\text{out}.\text{out} &= g_{ds2} + \frac{g_{m14}(C_{c1}+C_{c2}+C_{gd1})s + g_{m14}g_{ds1}}{g_{m14}+g_{ds12}+g_{ds14}} \\
ta2.\text{out}.17 &= \frac{(g_{m14}+g_{ds12})\cdot(g_{m1}+g_{m2})}{g_{m14}+g_{ds12}+g_{ds14}} \\
a2.17.17 &= s(C_{c1}+C_{c2}+C_{gs2}+C_{gs2}) \\
&+ \frac{g_{m14}(C_{gd1}s + g_{bd3}+g_{bd4}+g_{bs3}) + g_{ds12}(g_{ds14}+g_{bd4})}{g_{m14}+g_{ds12}+g_{ds14}} \\
ta1.17.\text{in} &= \frac{g_{m6}(g_{m8}+g_{ds8})(g_{mI3}g_{m11}+g_{mI3}g_{m9}+g_{mI1}g_{m9})}{g_{m5}(g_{m8}+g_{ds8})(g_{m9}+g_{m11})+g_{m8}(g_{m5}C_{gs9}+g_{m11}C_{gs6})s} \\
ta2.17.\text{out} &= s(C_{c1}+C_{c2}+C_{gd1})
\end{aligned} \qquad (3)$$

The results have been obtained in 14 seconds of CPU time.

This example shows that, unlike previous approaches, the resulting methodology does not impose any restriction on the connectivity of the circuits to analyze; it is applicable to either loosely or tightly coupled circuits.

If the results are compared to those obtained through a flat symbolic analysis (a network function with 91 terms is obtained), it is clear that the obtained expressions are more efficient to evaluate and even a better insight can be obtained in the hierarchical case. This makes the proposed methodology competitive with conventional (SBG+SDG)-based techniques when analyzing large building blocks.

5. Conclusions

This paper has introduced a methodology for the incorporation of approximation strategies into a hierarchical analysis method. On the one hand, this overcomes the problems of approximate flat analysis techniques when facing very large circuits. On the other, the inherent hierarchy of large circuits is respected, making the results more interpretable and more efficiently evaluated than if a flat approach were used.

6. References

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