

# The Generalized Boundary Curve - A Common Method for Automatic Nominal Design and Design Centering of Analog Circuits

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## Abstract

*In this paper, a new method for analog circuit sizing with respect to manufacturing and operating tolerances is presented. Two types of robustness objectives are presented, i.e. parameter distances for the nominal design and worst-case distances for the design centering. Moreover, the generalized boundary curve is presented as a method to determine a parameter correction within an iterative trust region algorithm. Results show that a significant reduction in computational costs is achieved using the presented robustness objectives and generalized boundary curve.*

## 1 Introduction

In the era of System-on-Chip (SoC), mixed-signal ICs gain an ever growing market share. For the digital part of those mixed-signal ICs, an established design flow exists, while for the analog designer the circuit simulator is still the most important design tool. In order to keep up with the ever growing demands on the designers' productivity and time-to-market, algorithms and tools for the automatic nominal design and design centering of analog cells are needed to design robust analog cells in acceptable design times.

For the nominal design of analog circuits, big improvements were made in the area of symbolic [5, 12] and simulation-based [4, 10, 14, 16] algorithms. On the other hand, for the design centering statistical [13, 17] and deterministic methods based e.g. on simplicial approximation [6] or ellipsoidal techniques [1] were presented.

More recently, deterministic unified approaches for nominal design and design centering were published, that are based on multiple robustness objectives (MROs) for individual performances e.g. linearized performance penalties (LPP) [11] or worst-case distances (WCD) [2]. But these algorithms suffer from high computational cost that are determined by the number of simulations.

On the one hand the simulation effort is caused by the calculation of the MROs. These MROs give an estimation of the performance-oriented yield of the circuit, but at the beginning of an optimization, the performances are usually far away from their specification and the primary goal is to fulfill the specification. To reduce the simulation cost at that stage, robustness objectives are needed that describe the robustness of the individual performances and can be calculated with as little effort as possible.

On the other hand, the published algorithms transform the MROs into a scalar cost function with a sum of exponential functions. This results in a strongly nonlinear function, while the original MROs are often only weakly nonlinear in the region of interest. This in turn leads to increased simulation costs, if a standard optimization algorithm is used.

In this paper, the *parameter distances* are defined as new robustness objectives for the nominal design, that cause no additional simulation effort compared to a simple sensitivity analysis while they can be used with the same cost function as the WCDs and LPPs. Thus they are a significant progress compared to the state-of-art, since they allow to apply the same algorithms as for the design centering at a significantly lower simulation effort. Additionally, they may also be used if no process statistic is available.

Furthermore, the *generalized boundary curve* (GBC) is presented as a method to determine a step length within an iterative trust-region algorithm. Compared to a trust-region algorithm, that uses the linearized cost function to determine a step length (e.g. [16]), the GBC is based on the full nonlinear cost function calculated with the linearized objectives. Thus the "linearization error" for the strongly nonlinear cost function is kept small. As shown in the results (Section 4), using the full nonlinear cost function based on the linearized objectives significantly reduces the total number of iterations in the optimization. This is a significant improvement compared to gradient-based sizing algorithms like e.g. [16].

The remainder of this paper is structured as follows. In

the following section 2, the parameter distances and WCDs are introduced as robustness objectives for the nominal design and the design centering. Based on these objectives the optimization problem is defined. Section 3 gives a brief overview over the GBC. Section 4 presents results, and section 5 concludes the paper.

## 2 Problem definition

For a fixed topology, an analog circuit can be described by its parameters and performances. The circuit parameters can be divided into three different classes:

- The *design parameters*  $\mathbf{d}$  (e.g. transistor widths and lengths) are tuned by the circuit designer in order to improve the circuit performances and yield.
- For the *operating parameters*  $\theta$  (e.g. supply-voltage and temperature), a tolerance region  $T_\theta$  is defined by the upper bounds  $\theta_u$  and lower bounds  $\theta_l$ :

$$T_\theta = \{\theta \mid \theta_l \leq \theta \leq \theta_u\} \quad (1)$$

The circuit must fulfill the given specifications for all operating parameters within this tolerance-region.

- The fluctuations of the manufacturing process are described by the *statistical parameters*  $\mathbf{s}$  (e.g. oxide thickness). These parameters cannot be tuned by the circuit designer. They are characterized by their mean values  $s_0$ , covariance matrix  $\mathbf{C}$ , and probability density function  $\text{pdf}(\mathbf{s})$ . In the rest of the paper the statistical parameters are assumed to be normally distributed. As shown in [8], this is no serious limitation.

For given parameters, the *circuit performances*  $\mathbf{f}$  can be calculated by simulation. For these performances, *specifications*  $\mathbf{f}_b$  are given and can generally be written as upper bounds:

$$\mathbf{f}(\mathbf{d}, \theta, \mathbf{s}) \leq \mathbf{f}_b \quad (2)$$

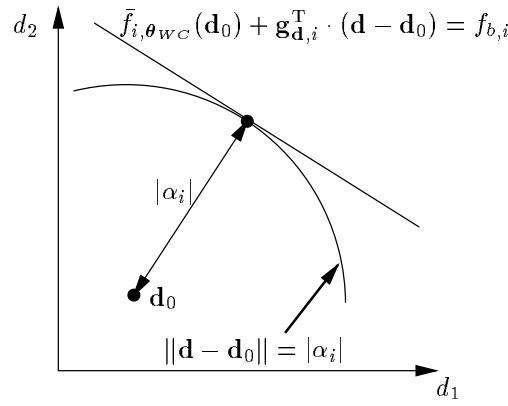
### 2.1 Parameter distances

Goal of the nominal design is to satisfy all specifications with as much safety margin as possible for process variations. This poses the problem to compare different performances with different units (e.g. slew-rate and gain) with each other.

Each performance  $f_i$  is linearized with respect to the design and operating parameters:

$$\bar{f}_i(\mathbf{d}, \theta) = \mathbf{g}_{\mathbf{d}, i}^T (\mathbf{d} - \mathbf{d}_0) + \mathbf{g}_{\theta, i}^T (\theta - \theta_0), \quad (3)$$

with  $\mathbf{g}_{\mathbf{d}, i} = \nabla_{\mathbf{d}} f_i, \quad \mathbf{g}_{\theta, i} = \nabla_{\theta} f_i$



**Figure 1. Parameter distance**

Based on this linearization the influence of the operating parameters can be approximated as:

$$\theta_{WC_i} = \underset{\theta}{\operatorname{argmax}} \{ \bar{f}_i(\mathbf{d}_0, \theta) \mid \theta \in T_\theta \} \quad (4)$$

$$\bar{f}_{i, \theta_{WC}}(\mathbf{d}_0) = \bar{f}_i(\mathbf{d}_0, \theta_{WC_i}) \quad (5)$$

The value  $\bar{f}_{i, \theta_{WC}}(\mathbf{d}_0)$  is the performance value for the approximated worst-case corner  $\theta_{WC_i}$  of the operating parameters.

The sensitivity of a performance can be determined as the norm of its gradient with respect to the design parameters. Taking this into account, the minimum deviation  $\|\Delta \mathbf{d}\|$  of the design parameters that is needed to shift the performance  $\bar{f}_i$  in the linear model from the value  $\bar{f}_{i, \theta_{WC}}(\mathbf{d}_0)$  to the specification  $f_{b,i}$  is an appropriate measure to characterize the distance of the performance from its specification:

$$\|\Delta \mathbf{d}\| = \min_{\mathbf{d}} \{ \|\mathbf{d} - \mathbf{d}_0\| \mid \bar{f}_i(\mathbf{d}, \theta_{WC_i}) = f_{b,i} \} \quad (6)$$

The design parameters are assumed to be scaled, such that the different parameters are comparable. Eq. (6) can be solved exactly using a Lagrange formulation:

$$\|\Delta \mathbf{d}\| = \frac{|f_{b,i} - \bar{f}_{i, \theta_{WC}}(\mathbf{d}_0)|}{\|\mathbf{g}_{\mathbf{d}, i}\|} \quad (7)$$

The value  $\|\Delta \mathbf{d}\|$  in eq. (7) is defined as the *unsigned parameter distance*. A signed parameter distance is introduced, such that fulfilled specifications get a positive sign and violated specifications a negative one. Hence, the *signed parameter distance*  $\alpha_i(\mathbf{d}_0)$  is defined as:

$$\alpha_i(\mathbf{d}_0) = \frac{f_{b,i} - \bar{f}_{i, \theta_{WC}}(\mathbf{d}_0)}{\|\mathbf{g}_{\mathbf{d}, i}\|} \quad (8)$$

The calculation of the parameter distance is illustrated in Figure 1. The parameter distance  $\alpha_i$  considers both, the distance of the performance from its specification, and its

sensitivity with respect to the design and operational parameters. Considering eq. (8) the parameter distance can be interpreted as the distance of the specification from its performance measured in units of the reciprocal value of its sensitivity.

Thus the parameter distance is well-suited to measure the “error” of one performance and compare different performances with each other. Compared to other norms with the same purpose (e.g. generalized  $l_p$ -norm [3]) it has the advantage of being differentiable, if the performance is differentiable. This is a prerequisite for many optimization algorithms. The goal of the nominal design is to tune the design parameters, such that the smallest parameter distances are improved and all parameter distances are as great as possible. This yields a good starting point for design centering.

## 2.2 Worst-case distances

Goal of the design centering is to adjust the design parameters, such that the yield of the circuit is maximized. Generally the overall yield cannot be calculated analytically. As shown in [2] the worst-case distances (WCD)  $\beta_i$  can be used to estimate and improve the yield. The worst-case distances have the following properties:

- The worst-case distances take operating parameters and variations of the statistical parameters, including correlations into account.
- A worst-case distance is negative, if the specification is violated for the worst-case operating parameters. It is positive, if the specification is fulfilled.
- The yield  $Y_i(\mathbf{d}_0)$  with respect to the specification  $f_{b,i}$  can be estimated based on the WCD  $\beta_i$ :

$$Y_i = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\beta_i} \exp(-\xi^2/2) d\xi \quad (9)$$

- Even for a high yield, the worst-case distances still have reasonable variations and thus can be used to further improve the yield and robustness of the circuit.

It can be seen, that the worst-case distances have similar properties as the parameter distances. So, except for their significantly higher simulation effort, they could also be used for a nominal design. In the approach presented in this paper, the parameter distances are used in the nominal design to calculate a good starting point for the design centering and thus reduce the overall number of simulations.

The design centering is based on the worst-case distances as objectives. The aim is to size the circuit, such that all worst-case distances are as great as possible.

## 2.3 Cost function

In both cases the goals for the design centering and nominal design are to maximize all objectives but especially the smallest ones. This means, that from a mathematical point of view, the two optimization tasks are the same. For the rest of the paper, the objectives are denoted with  $\gamma_i(\mathbf{d}_0)$ . For the design centering,  $\gamma_i$  is equal to the WCD  $\beta_i$ , for the nominal design,  $\gamma_i$  denotes the parameter distance  $\alpha_i$ . It is important to note that the proposed method is not limited to WCDs and parameter distances. In fact it can be applied to any differentiable robustness objectives and cost function, as long as the cost function is convex for the linearized robustness objectives.

As proposed in [2, 11], a suitable cost function  $\varphi$  for the proposed optimization task is:

$$\varphi(\mathbf{d}) = \sum_{i=1}^{n_\gamma} \exp(-a \cdot \gamma_i(\mathbf{d})), \quad a > 0 \quad (10)$$

The constant factor  $a$  in this equation is a scaling factor for the objectives. The cost function (10) is constructed, such that small or negative objectives have a high contribution to the overall cost and positive ones only have a minor contribution.

An automatic circuit sizing is only feasible if the principal functionality of the circuit is guaranteed during the whole sizing process by considering functional constraints (e.g. saturation condition for the MOS-transistors of a current mirror) [7, 16, 18]. These constraints can be divided into equality constraints for design parameters and inequality constraints for parameters and simulated properties.

Every equality constraint reduces the number of free design parameters by one and therefore reduces the design space and speeds up the sizing. The inequality constraints  $\mathbf{u}(\mathbf{d})$  are formulated such that fulfilled constraints are positive:

$$\mathbf{u}(\mathbf{d}) \geq \mathbf{0} \quad (11)$$

These constraints are either constraints on parameters or on simulated properties, that can be extracted from a DC-simulation, that must be done anyway. Thus they cause no additional simulation effort.

Combining the constraints (11) and the cost function (10), the sizing problem can be formulated as:

$$\min_{\mathbf{d}} \{ \varphi(\mathbf{d}) \mid \mathbf{u}(\mathbf{d}) \geq \mathbf{0} \} \quad (12)$$

## 3 The generalized boundary curve

The minimization problem (12) could be solved using a standard optimization algorithm. But as stated in the introduction, due to the strongly nonlinear cost function this may result in a huge number of iterations.

On the other hand, trust-region algorithms have proven to be very effective within circuit design (e.g. [16]). As key task in each iteration of these algorithms a parameter correction has to be determined, that has a good ratio between error reduction and norm of the parameter correction, such that the linearization is still valid for the chosen step-size.

The CBC [16] turned out to be very well suited for this job in presence of linearized objectives. Therefore in this paper the GBC is presented as a generalization of the CBC, that inherits its most important properties but is also suited for the proposed strongly nonlinear cost function. The sizing algorithm itself is the same as the one presented in [16], except that the GBC is used to determine a parameter correction.

The main idea of the GBC is, not to use the linearized cost function but only the linearized objectives to calculate a boundary curve similar to the characteristic boundary curve. The objectives  $\gamma$  and the constraints  $u$  are linearized at the linearization point  $d_0$ :

$$\gamma(d) = \underbrace{\gamma(d_0)}_{\gamma_0} + \underbrace{\nabla_d \gamma|_{d=d_0}}_{S} \cdot (d - d_0) + \dots \quad (13)$$

$$u(d) = \underbrace{u(d_0)}_{u_0} + \underbrace{\nabla_d u|_{d=d_0}}_{U} \cdot (d - d_0) + \dots \quad (14)$$

Based on the linearized objectives, the approximated objective function  $\bar{\varphi}(x)$  is set up:

$$\bar{\varphi}(x) = \sum_{i=1}^{n_\gamma} \exp(-a \cdot \bar{\gamma}_i(x)) \quad (15)$$

Similarly to the CBC the cost function (15) is modified in order to find a good compromise between the error reduction and the norm of the parameter correction:

$$\bar{\Phi}(x, \lambda) = \bar{\varphi}^2(x) + \lambda \cdot \|x\|^2, \quad \lambda \geq 0 \quad (16)$$

The factor  $\lambda$  is a weight for the parameter correction. Based on (16) the modified optimization problem is set up:

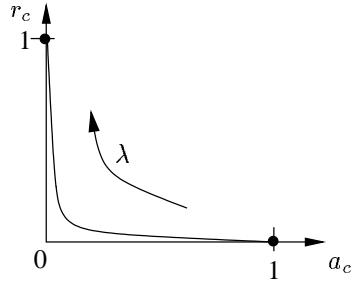
$$x_c(\lambda) = \underset{x}{\operatorname{argmin}} \{ \bar{\Phi}(x) | \bar{u}(x) \geq 0 \} \quad (17)$$

$$\bar{\varphi}_c(\lambda) = \bar{\varphi}(x_c(\lambda)) \quad (18)$$

To solve this problem, no simulations are necessary, because it relies on the linearized objectives. As suggested in [16] the resulting parameter correction  $\|x_c\|$  and the cost function  $\bar{\varphi}_c$  are transformed, such that all solutions are in the interval  $[0, 1]$ :

$$a_c(\lambda) = \frac{\|x_c(\lambda)\| - \|x_c(\lambda \rightarrow \infty)\|}{\|x_c(0)\| - \|x_c(\lambda \rightarrow \infty)\|} \quad (19)$$

$$r_c(\lambda) = \frac{\bar{\varphi}_c(\lambda) - \bar{\varphi}_c(\lambda \rightarrow \infty)}{\bar{\varphi}_c(0) - \bar{\varphi}_c(\lambda \rightarrow \infty)} \quad (20)$$



**Figure 2. Typical example for a GBC.**

A typical example of a GBC is shown in Fig. 2, where the GBC is the generalization of the CBC. The CBC can only be applied to linear objectives transformed into a scalar quadratic cost function. Whereas the GBC is suitable for any cost function, that is convex for the linearized objectives. For the GBC following theorems are true (proofs see [15]):

**Theorem 1** If  $\bar{\varphi}(x)$  is convex and the active constraints are linearly independent,  $x_c(\lambda)$  is the parameter correction with minimum  $\bar{\varphi}(x)$  for all  $x \in \mathcal{D}$  and  $\|x\| \leq c = \|x_c(\lambda)\|$ .  $\square$

**Theorem 2** If the cost function  $\bar{\varphi}(x)$  is convex, then the resulting parametric curve  $[a_c(\lambda), r_c(\lambda)]^T$  is convex.  $\square$

**Theorem 3** The slope  $m_c$  of the GBC is given by:

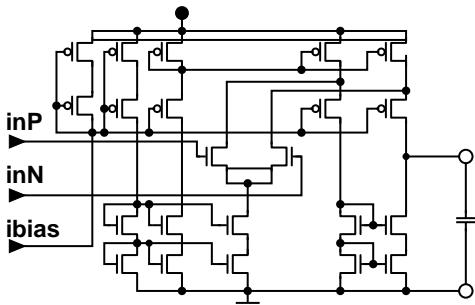
$$m_c = -\lambda \frac{\|x_c(\lambda)\|}{\bar{\varphi}_c(\lambda)} \cdot \frac{\|x_c(0)\| - \|x_c(\lambda \rightarrow \infty)\|}{\bar{\varphi}_c(0) - \bar{\varphi}_c(\lambda \rightarrow \infty)} \quad (21)$$

These theorems show, that the GBC inherits all important properties from the CBC. Theorem 1 and 2 mean, that the GBC is suitable to determine a parameter correction in an automatic sizing algorithm. Theorem 3 guarantees that the GBC can be approximated with the same algorithms as the CBC and an identical algorithm can be used to search the kink of the curve. This kink represents a parameter correction, that on the one hand has a reasonable step size and on the other hand a significant error reduction.

## 4 Results

The introduced sizing method was used to design a folded cascode operational amplifier (Fig. 3) and an output buffer (Fig. 4).

The folded-cascode operational amplifier consists of 22 transistors, which result in 44 possible design parameters. Based on the structural constraints, the number of these can



**Figure 3. Folded-cascode operational amplifier**

be reduced from 44 to 9 design parameters. The operating conditions are described by 4 operating parameters and the process statistic is modeled with technology data from Infineon Technologies. The detailed sizing results are shown in Table 1.

Perf.	Spec	Initial Val/WCD	Nominal Val/WCD	Centered Val/WCD
$A_0[\text{dB}]$	>65	95/0.2 $\sigma$	76/2.7 $\sigma$	76/4.2 $\sigma$
$f_t[\text{MHz}]$	>30	21/-9.7 $\sigma$	68/8.0 $\sigma$	58/4.5 $\sigma$
PHM[°]	>60	39/-6.6 $\sigma$	67/1.6 $\sigma$	71/3.9 $\sigma$
Slew <sub>p</sub> [V/ $\mu$ s]	>32	20.8/—	67/6.4 $\sigma$	58/3.9 $\sigma$
Power[mW]	<3.5	1.1/6.0 $\sigma$	2.6/0.9 $\sigma$	2.3/4.2 $\sigma$
Yield (WCD)	—	0.0%	76.2%	99.9%
Yield (MC)	—	0.0%	77.3%	100%

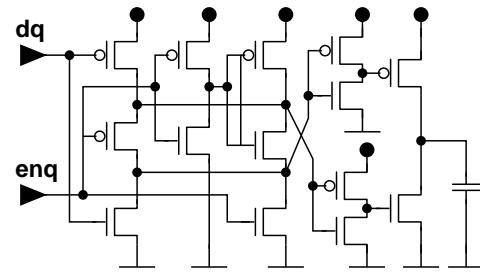
**Table 1. Sizing results and yield estimations based on worst-case distances (WCD) and a 1000 sample Monte Carlo analysis (MC) for the OP**

All sensitivities were calculated with forward finite differences with Infineon's in-house simulator TITAN [9] on a Pentium II/450MHz. A further reduction in simulation time can be expected if simulator-built-in sensitivities are used.

Especially remarkable are the results for the gain  $A_0$  of the operational amplifier. The design centering improves the WCD from 2.5 to 4.2 in 3 iterations, but the performance value is 76dB in both cases. This shows, that a parameter set is calculated where the circuit is significantly less sensitive to variations of the production process and the operating conditions. Such a solution can only be calculated by a design centering, that takes both statistical and operational parameters into account.

For the output buffer a technology transfer was done. This means, that the values for the design parameters are taken from an old technology and are scaled down. Afterwards a resizing is necessary in order to fulfill the specifications. Table 2 summarizes the results for the output buffer.

In both cases a good starting point for the design centering was calculated in the nominal design. This is enabled by the parameter distances as robustness objectives. Thus the number of iterations in the subsequent design centering



**Figure 4. Output buffer**

Perf.	Spec	Initial Val/WCD	Nominal Val/WCD	Centered Val/WCD
Delay <sub>fall</sub> [ns]	<4	3.2/2.5 $\sigma$	2.4/5.4 $\sigma$	2.6/4.8 $\sigma$
Delay <sub>rise</sub> [ns]	<4	3.9/-0.2 $\sigma$	2.8/2.9 $\sigma$	2.7/3.4 $\sigma$
Slope <sub>fall</sub> [ns]	<4.5	5.0/-1.7 $\sigma$	3.0/5.4 $\sigma$	3.1/3.7 $\sigma$
Slope <sub>rise</sub> [ns]	<4.5	6.7/-3.4 $\sigma$	3.3/2.5 $\sigma$	3.3/3.4 $\sigma$
Noise <sub>gnd</sub> [mV/nH]	<25	12.3/6.8 $\sigma$	14.9/4.1 $\sigma$	14.4/3.9 $\sigma$
Noise <sub>vdd</sub> [mV/nH]	<25	12.3/6.8 $\sigma$	14.4/4.3 $\sigma$	15.3/3.4 $\sigma$
Yield (WCD)	—	0.0%	99.2%	99.9%
Yield (MC)	—	0.0%	98.9%	100%

**Table 2. Sizing results and yield estimations based on worst-case distances (WCD) and a 1000 sample Monte Carlo analysis (MC) for the output buffer**

is kept small, which is essential for an industrial applicability of a design centering algorithm. For both circuits it was possible to calculate a  $3\sigma$  design or better.

As stated in section 3, the circuit sizing could also be done with a standard optimization algorithm. But due to the strongly nonlinear cost function, this may result in a significantly larger number of iterations.

The results archived with the GBC-based algorithm are compared to the standard gradient-based algorithm discussed in [16]. Both algorithms resulted in nearly the same solution (performance differences less than 2%, WCD differences less than 0.1). But as shown in Table 3 the simulation effort for the gradient-based algorithm was significantly higher.

	OpAmp		Buffer	
	Grad.	GBC	Grad	GBC
Iterations nom. design	14	6	6	3
CPU nom. design	769s	305s	337s	147s
Iterations design cent.	5	3	6	2
CPU design centering	2812s	1567s	3310s	1160s
Average lin. error	95%	28%	58%	15%
Average $\ x\ $	0.13	0.35	0.05	0.11
Reduction in sim. time	48%		64%	

**Table 3. Comparison of GBC and gradient-based minimization algorithm**

For the gradient-based algorithm, due to the high linearization error, only small steps were possible. Thus, more iterations were needed to achieve the same results.

For the GBC based algorithm the linearization error was rather small. This shows, that the robustness objectives are only weakly nonlinear and thus the estimation of the error on linearized objectives gives a good idea of the real error.

## 5 Conclusion

In this contribution an automatic sizing method for analog cells based on robustness objectives was presented. The proposed method is suitable for both nominal design and design centering. Robustness objectives for the design centering are the worst-case distances (WCD); for the nominal design, the parameter distances are introduced as robustness objectives.

The chosen sizing algorithm requires the transformation of the robustness objectives into a cost function via a sum of exponential functions. This results in a strongly nonlinear cost function, even for linear objectives. To overcome this problem, the generalized boundary curve (GBC) is introduced. This GBC is based only on the linearized objectives themselves and not the strongly nonlinear cost function. Thus the linearization error is kept small. In every iteration step of the sizing algorithm, the GBC is used to calculate a parameter correction with a good ratio between error reduction and norm of the parameter correction.

Results show that a reduction in computational costs of about 50% with respect to [16] is achieved by the presented robustness objectives and generalized boundary curve.

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## References

- [1] H. Abdel-Malek and A. Hassan. The ellipsoidal technique for design centering and region approximation. *IEEE Trans. on CAD*, 10:1006–1013, 1991.
- [2] K. Antreich, H. Graeb, and C. Wieser. Circuit analysis and optimization driven by worst-case distances. *IEEE Trans. on CAD*, 13(1):57–71, 1994.
- [3] J. Bandler and S. Chen. Circuit optimization: The state of the art. *IEEE Trans. on Microwaves Theory Techniques (MTT)*, 36:424–442, 1988.
- [4] A. R. Conn, P. K. Coulman, R. A. Haring, G. L. Morill, C. Visweswarah, and C. W. Wu. JiffyTune: Circuit optimization using time-domain sensitivities. *IEEE Trans. on CAD*, 17(12):1292–1309, Dec. 1998.
- [5] M. del Mar Hershenson, S. P. Boyd, and T. H. Lee. GPCAD: A tool for CMOS op-amp synthesis. In *IEEE/ACM Int. Conf. on CAD (ICCAD)*, 1998.
- [6] S. Director, W. Maly, and A. Strojwas. *VLSI Design for Manufacturing: Yield Enhancement*. Kluwer Academic Publishers, USA, 1990.
- [7] J. Eckmueller, M. Groepl, and H. Graeb. Hierarchical characterization of analog integrated CMOS circuits. In *Design, Automation and Test in Europe (DATE)*, pages 636–643, Paris, France, Feb. 1998.
- [8] K. Eshbaugh. Generation of correlated parameters for statistical circuit simulation. *IEEE Trans. on CAD*, 11:1198–1206, 1992.
- [9] U. Feldmann, U. Wever, Q. Zheng, R. Schultz, and H. Wriedt. Algorithms for modern circuit simulation. *Archiv für Elektronik und Übertragungstechnik (AEÜ)*, 46:274–285, 1992.
- [10] M. Krasnicki, R. Phelps, R. A. Rutenbar, and L. R. Carley. MAELSTROM: Efficient simulation-based synthesis for custom analog cells. 1999.
- [11] K. Krishna and S. Director. The linearized performance penalty (LPP) method for optimization of parametric yield and its reliability. *IEEE Trans. on CAD*, 14(12):1557–1568, Dec. 1995.
- [12] F. Leyn, W. Daems, G. Gielen, and W. Sansen. A behavioral signal path modeling methodology for qualitative insight in and efficient sizing of cmos opamps. In *IEEE/ACM Int. Conf. on CAD (ICCAD)*, 1997.
- [13] M. D. Meehan and J. Purviance. *Yield and Reliability in Microwave Circuit and System Design*. Artech House Boston/London, 1993.
- [14] E. S. Ochotta, R. A. Rutenbar, and L. R. Carley. Synthesis of high-performance analog circuits in ASTRX/OBLX. *IEEE Trans. on CAD*, 15(3):273–294, March 1996.
- [15] R. Schwencker. Automatic design centering of analog integrated circuits based on the generalized boundary curve of multiple robustness objectives. Technical Report TUM-LEA-99-1, Technical University Munich, 1999.
- [16] R. Schwencker, J. Eckmueller, H. Graeb, and K. Antreich. Automating the sizing of analog cmos-circuits by consideration of structural constraints. In *Design, Automation and Test in Europe (DATE)*, Munich, Mar. 1999.
- [17] J. C. Zhang and M. A. Styblinski. *Yield and Variability Optimization of Integrated Circuits*. Kluwer Academic Publishers, 1995.
- [18] S. Zizala, J. Eckmueller, and H. Graeb. Fast calculation of analog circuits' feasibility regions by low level functional measures. In *IEEE Int. Conf. on Electronics, Circuits and Systems*, pages 85–88, Sept. 1998.