

Virtual Components Application and Customization

Jean-François Agaësse and Bernard Laurent

ASIC Product Line
Thomson CSF Semiconducteurs Spécifiques TCS
Avenue de Rocheplaine BP 123
38521 Saint Egrève Cedex FRANCE

1 Motivation

The competitive pressure for time-to-market and the tremendous integration capacity provided by the silicon technology developers has raised the promise of systems-on-a-chip. This inescapable evolution however increases the need for cost effective design methodologies and solutions, and the electronic engineering and design community is now firmly convinced that it can not be accomplished without a systematic use of already designed and qualified components, in a similar approach to the one already familiar to software developers. Complex system functions, improperly named IPs, are delivered by ASIC suppliers, created by the customer or developed by independent specialized companies, and offered to system designers, in the form of dedicated predesigned circuit blocks, allowing them to best use their expertise and creativity and finally keep pace with the dramatic productivity challenge required to make the system level silicon a reality.

2 Reuse of IP

Currently, reuse of IP is slowly turning to reality. Recently, a major system house reported the first massively IP-based designs, with more than 60% of the silicon area occupied with Virtual Components of different type and provenance [1]. However, despite the effort of IP providers to deliver well-designed, documented and qualified components, the route from “plug-and-pray” to “plug-and-play” is still long, and painful. It might finally turn-out that the growing demand for IP application and customization will make the “plug” objective an inaccessible dream.

To face the increasing demand for support when exercising the most popular IP, some silicon manufacturers did not hesitate to develop integrated solutions, based on their own experience and the most frequently demanded functionality enhancements from their customer, to simplify the use of the component. In late 1998, an embedded array has been released, that combines all blocks and glue required for ARM-based applications [2].

3 Customization of IPs

Meanwhile, it appears that even the most popular and frequently used components, although they implement a well established standard, require a minimum customization to fit in the application. This trend is clearly demonstrated by the number of available components that implement the popular PCI or USB standards and that are registered in [3]. An other example of this need for local adaptation is described in [1].

However, the need for local adaptation might go well, the customer demands for a simple interfacing function, requested to connect the virtual component to the rest of the application. Nevertheless, this demand is on the way to be satisfied, and the silicon prophets predict that the heavy specification work undertaken under the umbrella of VSIA will ultimately lead to the definition of a standardized bus that will be the back-bone of the IP-based system industry. In fact, the spectrum of customization is much wider. It extends from the insertion of testability resource, in the simplest form of scan-based

approach or by the means of generalized or dedicated BISTs, up to a complete flexibility of the proposed device.

The demand for flexibility is of course - more or less - fulfilled by parametrized IPs [4], that open at least as many issues as they solve problems. For instance, in the field of high-performance *Forward-Error-Correction* components for high bit-rate wireless communication applications, the selection of the best suited parameters is only made possible if an abstract - but yet accurate - model is released to the customer, to help in the architecture definition step, as well as in the trimming of the different blocks. However, the issue is to release the circuit blocks that will fit at best in the application needs, if the functional parameters of each function are frozen. Depending on the transmission environment (channel capacity, bit-rate, ...), a dedicated protocol must be added to the core functionality, that cannot reasonably be implemented up front, without the guarantee it will fulfill the application's architectural requirements and meet system designer's expectations. When high performance is expected, an interface layer can no longer be added on the top of the existing component, that would dramatically impact the overall performance of the application. Ultimately, the quest for flexibility could require to turn a "parametrized" component, for which generic parameters are set to the appropriate value at the silicon compilation time, and to a "configurable" component, that would implement enough resource on silicon to allow the on-life configuration. Therefore, an entire **family** of virtual components must then be developed, qualified and documented, closely based on the root technology.

In summary, the challenge is then to address the documentation, (area/performance/power trade-off), the qualification, the testability, for more instances than a designer could handle in its own life. Only the dialog between the IP provider and the customer, as well as dedicated service for instance-based validation, e.g., by the mean of fast prototyping, can establish the level of confi-

dence and trust required for the success of such components.

4 Conclusion

Despite the growing pain for their integration in today's designs, Virtual Components are on the way to take a key part in developing the System-on-Chip required for the next generation of communication products. The customers' need for assistance in the IP application and customization raises the promise for a fruitful business, based on service and dedicated support. New resources must be allocated by Virtual Component developers a/o providers, ASIC providers, and dedicated independent companies, so as to serve at best the customers' expectations.

5 References

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