SINGLE CHIP OR HYBRID SYSTEM INTEGRATION

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If we continue to increase the complexity of ICs at the same pace as we did from 1960 onwards, this complexity will have reached a level of half a billion transistors per chip very soon and the clock period is 'expected' to be below the one nanosecond. This evolution is rapidly leading to forecasts of Systems-on-Chip designed at processor-memory level and containing a lot of mixed-signal and even RF architectures. Chip complextiy will exceed that of most of today's PCB's. Hence, chips will no longer be stand alone system components but "silicon boards" encapsulating complex system knowledge, specified in software-like languages and implemented in novel heterogeneous architectures. This is a commandable goal but it is also fair to question whether this is a viable goal.

There is a general awareness that there are some limits to CMOS performance in the future. This creates uncertainty about the long term future for CMOS monolithic integration . This means that slopes for curves that predict improvement trends for CMOS technology will ultimately saturate. As this happens, pressure will be put upon the design community to find better and cheaper ways to improve performance of complex systems.
Some concerns for the future of single chip systems are :

- The increasing dominance of physical effects that create interference and noise in VLSI designs, more and more requires analog measures to limit their influence.
- The spectacular progress of micro-electronics has been driven by the development of better processing technologies, using constantly improved, but also more expensive manufacturing technology. As a consequence it can be expected that the cost of silicon will have to consume a rapidly increasing portion of the available profit margins.
- To date, CMOS density and performance development was aided by the proces of scaling. A parameter that is known not to scale properly is the interconnect resistance. The RC delays of long lossy lines can be overcome somewhat by using copper and low-K dielectrics, but these are stopgap measures which do not address the fundamental problem.
- The I/O to the next level of packaging is not growing as fast as the scale of integration. This leads to chips that are powerful but many of the on-chip resources are not available to the system designer.

As consequence, the distribution of system functionality between the chip and the packaging level can offer several technical benefits. To exploit the inherent potentials of hybrid system integration a lot of fascinating research topics calls upon academia and industry. However, the question can be posed whether a strategy towards hybrid integration can be of benefit for the IC manufacturing industry that will have to support it. For example the reserved introduction of bare dies is an illustration of divergent interests between IC manufacturer and system manufacturer.