Exploring the Combination of I_{DDQ} and i_{DDt} Testing: Energy Testing

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Abstract

The feasibility of combining I_{DDQ} and i_{DDt} testing to detect defective circuits by measuring the energy consumed by the tested circuit is considered. The energy chronogram of a circuit is used as an Energy Signature which makes it possible to distinguish between defect-free and defective circuits. Exploratory implementation of the proposed method is presented and experimental results obtained from in-house full custom circuits and commercially available circuits are discussed.

1. Introduction

Conventional voltage based testing methodologies are fast and efficient provided that defects can be excited and observed. However, there are many defects (like bridges, GOS or floating gates) which may not cause an observable logic fault and, therefore, its detectability is not guaranteed [1]. New methodologies, such as I_{DDQ} testing, solve some of these problems [2][3][4]. However, I_{DDQ} testing does not detect defects which do not produce sufficient increase of the quiescent current. Also, defects producing exclusively changes in the dynamic current are not I_{DDQ} testable [5]. In addition, the I_{DDQ} test must be applied at very low rates due to the long time needed by the circuit under test (CUT) to reach its quiescent state.

On the other hand, a different test methodology, named i_{DDt} testing, tries to overcome the shortcomings of I_{DDQ} testing by measuring the transient current of the circuit [11]. Such methodology may be effective to detect defects, for example some opens that modify this current or other defects not detected by I_{DDQ} testing. However, it also presents problems related to the detection of small changes in the dynamic current of a large circuit [12].

In this paper, we explore the possibilities of combining the I_{DDQ} and i_{DDt} tests by the use of a new observable to test CMOS circuits: energy consumption. Indeed, the energy consumed by a CMOS circuit during a time interval is the sum of dynamic capacitive energy (due to the charge and the discharge of the circuit capacitances), short-circuit energy (due to the short-circuit current), and static energy (due to the quiescent current). Thus, the energy consumption of CMOS circuits reflects changes in the switching activity modifying the dynamic and short-circuit current. The changes in the quiescent current I_{DDQ} are also reflected by the energy consumed during the period of the time interval in which the signals remain in quiescent state. Consequently, the energy chronogram of a given circuit for a given input sequence and given environmental conditions can be conceived as an *Energy Signature* of this circuit [6]. Recently, this subject has been addressed in [10] but restricted only for defects that change the logic behavior of the CUT.

In the presence of defects, changes in the Energy Signature are expected. For instance, if a bridge exists between two circuit nodes, an increase in the static consumption may be observed each time the bridge is excited. Also, changes in the dynamic consumption are expected due to the changes in the voltage swing in the bridged nodes. Moreover, depending on the characteristics of the bridge, changes in the global behavior of the circuit may appear, thus modifying the internal activity and the dynamic consumption.

In this paper we analyze the possibilities to determine the presence of defects in a tested circuit by comparing its Energy Signature with the Energy Signature of a "golden" circuit. The variations in the Energy Signature of defect-free circuits due to the fabrication process determine the valid Energy Signature window which makes it possible to distinguish between "good" and "defective" circuits.

The rest of the paper is structured as follows. In the next section we present an analysis of the energy consumed by the CUT and the proposed implementation of the Energy Signature test. In section three, we show experimental results on real circuits with and without artificially introduced bridges. Finally, in section four,

the conclusions of the paper are presented.

2. Analysis and implementation of the Energy Signature Test

In order to analyze the differences between the energy consumed by a defect-free circuit and an identical defective one, we consider that the input sequence applied to the circuit and the environmental conditions such as temperature or supply voltage are the same for both circuits. This condition is necessary to avoid changes in the energy chronogram not due to defects.

An example of the energy chronogram of a defect-free and a defective circuit is outlined in Figure 1, where we assume that the static consumption of a defect-free circuit is negligible.

In this chronogram, we can see how there is the same evolution in the energy consumed by the defective and the defect-free circuit for the first three input vectors. The fourth vector excites the defect in the defective circuit and generates a static consumption, as shown by the linearly increasing energy consumption during the application of vector four. In this illustrative example it is assumed that, as a consequence of the defect, only the static consumption is changed. In vector twenty-second the defect is excited again, thus generating an additional amount of extra static consumption.

If, as a consequence of the defect, the circuit changes the behavior of other parts of the CUT in addition to the electrical paths containing the defect, the energy chronogram may be very different because the dynamic consumption may change significantly.

In any case, equipment able to record the energy chronogram with enough precision to discriminate between defective and defect-free circuits is required. In the next subsection, we describe an implementation of such equipment.

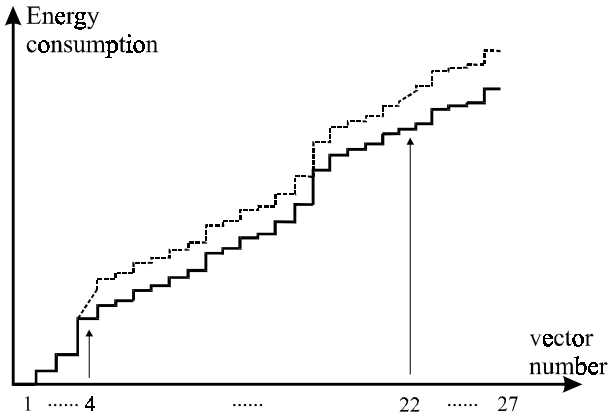

Figure 1. **The solid line is the chronogram of the energy consumed by a defect-free circuit. The dotted line is the chronogram for a defective circuit.**

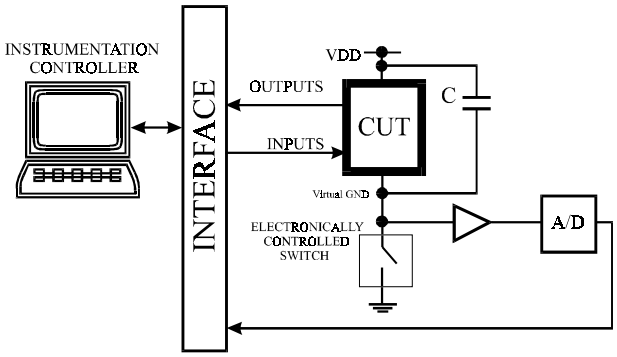

Figure 2. **Testbench implementing the Energy Signature test.**

2.1. Implementation of the Energy Signature test

To record the Energy Signature we use the following approach (see Figure 2): the power supply current of the CUT is provided by a linear capacitor C, while the CUT receives a sequence of input vectors from $t = 0$ to $t = t_1$. As a consequence, capacitor C is partially discharged and the voltage at the virtual ground node increases.

The change in the energy stored in the capacitor in the period of time $0 - t_1$, is *exactly the same* as the energy consumed by the circuit in the same period [7]. The evolution of the voltage in the capacitor is used to obtain the chronogram of the energy consumed by the CUT.

The measuring system reads the voltage appearing in the opened switch as long as the instrumentation controller supplies the circuit inputs. This implementation follows closely the proposal of Keating-Meyer [9] for I_{DDQ} testing.

In order to avoid an excessive voltage at the CUT's virtual ground node, the switch is closed each time the voltage V_{GND} reaches a given threshold.

Each time the switch is closed, a "quantum" of energy is consumed by the circuit. This "quantum" is equal to the difference of the energy stored in C when it is at V_{DD} volts and at $V_{DD} - V_\alpha$ volts:

$$E_Q = \frac{1}{2} C V_{DD}^2 \left[2 \left(\frac{V_\alpha}{V_{DD}} \right) - \left(\frac{V_\alpha}{V_{DD}} \right)^2 \right] \qquad (1)$$

where V_α is the maximum voltage allowed at the CUT's virtual ground. Voltage V_α need to be small (0.1 - 0.2 V) in order to operate under similar conditions as the circuit in normal operation.

The computation of the Energy Signature is made by recording the number of input vectors needed by the circuit to consume each "quantum" of energy, E_Q which is proportional to the time elapsed with the switch open.

2.2 Discriminating between "good" and "bad" circuits

The Energy Signature of a CUT is a set of k numbers $S = \{n_1, n_2, ...n_k\}$, each one of which is the number of input vectors needed by the circuit to consume E_Q. The energy consumed by the n_i vectors applied after the i_{th} opening of the switch is denoted by $E(n_i)$. The switch is closed when the consumed energy is equal or just exceeds the preselected "quantum" E_Q. Formally:

$$E(n_i - 1) < E_Q \leq E(n_i) \qquad (2)$$

where $E(n_i - 1)$ is the energy consumed by the CUT when it receives the first $n_i - 1$ input vectors, and $E(n_i)$ is the previous energy plus the energy consumed by the CUT in the transition from the $(n_i - 1)^{th}$ vector to the $(n_i)^{th}$.

The following question arises: how to distinguish between the Energy Signatures of a defective and a non-defective circuit? The following facts need to be considered:

1. The *total* energy consumption (for a given input sequence) of a defective circuit can be not only greater or smaller, but also *equal* to the consumption of a defect-free one. A "bad" circuit may be erroneously detected as a "good" one.

2. The energy consumption of different samples of the same defect-free circuits is not exactly equal due to noise and to small changes in the geometric and physical parameters imposed by the fabrication process. A "good" circuit may be erroneously classified as a "bad" one.

The following method gives good results to discriminate between "good" and "bad" circuits; as shown in Section 3.

a) From a defect-free circuit, we define the "golden" Energy Signature by obtaining k numbers: $S_G = \{n_{G1}, n_{G2}, ...n_{Gk}\}$. It will be the reference signature for a test vector sequence.

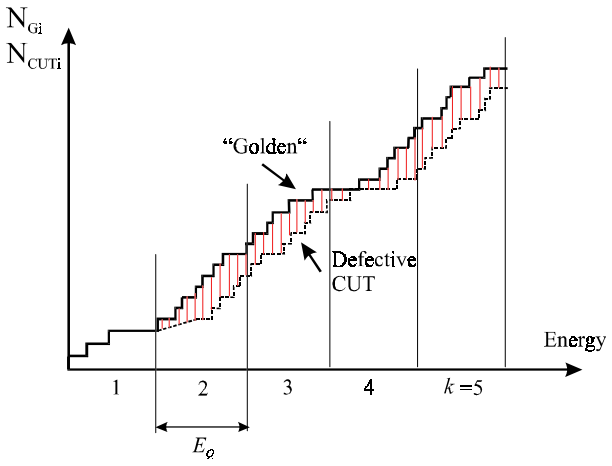

Figure 3. **Number of vectors as a function of the energy consumed by the "golden" circuit and a defective CUT.**

b) From the circuit under test, we obtain its Energy Signature $S_{CUT} = \{n_{CUT1}, n_{CUT2}, ...n_{CUTk}\}$ by applying sequentially the input vectors as in the "golden" CUT until k numbers are obtained.

c) From the previous signatures, we compute a *distance* between the golden signature and the CUT's signature. This distance is computed as follows.

Let:

$$N_{CUTi} = \sum_{j=1}^{i} n_{CUTj} \quad \text{and} \quad N_{Gi} = \sum_{j=1}^{i} n_{Gj} \qquad (3)$$

then, the distance is defined as:

$$D = \sum_{i=1}^{k} |N_{CUTi} - N_{Gi}| \qquad (4)$$

d) If $D \geq D_{TH}$, where D_{TH} is a threshold, then the CUT is "bad".

The use of distance D is explained in the following paragraphs.

In Figure 1, we have shown the evolution of the energy consumption of a circuit as a function of the number of vectors applied. However, it is possible to construct the inverse function that gives the number of vectors necessary to consume a given amount of energy. A picture of such function for the "golden" circuit and a defective CUT is shown in Figure 3.

It is easy to prove that the shadowed area in the Figure measures distance D.

We have found that the use of distance D defined by (4) gives good results to discriminate between "-good" and "bad" circuits if D_{TH} takes into account the variations in the energy consumed by the defect-free circuits due to their fabrication process and the unavoidable noise in the measurements. This problem is considered in the following section.

3. Experimental results

In order to prove the feasibility of the Energy Signature test, an exploratory experiment was performed on a set of circuits.

Three types of circuits were experimented. The first type included five commercial MSI circuits of the 74hc series, the second type was an in-house full custom design and the third type was a standard, commercially available microcontroller. The defects introduced were resistive bridges connected between a circuit pin and the ground. As the Energy Signature test is able to capture changes in the static consumption as well as changes in the dynamic one, the increase in the quiescent current as well as the changes in the dynamic current due to the bridges were detected.

In all experiments, the maximum voltage at the virtual ground node was limited to $V_\alpha = 200$ mV.

3.1. Experiment with commercially available MSI circuits

Five standard 74hc circuits were tested. The defect introduced in all circuits was a resistor of 4.11 MΩ connected between an output pin and the ground. Each time the output pin became high, an I_{DDQ} current equal to 1.1 μA was generated. The vector rate was 16 KHz and the fraction of the period the bridge was excited ranged from 0.42 % to 47.8 % depending on the circuit. Capacitor C was selected in the range from 3.6 nF to 14 nF. A number of random input vectors was applied to obtain Energy Signatures with $k = 50$ for both defect-free and defective circuits.

Many applications of the vector set were performed on the defect-free circuits to obtain a reference value for parameter D (expression (4)). The value found for D is shown in Table 1 for both defect-free and defective circuits.

Taking as discriminability parameter $\eta = \frac{D_{defective}}{D_{defect-free}}$, we can see that the defects are all detected because η is equal to 31, ∞, 148, 3 and 13 for circuit C1, C2, C3 C4 and C5 respectively. As can be seen, η is large enough to clearly distinguish the defective from the defect-free circuits.

	Defect-free circuits				
	C1	**C2**	**C3**	**C4**	**C5**
D	92	0	13	521	115
	Defective circuits				
	C1	**C2**	**C3**	**C4**	**C5**
D	2844	927	1925	1563	1503

Table 1. **Value of D for defective and defect-free circuits. C1 is 74hc688, C2 is 74hc00, C3 is 74hc244, C4 is 74hc161 and C5 is 74hc373**

	Circuit m33 defect-free sample #					
	1	**2**	**3**	**4**	**5**	**6**
D	0	5176	6969	11035	3791	3930
	m33 defective sample #					
	1	**2**	**3**	**4**	**5**	**6**
D	55337	54517	57212	73033	61077	62203

Table 2. **Value of D for the circuit m33 taking sample 1 of the defect-free circuits as the "golden" circuit.**

3.2. Experiment with a full custom circuit

Six samples of a 3×3 bits multiplier circuit (**m33**) were tested. The defect introduced in all defective circuits was a resistor of 10.1 MΩ connected between an output pin and the ground. Each time the output pin became high (one input vector out of four, as average), an I_{DDQ} current of approximately 0.5 μA was generated. The vector rate was of 4 KHz. The value of capacitor C was 7.7 nF.

A number of random input vectors was applied to obtain Energy Signatures with $k = 256$ for both defect-free and defective circuits.

According to the expression (4), the value found for D is shown in Table 2 taking the first sample of the defect-free circuits as the "golden".

In this case the average discriminability parameter $\overline{\eta} = \frac{\overline{D}_{defective}}{\overline{D}_{defect-free}}$ is equal to 65.7. As can be seen, $\overline{\eta}$ is large enough to clearly distinguish the defective from the defect-free circuits.

3.3. Experiment with a commercial microcontroller

The last type of circuit tested was a commercial microcontroller, the NEC 78K0 [8], working at 10 MHz. Two experiments were performed. In the first, the program stored in the microcontroller was an infinite loop.

	Defect #		
	1	**2**	**3**
I_{DDQ}	89 μA	89 μA	1.07 mA
% time	4.3	95.7	4.3
	4	**5**	**6**
I_{DDQ}	6.25 mA	15 μA	227 μA
% time	4.3	4.3	4.3

Table 3. **Value of I_{DDQ} and percentage of time that each bridge in the NEC78K0 was excited.**

	Defect-free sample		
D	17051		
	Defect #		
Defect	**1**	**2**	**3**
D	57087	770994	439656
Defect	**4**	**5**	**6**
D	1178024	11135	114022

Table 4. **Value of D for the defect-free NEC78K0 and for the six defects.**

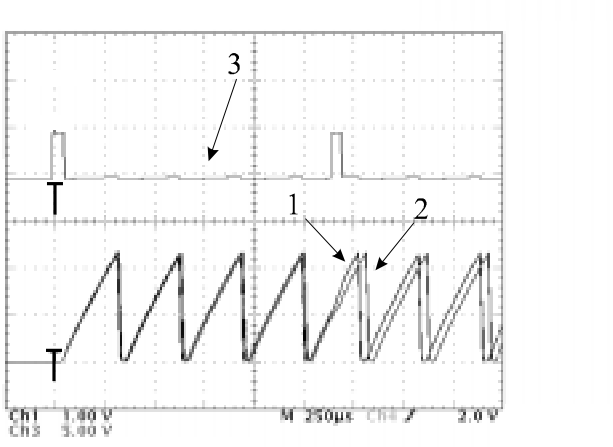

Figure 4. **Waveforms in the NEC 78K0. Signal 1 is the voltage at the ground pin of the defective circuit (amplified 12 times). Signal 2 is the same voltage in the defect-free circuit. Signal 3 is the voltage at the output pin with a resistive bridge connected to ground.**

The starting point was synchronized by means of the RESET pin and the test finished when a given number of "quanta" of energy was consumed by the microcontroller. To introduce a defect, resistors of different values were connected to bridge an output pin of the microcontroller and the ground. Each time the pin became high, a given amount of energy was wasted in the resistor. Table 3 shows the quiescent current generated by each bridge and the percentage of the loop period the bridge was excited.

The effect of the bridge on the circuit consumption can be seen in Figure 4. There, waveform 3 shows the voltage at the output pin, and waveforms 1 and 2 show the change in the voltage of capacitor C (amplified 12 times) for a microcontroller with and without the bridge, respectively. The waveforms are synchronized and superimposed in order to show the time needed by each circuit to consume E_Q . The test started at the point labeled T in the figure. The slope of waveform 1 increased each time the output pin became high, thus making the time needed by the circuit with the bridge to consume E_Q decrease.

The results on applying expression (4) for $k = 256$ are shown in Table 4 for the defect-free circuit and for the six defects.

For the defect-free circuit, the "golden" reference was obtained by repeating the test several times and averaging the calculated D (expression (4)).

As can be seen, all the defects except number 5 are easily detected because the discriminability parameter $\eta > 3$ in all cases except number 5. The non detectability of defect number 5 is due to the small amount of I_{DDQ} current generated by this bridge and the short time the bridge is excited (the output pin was high only for 60 μs, over a loop period of 1.45 ms).

The second experiment was performed to emphasize the detection of changes in the dynamic consumption due to a defect. Here, the program stored in the microcontroller executed two alternative loops, depending on the state of an input pin. One loop had high dynamic consumption, and the other one was less consuming. The state of the input pin was controlled to switch the microcontroller between both loops so that the time spent in the execution of each loop was the same. By introducing a resistive bridge in the input pin, the behavior (that is, the power consumption) of the microcontroller was modified because, due to the bridge, the only loop executed was the less consuming. Thus, the bridge modifies the power consumption *decreasing it*, in this case.

The results on applying expression (4) for $k = 256$ are shown in Table 5 for the defect-free microcontroller and for the defective one. In this second experiment $\eta = \frac{D_{defective}}{D_{defect-free}} = 659$, which means that the defect is clearly detected.

	Defect-free circuit
D	7220
	Defective circuit
D	4762744

Table 5. **Value of D for the defect-free NEC78K0 (average of three samples) and for the defective one (second experiment).**

4. Conclusions

A large class of defects may change the quiescent and/or the dynamic current of CMOS circuits. As a consequence, the energy consumption is expected to reflect these changes. Consequently, a test methodology based on the energy consumption measurement may combine the "best of both worlds" from the I_{DDQ} and i_{DDt} testing.

The energy chronogram can be used as a circuit Energy Signature and this signature may be used to discriminate between defective and defect-free circuits.

An exploratory work on a method to obtain the energy signature of a circuit by recording the number of input vectors needed by the circuit to consume a known "quantum" of energy is proposed. The set of such integers constitutes the Energy Signature.

The distance between the Energy Signature of the "golden" circuit and the CUT proposed has proven to be useful to discriminate between "good" and "bad" experimental circuits with artificially introduced defects. Moreover, the robustness of the Energy Signature Testing in front of variations of the energy consumed by defect-free circuits due to their fabrication process may be reinforced by using a normalized form of the signature. We are currently working on this normalized metric.

Exploratory experiments on several samples of defective circuits show that the Energy Signature method may become useful as a combined I_{DDQ} / i_{DDt} test method of such circuits containing defects which cause very small changes in the power supply current (below 1 μA in some cases).

Energy Testing can be performed at a faster rate than single vector application schemes like I_{DDQ} or i_{DDt}. In fact, the microcontroller experiment was performed while the microcontroller was working at nominal operational speed.

5. Acknowledgements

This work has been partially supported by the CICYT - Project No. TIC98-0478, by CIRIT Ref. 1997SGR00002 and by the ESPRIT WG-21898 Project POSEIDON.

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