On-chip Transient Current Monitor for Testing of Low-Voltage CMOS IC

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Abstract

In this paper, on-chip test circuitry performing the transient supply current measurement is presented. The introduced principle makes uses of the parasitic resistance of the supply connection to sense the dynamic supply current. Thus, the monitor does not cause any additional power supply voltage degradation and provides detection capabilities for open defects that usually cause a significant reduction of the I_{DDT} current. The proposed monitor does not affect the performance of the CUT and can be efficiently used to test low-voltage CMOS circuits. Significant results summarising possibilities and limitations of the circuit are discussed as well. The design has been implemented together with an experimental CMOS circuit using Alcatel-Mietec 0.7µm CMOS technology and its processing is in progress. Evaluation results of the prototype test chips will be presented at the conference.

1 Introduction

In recent years, it has been shown that some physical defects, which do not affect the logic behaviour of a CMOS circuit usually cannot be detected using voltage oriented test techniques. However, they often apparently reduce the reliability of the circuit. No doubt that testing is best performed using a combination of test techniques, with each method dedicated to detect a class of defects. Quiescent power supply current monitoring (I_{DDQ} testing) has been successfully used to detect a variety of such defects [1]-[4]. Nevertheless, the efficiency of I_{DDQ} in detecting open defects presents some limitations due to the fact that these failures may prevent changes of the quiescent power supply current [5]-[6]. Therefore, the transient power supply current testing (I_{DDT} testing) [7]-[8] can be conveniently used to augment the existing test methods and to enhance the defect coverage. On the other hand, the on-chip measurement of the dynamic current presents a more complex issue than performing I_{DDQ} testing. So far, only a few transient built-in current (BIC) monitors have been proposed [7], [9]-[12].

In this paper, the development of a new transient on-chip current monitor is presented. The proposed approach takes advantage of the quite small parasitic resistance of the metallic interconnection, between the core of the circuit under test (CUT) and its VDD pad, that is used as a sensing device. Hence the monitor does not influence the operation of the CUT, even when measuring high transient currents. The sensor quantifies the current peaks in a wide measurement range, from several µA to 100mA. Additionally a test rate of 1MHz can be achieved. The monitor is designed for transient supply current measurements of low voltage 3.3V CMOS circuits. The technology selected is the Alcatel-Mietec 0.7µm n-well CMOS. The transient BIC monitor is incorporated into an experimental digital design to prove its expected feasibility.

2 Design of the transient monitor

It is known that the current consumption of CMOS digital circuits exhibits sharp transient current peaks that appear during switching actions of the circuit. If an open defect is present, the transient current peaks of the defective circuit will differ from these of a defect-free one. To detect variations in the transient supply current peaks, the measurement of the charge involved is performed. The basic idea used for the proposed on-chip transient monitor is based on a consideration that, in most cases, it is sufficient to check the circuit for presence or absence of the current peaks (related to a reference value) rather than to characterise and to compare the shape of the current pulses.

The developed monitor takes advantage of the metal layer's parasitic resistance. It is known that the metal interconnections between the core of a design and its I/O pads always induce a small parasitic resistance [6]. This small resistance (assumed around 1Ω) can be used to sense the very high transient supply currents, typically drawn by the CUT during its switching actions. The principal scheme of the circuit providing this idea is depicted in Figure 1.

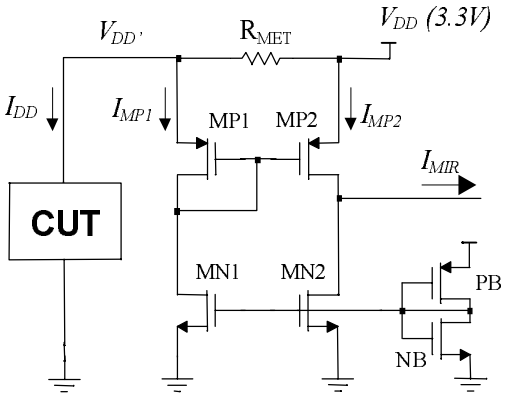

Figure 1 Current mirror principle of I_{DD} monitoring

The dynamic supply current I_{DD} flowing through the CUT always provides a small voltage drop across the parasitic resistance R_{MET}. This voltage difference makes the current mirror (MP1, MP2) unbalanced that implies a current I_{MIR} at its output. This current can be expressed as follows:

$$I_{MIR} = I_{offset}\left(1+\frac{I_{DD}}{I_{MP1}}\right)$$

where I_{offset} is the output offset current; I_{offset}/I_{MP1} is the current gain and I_{MP1} is DC current the transistor MP1.

The developed dynamic monitor using the current mirror principle consists of two main parts: an unbalanced current mirror that mirrors the transient supply current, and circuitry providing the quantification of the charge involved in the supply current. This circuitry consists of a diode (D), a switch (M_S), a capacitor (C_{charge}), and a differential amplifier (A). The general scheme of the whole transient current monitor is shown in Figure 2.

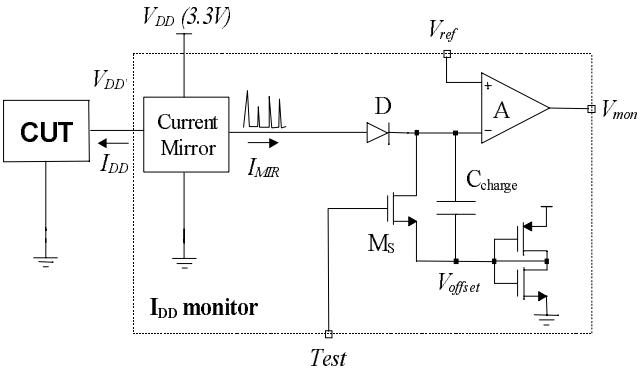

Figure 2 The proposed transient current monitor

The high transient peaks of the mirrored supply current I_{MIR} pass through the diode D and charge the capacitor C_{charge}. Initially, in monitoring mode, the transistor M_s is switched off so that the capacitor C_{charge} is fully charged by the transient supply current and the resulting voltage is compared to the voltage reference V_{ref} by the amplifier. Then the switch is closed to discharge the capacitor C_{charge} and to ensure that before each transition the amplifier input is set to zero.

The capacitance of C_{charge} is one of the essential parameters of the design as its value determines the voltage drop across it. Additionally, the reference voltage is another important parameter that should be tuned in function of the CUT being tested. These two parameters have to be set according to the transient current behaviour of the particular circuit when no defects are present. In a defect-free circuit, the minimum voltage across the capacitor C_{charge} will be:

$$V_{C\min} = \frac{Q_{DEF-FREE\min}}{C_{charge}}$$

where $Q_{DEF\text{-}FREE\ min}$ is the minimum charge driven during a transition in a defect-free circuit. The value V_{Cmin} represents the pass/fail level for the reference voltage V_{ref}

The offset in the output current I_{MIR} requires the capacitor C_{charge} and the switch M_S to be connected to a voltage reference not to provide current flowing through the diode in the quiescent state of the CUT. This voltage, denoted as V_{offset}, is given as follows:

$$V_{offset} = V_{out\_q} - V_{TD}$$

where V_{out_q} is output voltage of the current mirror (MP1,

MP2) in the quiescent state of the CUT and V_{TD} is the threshold voltage of the diode D.

3 Simulation results

The proposed monitor was simulated using HSPICE. A simple CMOS circuit composed of NOR gates loaded with ten inverters, was used as the CUT. Due to the very small resistance of metall layer, the proposed monitor is able to measure very high transient currents without affecting the CUT's performance. For the assumed R_{MET} value of 1Ω, the CUT supply voltage is lowered to 3.2V maximally for I_{DD} currents up to 100mA. The performance of the monitor for nominal parameters, room temperature and the C_{charge} value of 0.5nF is shown in Figure 3.

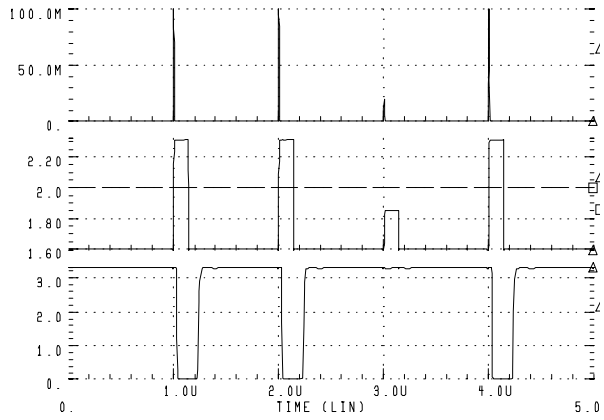

Figure 3 Performance of the monitor

The waveforms from the top to the bottom are: the dynamic supply current I_{DD}, the comparator inputs V_{in-} and V_{ref}, and the output voltage of the monitor V_{mon}. At 3µs an open defect is sensed (the V_{in-} voltage is lowered due to lower or missing transient current peak) and the monitor output V_{mon} remains at 3.3V.

Simulation results show that the most important design parameter affecting the monitor performance significantly is the sensing resistor R_{MET} as its particular value determines the 'operating' current range for which the monitor gives accurate current monitoring. In other words, the sensing resistor determines the level of the mirrored current charging the capacitor C_{charge} that leads to a respective voltage at the input of the differential amplifier. Table 1 demonstrates the accurate operating current ranges determined by the respective R_{MET} values and current mirror sizes. That means that the value of R_{MET} resistance has to be set according to the particular current range being measured.

If R_{MET} value is smaller than 0.5Ω the mirrored current I_{MIR} is too small to charge the capacitor C_{charge} (of reasonable value) in terms of a sufficient voltage drop at the comparator input. However, the considered range of R_{MET} shown in Table 1 is satisfactory from both the measurable transient current as well as from the power supply degradation points of view.

Table 1

R_{MET} [Ω]	$W/L_{(MP1,MP2)}$ [µm]	Working range (I_{DDT})
0.5	240/2	30mA÷100mA
1	240/2	10mA÷50mA
2	360/2	1mA÷10mA
3	240/2	500µA÷5mA

Although, the diode D affects the linearity of the current monitor, the current measurement in a respective operating range is quite linear as depicted in Figure 4.

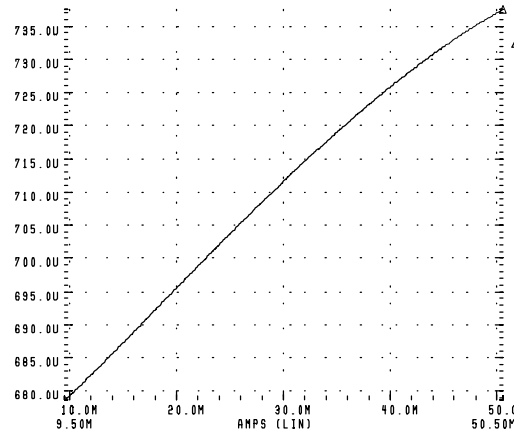

Figure 4 Linearity of the current mirror for R_{MET} of 1Ω and I_{DD} range from 10mA to 50mA

Although, the presented BIC monitor was originally supposed to be used for I_{DDT} testing of digital circuits, the results achieved also indicate the possibility to use it, if modified in a proper way, for analog test applications. If the CUT is an analog circuit then the supply current consumption is usually not negligible and an on-chip current monitor should handle high currents. Since most of the known monitors invoke unacceptable performance degradation due to significant voltage drop across the monitor they are generally impractical for real applications. The principle, proposed in this paper, does not create an additional voltage drop across the monitor, than the one already caused by the parasitic resistance of the supply connection, even for very high supply currents. Thus, slightly modifying the BIC monitor offers a wide range of possibilities to dynamic testing of mixed-signal circuits.

4 The layout implementation

Finally, the monitor circuit was implemented using the Alcatel-Mietec 0.7µm CMOS technology. The layout was designed using the Cadence design tool. The core of the monitor layout is shown in Figure 5.

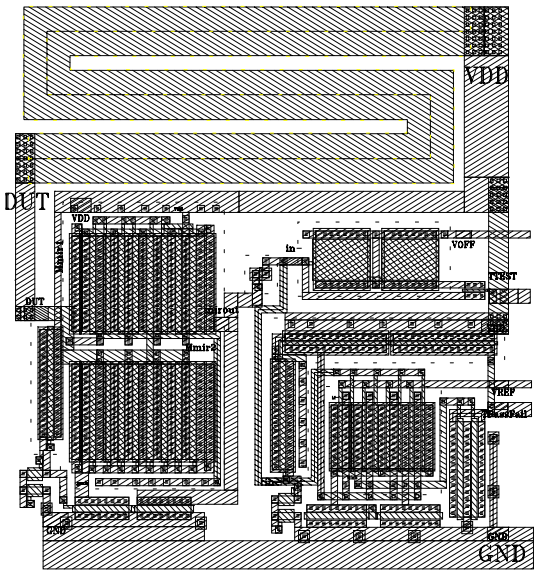

Figure 5 The core of the transient BIC monitor layout

For the prototype chip series of the monitor, a 1Ω R_{MET} resistor is implemented using Metal2 layer, implying an area overhead of 160µm x 55µm. Consequently, the total area of the transient BIC monitor is 170µm x 170µm. However, in a practical application, the parasitic resistance of the CUT, power supply line is used to implement R_{MET} and the total area overhead will be reduced or can even become neglectable if the monitor is placed under the supply routing.

5 Experimental usage

In order to verify feasibility and performance of the proposed circuit, the presented transient current monitor as well as a quiescent BIC monitor, developed previously under the same Copernicus project and published in [13], were implemented together with an experimental digital design (a two parallel 8-bit inputs multiplier) on a single chip. The layout of the whole experimental chip is depicted in Figure 6. The chip area of the digital circuit itself is 850µm x 850µm. In this implementation, the parasitic resistance of the power supply line of the CUT is used to sense the transient supply current. Therefore, the silicon area of the proposed monitor is reduced. The area of the transient monitor, placed under the circuit's power supply routing, is quite negligible 170µm x 140µm regarding the total chip area that is rather huge because of total number of I/O pads.

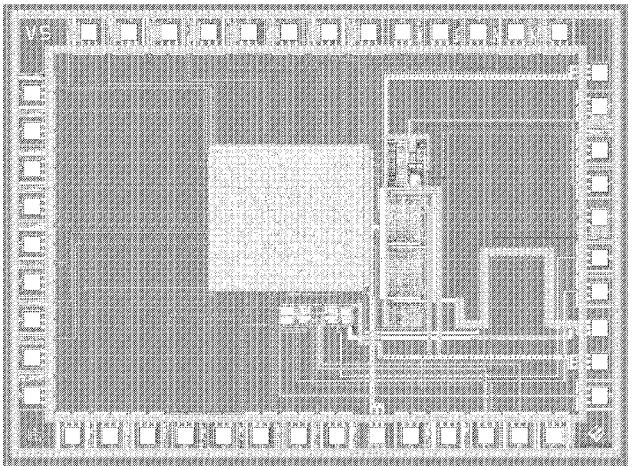

Figure 6 Layout of the experimental design

6 Conclusion

A new transient on-chip current monitor that tests the CUT for the presence or the absence of the certain transient supply current peaks is presented. By using the parasitic resistance of the metal connection as a sensing element, the proposed transient monitor does not cause an additional undesired supply voltage degradation and it is able to measure transient currents up to 100mA without affecting the performance of the CUT. A maximum test rate of 1MHz can be achieved. The proposed circuit is implemented in Alcatel-Mietec 0.7µm CMOS technology and is being fabricated together with an experimental digital circuit. Evaluation results will be available for the presentation at the conference. Moreover, the achieved results indicate the possibility to use the monitor also in analog and mixed-signal testing.

Acknowledgement

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