

Scaling Deeper to Submicron: On-Line Testing to the Rescue

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Progress in technological scaling allows the integration into a single chip of hundreds of millions of transistors, moving quickly to the multi-billion transistor capacities. The integration of complex systems into a single chip, that may include heterogeneous parts such as logic, SRAM, DRAM non-volatile memories, analog and even micromechanical and optical parts, is becoming a reality. Achieving acceptable quality and reliability levels for these complex products is one of the most critical issues that need to be faced. Testability is therefore a key factor that could limit these trends if not addressed adequately. At these levels of complexity external testing is becoming unfeasible due to ATPG limitations (reduced controllability/observability due to rapidly increasing #devices/pin and sequential depth). At the same time, the scan approach is losing interest due to the increasing length of scan chains (and thus test length), and low test application speed. At-speed test is a major limitation at a context where increasing clock frequencies (moving quickly to the multi-GHz domain), are making timing faults predominant. Automatic Test Equipment (ATE) is another important limitation, since, although its very high cost, it does not offer the memory capacities/depth and test application speed, required for testing nowadays ICs (development and production cycles are constraining ATE to use two-generations old IC technologies). In addition, several testers must be used to cope with the heterogeneous parts integrated into a single chip, increasing the test cost drastically. Under these constraints, the only realistic issue is to extend the BIST practice beyond memory testing. This requires new developments on logic BIST for increasing fault coverage while containing hardware cost, and extension of BIST approaches to other domains such as micromechanical. Furthermore, increased density and device size reduction, increased speed, low power requirements (i.e. reduced supply voltage), are reducing noise margins and component reliability, increase the impact and complicate the behavior of defects that in the past could be represented by simple fault models. Therefore, new developments on fault modeling, fault simulation, and ATPG tools are

needed to encounter for timing faults, cross talk, ground bounce and other spurious faults. These developments should be oriented towards a BIST approach. In addition, as circuit complexity increases, and faults with more complex behavior than stuck-at are gaining importance, the BIST hardware must be extended to enhance debugging who is becoming increasingly complex. Furthermore, as higher circuit complexity and lower reliability levels of devices will affect yield adversely, Built-In Self-Repair mechanisms will be required (starting from large DRAMs and moving to other parts as technological scaling is progressing).

The above challenges have to be faced by extending the traditional fault modeling, fault simulation, ATPG, scan path, and BIST approaches. However, these solutions are not enough for guarantying a reasonable level of reliability. The increased operation speeds and noise margins reduction that accompany the technological scaling, are reducing continuously the reliability of deep submicron ICs face to the various internal sources of noise. This process is now approaching a point where it will be unfeasible to produce ICs that are free from these effects. A more significant problem is related to the single-event upsets (SEUs). In particular, SEUs induced by cosmic radiation such as neutrons, will become a cause of unacceptable error rates in nanometer technologies. In the past this problem, was a concern in hostile environments like space. But nanometer ICs are becoming so sensitive that even sea level radiation will induce unacceptable rates of soft errors. Also, while in the past protection against SEUs was limited to memory parts only, even in space, under the new conditions logic parts should also be protected as they may become even more sensitive than memories. Thus, soft-error tolerant design is becoming mandatory, even for commodity applications. But economic constraints of such applications exclude the use of traditional, high-cost fault tolerant techniques. The only viable solution is to modify the design practice and CAD tools in order to generate ICs robust to soft-error.