A single-package solution for wireless transceivers

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Abstract

Although a single-chip solution seems to be ultimate goal for the design of wireless transceivers, there are many reasons to believe that this approach is not feasible for high-performance applications. Especially the RF front-ends of these transceivers require components that are difficult to combine into one single chip. As an alternative we propose a single-package solution that contains different components that are interconnected with a multi-chip module (MCM) interconnect technology. By implementing passive front-end components directly into this interconnect technology, instead of using external commercial components, a cost-effective realization of the front-end can be obtained with a higher performance or a lower power consumption.

1. Introduction

For future wireless communication systems we see an important trend towards more flexible and wideband applications (multimedia) and towards higher carrier frequencies. A good example of these trends is the upcoming standards for high-bandwidth wireless local area networks (WLAN) in the 5-6 GHz band. Designing analog front-ends for these future wireless applications is quite challenging. Next to the high operating frequency, critical aspects are the wide bandwidth, large dynamic range and (especially for multicarrier systems) a good linearity. For wireless/portable applications low power consumption as well as a high level of integration to reduce size and weight are of course also essential. In the next section the prospects and limitations of a single-chip approach are discussed. In Section 3 we present a single-package approach with a thin-film MCM interconnection technology (MCM-D). This technology offers many possibilities for the realization of passive components, either realized in the available interconnect layers, or with micromachining. Section 4 illustrates how active and passive components can be co-designed in order to obtain RF blocks with a high performance or a low power consumption.

2. Single-chip integrated telecom systems?

Traditionally radio front-ends have been based on the superheterodyne architecture that makes use of one or more intermediate frequencies (IF) with image-reject bandpass filters on every IF. On the lowest IF frequency typically a high-Q analog bandpass filter is required for channel selection. The superheterodyne transceiver has a good performance but it is not suited for a high level of integration, mainly because of the different high-Q analog bandpass filters, which are typically implemented as discrete LC, ceramic or SAW filters.

On the other hand, a high degree of integration is helpful to obtain high-performance systems with small sizes and weight, in conjunction with a low power consumption. At first sight, the "Holy Grail" for the realization of a telecom transceiver front-end is a single-chip solution that even combines the RF front-end with the DSP core of the transceiver. In the latter case, the most economical technology would be standard digital CMOS. During the last few years a lot of research has been focused on this single-chip CMOS route for RF transceivers. Several trends and developments have indeed led to more integrated transceivers:

Evolution of CMOS technologies allowing Si RF design - In the majority of today's RF front-end implementations most active components are realized in GaAs (e.g. LNA, power amplifier, mixer, antenna switch,…) [1] or silicon bipolar technologies (e.g. frequency synthesizer, mixer,…) [2-4] and very often as individually packaged components. In commercial products the use of CMOS technologies is limited to the IF and baseband sections.

In recent years a lot of research has been devoted towards single-chip CMOS transceivers [5-9].

But there are still several **problems** that could prevent single-chip integration of complete RF front-ends in the future:

- A number of front-end blocks are (and will most likely remain) impossible to integrate in CMOS, e.g. high-Q RF and IF bandpass filters or antenna switches.
- For some blocks there is an important performance penalty associated with standard digital CMOS compared to a GaAs or Si bipolar implementation. Depending on the application-specific requirements some of these blocks will have to be kept off-chip and implemented in GaAs, such as very low-noise LNAs (with NF around 1dB) and power amplifiers with output power of several Watts. Sometimes [4, 10] a power pre-amplifier is integrated on-chip, but the actual power amplifier (PA) is off-chip. Another problem that may prevent the integration of the PA is the interference of the very large signals at the output of the PA with the weak signals in the receiver front-end.
- The maximum allowable supply voltage decreases with CMOS technology scaling. As a result, analog front-end blocks realized in deep submicron digital CMOS technologies suffer from smaller dynamic ranges, which may not be allowable in future digital telecom applications.

Mixed-signal ICs - The rationale behind the research in CMOS RF design is the perspective of future single-chip integration of the RF front-end with the digital baseband processing circuits in deep submicron technologies.

Here are also several **problems** that could prevent single-chip integration of mixed analog (RF)-digital transceivers:

- In single-chip solutions of mixed-signal front-ends the signal-to-noise ratio of the analog blocks can degrade due to coupling between different functional blocks, especially the coupling via the substrate and the power lines from the digital parts to the analog blocks. This noise-coupling

problem becomes even worse in deep submicron technologies with supply voltage scaling, since this will reduce the analog dynamic range even further.

- Analog circuits and especially RF circuits typically have a lower yield than digital circuits due to inevitable parametric variations. Single-chip integration will therefore reduce the yield of the overall system.

On-chip inductors – In the last few years [11-12] there has been a trend in silicon RF design to use on-chip inductors. Integrating inductors would allow to eliminate a large part of the discrete passives used in many commercial RF front-end implementations.

Some *problems* associated with on-chip inductors are:

- The quality factor of on-chip inductors is very low compared to discrete inductors. Unloaded Q's of on-chip inductors are typically not higher than 5. By using several metal layers in parallel or by using thick metal layers, Q's of around 10 will probably be feasible in the frequency range of interest 5-6 GHz. By using even more advanced technological solutions (low-k dielectrics, Cu metallization) Q's of about 20 are predicted in future deep submicron CMOS processes, but this seems to be an upper limit in the frequency range of interest for standard CMOS technologies [12]. High inductor Q's are important in a number of RF blocks, because they are directly related to block performance and power consumption. For example, phase noise of a VCO is inversely proportional to the square of the Q of the LC tank [13] and directly proportional to the amplifier noise figure. The Q of the tank is limited by the component with the lowest Q, which is most often the inductor. Given that increasing the operating power can often reduce noise figure, we can say that power and inductor Q can be traded to achieve a given phase noise specification. High Q's are e.g. also important to obtain a low noise figure in LNAs.
- The area of inductors and of passive components in general in RF circuits is very large. For example, in the 2.4 GHz WLAN front-end described in [14], the passive components (mainly inductors) consume about 60% of the chip area. Since the cost per square millimeter of deep-submicron silicon processes is increasing rapidly with technology scaling and the size of inductors does not scale, the cost of these integrated inductors will become more and more important in fully integrated RF front-ends.

New architectures – Alternatives for the superheterodyne front-end architecture have been explored recently, to allow higher levels of front-end integration by eliminating high-Q discrete IF bandpass filters: zero-IF [10, 15], low-IF [5], wideband IF double conversion [7] architectures, ... These architectures have a number of features in common, e.g. the use of quadrature (up-) downconversion and channel selection filtering at (near-) baseband frequencies, which can be integrated in CMOS using analog or even digital signal processing.

Some *problems* related to these new architectures are:

- The signal-to-noise ratio (SNR) performance of these architectures based on quadrature conversion is lower than for the traditional superheterodyne architectures. The mirror signal suppression is limited by the imperfect quadrature generation at RF frequencies and mismatches in the in-phase (I) and quadrature (Q) signals to about 30-40 dB. However, for most digital telecom applications this limitation does not present a problem (e.g. in GSM a SNR of 10 dB is required) and very often the receiver SNR is limited by other effects, e.g. phase noise, distortion, adjacent-channel interference, etc.
- A discrete RF antenna bandpass filter in the receiver (a blocking filter) as well as in the transmitter (to limit out-of-band spurious emissions) are still required.

Some of the problems mentioned above could probably be solved (at least partially) by further (planned) developments in deep submicron CMOS technologies or by going to specialized, non-standard (expensive) technology options:

- Antenna switches could possibly be implemented in silicon by going to SOI technologies.
- Very high-performance, high-frequency RF blocks could be implemented in silicon by going to SiGe BiCMOS technologies.
- The voltage scaling problem can be alleviated by going to BiCMOS technologies, where the bipolar devices can typically stand higher supply voltages. Other solutions in CMOS technologies are: triple-well technology, low-V_T devices.
- The substrate coupling problem between analog and digital circuits could be alleviated by going to triple-well technology, deep trench isolation, SOI, SOS,…
- Using thicker metal layers, Cu metallization or low-k dielectrics can increase on-chip inductor Q's.

The above arguments indicate that a fully integrated single-chip transceiver in a digital deep submicron CMOS technology is probably not feasible in the foreseeable future. A single-chip solution in some expensive specialized (silicon) process could be more feasible but will it also make economical sense? These specialized processes are typically one or more generations behind standard digital CMOS. It is doubtful that these processes will be cost effective for single-chip integration, when large digital circuits have to be integrated - and especially when the lower yield of the overall system is taken into account.

Therefore, we will probably end up with (at least) two chips: the digital part (possibly also containing some low-frequency analog circuits and AD/DA converters) will be implemented on a separate chip in standard CMOS technology[1]. The question that remains then is: is a single-chip RF front-end feasible and/or cost effective? The likely answer is that even when we only consider the RF part, single-chip solutions are not feasible nor cost effective (for high-end applications such as WLAN in the 5-6 GHz band):

- Even with very advanced (but not too exotic) processes (e.g. BiCMOS with SiGe bipolar devices) not all RF functionality can be integrated. Antenna switches require insulating substrates. High-Q or even moderate-Q RF bandpass filters cannot be integrated for the same reason. For high output power combined with high operating frequency, the power amplifier will remain a difficult to integrate block in the future.
- Predicted maximum inductor Q's of 20 (with Cu metallization and low-k dielectrics) are not high enough to meet the demanding phase noise specifications of some digital telecom applications in a power-efficient way compared to off-chip inductors.
- Typically, the expensive chip area occupied by integrated passives (especially inductors) is larger than the chip area used by active devices. Moreover, the size of these passives will not scale with technology. They will scale however a little bit with increasing frequencies, but their size is still considerable in the 5-6 GHz band. Therefore it would make economical sense to try to remove these passives from the chip and implement them in a cheaper technology.

3. "Single-package" integration

An alternative implementation of integrated systems is the use of a thin film multichip module technology (MCM-D) [17-19] to interconnect multiple chips. With this technology

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[1] Even the cost effectiveness of large digital single-chip systems is doubted in some publications [16]. It may be more cost effective to partition the digital system in a number of chips and implement the interchip connections on a MCM substrate or interposer.

a number of RF components, each implemented in the most suitable IC technology, can be assembled in a relatively simple and economical way. Fig. 1 shows the architecture of the MCM-D technology developed at IMEC [17]. It consists of alternating layers of a dielectric with $\varepsilon_r = 2.7$ and copper conductors stacked on a high resistivity silicon, a borosilicate based glass or a low loss ceramic carrier substrate.
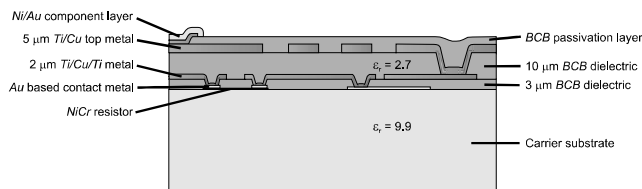

Fig. 1: MCM-D layer architecture developed at IMEC.

An essential aspect of this technology is that good-quality and relatively cheap passives (resistors, capacitors, inductors, filters) can be implemented directly in the MCM substrate. The use of these MCM passives leads to cheaper and more compact realizations than with discrete devices. It is also a cheaper and higher-quality alternative for on-chip passives. Inductors with values between 1 and 40 nH and Q's up to 50 (depending on inductance value) can be realized, as well as capacitors up to 1nF/mm^2 (Ta$_2$O$_5$).

When flip-chip technology is used for mounting the different devices on the MCM substrate, the advantages of MCM technology are even more obvious since flip-chip interconnections have much smaller parasitics than bonding wires.

The advantages of the use of MCM technology for system integration compared to more traditional technologies (PCB, LTCC,…) are:
- smaller dimensions and weight, especially with integrated passives and flip-chip mounting
- the use of thin film technology yields high precision components, very good manufacturability and repeatability of complex RF structures
- it is a maturing technology

There are also a number of advantages compared to a single-chip solution:
- Higher performance for RF functions that benefit from high-Q inductors.
- A clever partitioning of the system into its subsystems, each realized in the most suitable technology, will lead to lower cost, increase of manufacturing yield and optimal performance.
- There is no coupling between different components through the common substrate.
- Different supply voltage levels can easily be used.
- The MCM technology also opens a perspective for single-package mixed analog-digital integrated systems. It allows to have low-cost digital and high-performance analog in the same package, thereby retaining a high level of system integration as well as offering a good combination of cost, performance and functionality.

Two of the perhaps most important advantages of RF-MCMs have not been discussed yet:
- Next to the implementation of individual high-quality passives, the MCM technology can also be used to implement RF functions, such as RF bandpass filters, matching networks, baluns, power splitters/combiners, etc. or even antennas. Fig. 2 depicts an integrated 1 GHz MCM-D high-pass filter [17].
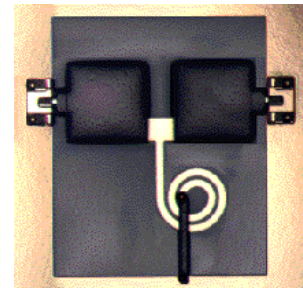

Fig. 2: photograph of an integrated 3rd-order high pass MCM filter with a size of 1.4mm by 1.7 mm.

- MCM technology provides the possibility to implement/integrate Micro Electro-Mechanical Systems (MEMS) which can yield cost-effective implementations of some RF functions. As a first example, Fig. 3 depicts the principle schematic of a micromechanical RF switch [20]: a suspended membrane can be moved under influence of an electrostastic force. Such switch has a better isolation compared to a GaAs switch. Further, this switch is extremely linear and it has a low insertion loss.
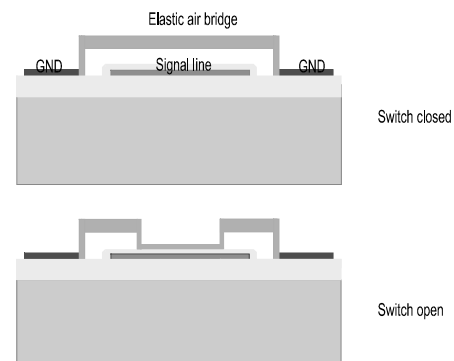

Fig. 3: cross-section of a micromechanical switch.

Figure 4 shows a photograph of the top view of the switch, and more particularly, the membrane and its surroundings.
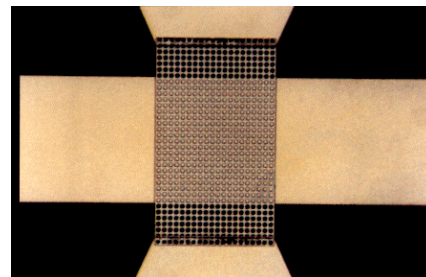

Fig.4: photograph of an RF switch (top view).

Another interesting component that can be fabricated with micromachining is a variable capacitor. In [21] such variable capacitor is described with a tuning range of 16% over a 5.5V range of applied bias, with capacitance values of about 2.2pF and a Q of 62 at 1GHz. This is a higher quality factor than can be obtained with on-chip varactors, which are realized as inversely biased diodes. The features and limitations of other MEMS components such as different types of high-Q resonators, are discussed in [20].

4. Chip-package co-design

Single-package integration of RF components on an MCM substrate is the subject of a lot of recent research and is finding its way into commercial products. In Fig.4 the functionality of the RF part of a Hiperlan radio developed by Mitel is schematically shown [22]. A photograph of the MCM module itself is shown in Fig.5. Its size is 13mm by 13mm.
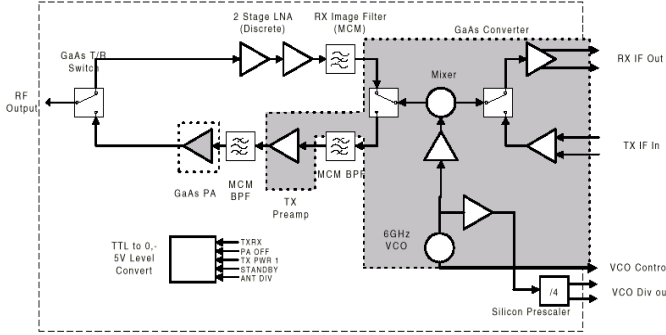

Fig 4: Block diagram of MITEL Hiperlan RF MCM.

The MCM module consists of GaAs MMICs, silicon chips, switches and MCM filters and transmission lines The chips were mounted with wire bonding.
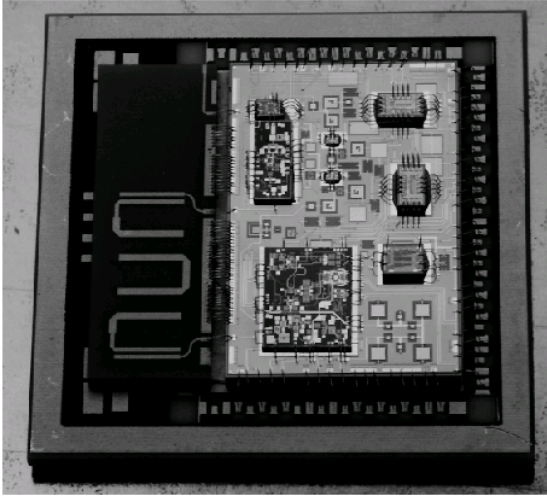

Fig 5: Photograph of the MITEL Hiperlan RF MCM.

The design of RF front-ends requires a good knowledge of the features and limitations of different IC technologies and of interconnection technologies. Hence, it is really essential to "co-design" the chips and the package.

With such co-design the design of the MCM-D passives can be tuned to the design of the active on-chip components. For example, the value of the characteristic impedances as well as the terminal impedances of bandpass filters could be chosen different from 50Ω if this leads to a higher performance of the active blocks.

MCM passive components or MEMS devices can also be used within the active front-end blocks, such as an inductor in a LNA or a varactor in a VCO. This results into extra bonding pads and solder bumps between the flip-chip mounted components and the MCM substrate. By a careful design of the bonding pads their parasitic capacitance can be reduced to an amount that the circuit performance in the 5-6 GHz band is not significantly degraded.

The trade-offs between on-chip and MCM implementation of passive components can be illustrated with the simulations on a 4.8 GHz VCO (see Fig. 6) in a 0.35μm BiCMOS technology.

For the inductors L1 and L2 both an on-chip and a MCM version are considered. The on-chip inductor has been modeled by a lumped π network [23], the elements of which have been determined with measurements. The MCM inductor is modeled by a lumped network as well as described in [17] Both the bonding pads and the flip-chip solder bumps have been modeled for this case.
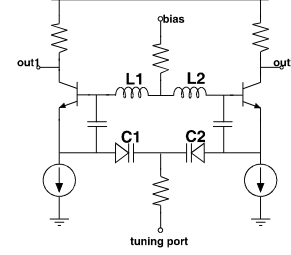

Fig. 6: A voltage-controlled oscillator [24].

The capacitors C1 and C2 are either modeled as an on-chip p+ to n-well diode with an estimated Q of 17, or as capacitor in series with a resistor such that the combination has a quality factor of 40. The second case, although it is a fixed capacitor, represents a high-quality capacitor with a Q that becomes comparable to that of a MEMS varactor. The simulated phase noise and the output power for several of these options are given in Table 2.

Inductor	Varactor	Phase noise (dBc/Hz @ 100kHz)	Output power (dBm)
On-chip (L=1.5nH, Q=5.5)	On-chip (Q≈17)	-86	-6.4
MCM (L=1.2nH,Q=30)	On-chip (Q≈17)	-92.5	-5
MCM (L=1.2nH, Q=30)	Capacitor with Q=40	-93.6	-3.4

Table 2: simulation results for the VCO of Fig. 7 with several options for the components of the LC tank.

The quality factor of the on-chip inductors is 5.5, whereas it is about 30 for an MCM-D inductor. By optimizing the layout of the latter inductor, a quality factor of 40 is possible. We see that the increase in performance between the version with the on-chip inductor and the version with the MCM inductor is significant. Further, the performance does not improve much anymore when quality of C1 and C2 is improved from 17 to 40. The reason is that the quality factor of the LC tank is limited again by the inductors. When the Q of the inductors would be increased to 40, then the change from 17 to 40 for the Q of the capacitor would give rise to a larger increase of the performance. The use of a MEMS varactor here would only make sense if such high Q can be obtained in conjunction with a large tuning range for the oscillation frequency, in the range of 20%.

Other examples of co-design of active on-chip components with off-chip passive MCM-D-type components have already been reported. For example, in [25] a VCO is presented with an MCM inductor. In this way, a low phase noise is obtained (-142dBc/Hz at 10MHz offset from a 1018 MHz center frequency), in conjunction with a high accuracy on the center frequency and a smaller volume than if a PCB mounted resonator would be used.

Also for RF blocks other than a VCO one can expect a performance improvement or a lower power consumption for the same performance.

For example, for a low-noise amplifier a figure of merit (FOM) can be defined as FOM=S_{21}/(NF x P_{dc}). Fig. 7 depicts a low-noise amplifier.
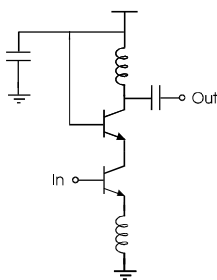

Fig. 7: a low-noise amplifier

In [12] this circuit has been designed for 5.8 GHz in a 0.5μm SiGe-BiCMOS process. If the quality factor of the inductors is increased from 4.5 (corresponding to an on-chip implementation) to 45 (which can be obtained with MCM inductors), then FOM increases with more than a factor two.

In order to come to an efficient single-package system design, however, some problems still need to be solved. For example, circuits that use off-chip passive components are more difficult to test than single-chip circuits. Another problem is the accurate simulation of on-chip components in conjunction with MCM components or MEMS. This would require a coupling of a circuit-level simulator (which is quite efficient in terms of CPU time) with a threedimensional solver for the Maxwell equations (with CPU times in the order of magnitude of days).

5. Conclusions

A single-package approach has been proposed for wireless transceivers. Such package contains different ASICs that are interconnected with an MCM-D technology. In this technology high-quality passive components and MEMS can be directly integrated. Several examples have shown a considerable increase in performance when some critical passive components of the RF front-ends are directly realized in the MCM substrate, rather than on chip. Conversely, a reduction of the power consumption can be obtained for the same performance.

The "single-package" integrated system design, proposed here as an alternative for single-chip integration, is not incompatible with the expected future improvement of CMOS. It is not a temporary solution that will become obsolete with predicted CMOS technology scaling. Instead, these single-package transceivers will only benefit from the evolution in RF CMOS design and the development of new front-end architectures: the resulting single-package solutions will only become more dense and cheaper. There will be fewer devices mounted on the MCM substrate, but the cost and performance gain by implementing the large passives in the MCM substrate instead of on-chip will remain. Moreover, a number of RF components will not be integrated on-chip, e.g. RF filters, antenna switch etc.

References
[1] TriQuint Semiconductor, http://www.triquint.com, e.g. TQ 9205 Transceiver.

[2] Harris Semiconductor, http://www.semi.harris.com/, e.g. HFA 3624 2.4 GHz Up/Down Converter.

[3] Maxim Integrated Products, http://www.maxim-ic.com, e.g. MAX 2402 800 MHz to 1000 MHz transmitter.

[4] LMX3161 Single chip radio transceiver, National Semiconductor, http://www.national.com

[5] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," IEEE J. Solid-State Circuits, Vol. 30, No. 12, December 1995, pp. 1483-1492.

[6] S. Wu, B. Razavi, "A 900 MHz / 1.8 GHz CMOS receiver for dual band applications," Proc. ISSCC 1998, pp. 24-25.[7] J. Rudell et al., "A 1.9 GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," IEEE J. Solid-State Circuits, Vol. 32, No. 12, December 1997, pp. 2071-2088.

[8] M. Steyaert et al., "A single-chip CMOS transceiver for DCS-1800 wireless communications," Proc. ISSCC 1998, pp. 48-49.

[9] F. Piazza et al., "A 0.25μm CMOS transceiver front-end for GSM," Proc. IEEE Custom Integrated Circuits Conference 1998, pp. 413-416.

[10] J. Sevenhans et al., "Silicon germanium and silicon bipolar RF circuits for 2.7V single chip radio transceiver integration," Proc. CICC 1998, pp. 409-412.

[11] N. Nguyen and R. Meyer, "Si IC-compatible inductors and LC passive filters," IEEE J. Solid-State Circuits, Vol. 25, No. 4, pp. 1028-1031, 1990.

[12] J. Burghartz et al., "RF circuit design aspects of spiral inductors on silicon," Proc. ISSCC 1998, pp. 246-247.

[13] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," Proceedings of the IEEE, Vol. 54, No. 2, p. 329, 1966.

[14] R. Meyer, W. Mack and J. Hageraats, "A 2.5-GHz BiCMOS transceiver for wireless LAN's," IEEE J. Solid-State Circuits, Vol. 32, No. 12, pp. 2097-2104, December 1997.

[15] S. Brett and G. Stanton, "A direct conversion L-band tuner for digital DBS," Proc. ISSCC 1998, pp. 126-127.

[16] E. Davidson et al., "Long Lossy Lines (L^3) and their impact upon large chip performance," IEEE Trans. Components, Packaging and Manufacturing Technology – Part B, Vol. 20, No. 4, November 1997, pp. 361-375.

[17] P. Pieters and E. Beyne, "Spiral inductors integrated in MCM-D technology using the design space concept," Proc. of the 1998 Int. Conf. On Multichip Modules and High Density Packaging, pp. 478-483.

[18] M. De Samber et al., "Low-complexity MCM-D technology with integrated passives for high frequency applications," Proc. of the 1998 Int. Conf. On Multichip Modules and High Density Packaging, pp. 285-290.

[19] R. Arnold et al., "MCM-D and direct module attach for RF applications," Proc. of the 1998 Int. Conf. On Multichip Modules and High Density Packaging, pp. 268-272.

[20] C. Nguyen et al., "Micromachined devices for wireless communications," Proceedings of the IEEE, Vol. 86, No. 8, pp. 1756-1768, August 1998.

[21] D. Young and B. Boser, "A micromachined variable capacitor for monolithic low-noise VCO's," Proc. 1996 Solid-State Sensor and Actuator Workshop, pp. 86-89.

[22] G. Arnold et al., "RF IC and MCM-D codesign for wireless communication systems," IEEE Int. Workshop on Chip-Package Codesign CPD '98, pp. 53-58.

[23] J. Long and M. Copeland, "The modeling, characterization and design of monolithic inductors for silicon RF IC's," IEEE J. Solid-State Circuits, Vol. 32, No. 3, March 1997, pp. 357-369.

[24] L. Dauphinee, M. Copeland and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated LC resonator," Proc. ISSCC 1997, pp. 390-391.

[25] P. Davis et al., "Silicon-on-silicon integration of a GSM transceiver with VCO resonator," Proc. ISSCC 1998, pp. 248-249.