Potentials of Chip-Package Co-Design for High-Speed Digital Applications

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Abstract

The inherent potentials of the Si technology are limited by the low interaction with packaging. Co-design as the symbiosis between the ICs and appropriate high-density packaging offers lower RC line delay, improved SSN and lower costs compared to single-chip approaches. The distribution of the system functionality between IC and the packaging level opens up new vistas in future electronic design and system architecture.

1. Roadmaps and co-design approach

The SIA roadmap for semiconductors [1] shows an undiminished performance increase of the inherent Si device technology over the next decade. But the overall system performance depends also on the packaging as the interconnect to the system environment. A low interaction between IC and packaging design will more and more limit the system potentials. The novel chip-package co-design approach with the objective of exploiting the synergism of ICs and packaging through their concurrent and matched design is clearly focused on system-level. For the challanges in high-speed digital design, clock delay, memory bandwidth, signal switching noise and cost/performance the co-design approach offers attractive solutions.

1.1 On-chip delay

The maximal clock speed is determined by the signal delay and clock skew. Signal delay is composed of the gates and the interconnect delay. Scaling of the MOS technology over the last two decades has continuously decreased the gate delay whereas the RC line delay is increasing because of the reduced line cross-section.

Up to now the gate delay has dominated the delay in high-speed digital circuits. Below the 130nm technology the on-chip interconnect delay becomes more and more dominant., even if using copper (Cu) as interconnect material instead of aluminum (Figure 1).

The package wiring layers provide about 1000 times less wire resistance and about 10 times less wire capacitance. Wiring of long interconnections like the global clock tree can benefit from the lower RC delay if interconnection is performed off-chip as depicted in Figure 2.

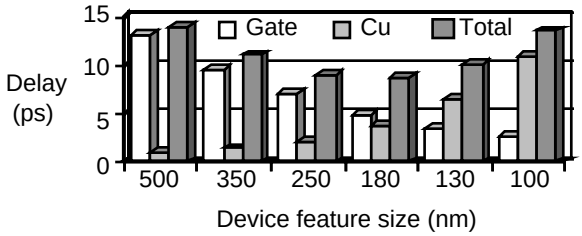

Figure 1. On-chip delay consisting of the intrinsic gate delay plus the interconnection delay

Zhu [2] reported about a clearly reduced clock skew and 10 percent power reduction. Obviously this off-chip routing opens the path to high clocked systems above 1 GHz; on the other hand, it requires a close interaction between IC and packaging design, because the functionality is distributed between the IC and the packaging level.

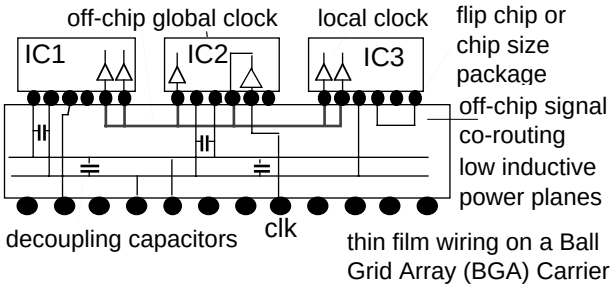

Figure 2. Future high-speed digital system integration with off-chip signal and clock co-routing on a high-density substrate

1.2 Memory bandwidth

The bottleneck in overall system performance of high-end computers is the bandwidth between the CPU and the memories. The gap between the processor and DRAM speed is growing by about 50 percent per year [3]. Hierarchically organized cache memories are normally used to bridge this performance gap. The co-design approach together with advanced interconnection technologies allow the direct access from the CPU core logic to physically separated memory banks with high

bandwidth [4]; e.g. 1000 I/Os covering 80mm^2 in 0.5µm CMOS enables 200GByte/s data rate so that also big memories are virtually embedded within the CPU. A packaging and interconnection scheme with flipchip and area I/O as depicted in Figure 2 is necessary to enable the high-density interconnect between the different ICs.

1.3 Signal Switching noise and signal integrity

The SIA roadmap predicts a power consumption growth in high-performance processors from 70W in 1997 to 160W in 2006, whereas the core voltage will decrease from 2.5V to 1.2V respectively which yield in a 5 times higher current density. If the expected current surge di/dt of about 500A/ns can not be ensured the speed of the circuit will be degraded. Only low-ohmic on-chip connections, off-chip low-inductance power planes and a carefully designed arrangement of on- and off-chip de-coupling capacitors can provide the necessary current stability. In high-speed processor modules more than thousand power lines and flipchip interconnections are necessary to provide a low inductive power line locally into each logic block.

1.4 Cost/Performance

The PC and server market is characterized by a 2 times yearly increase in the performance/cost ratio. A careful and concurrent optimization over the complete design chain includes the adaptation of the system architecture to an appropriate manufacturing technology. E.g. the costs are smaller to add a layer on the package than on the IC. Krusius et al proved in [5] that tiled silicon on a Multichip Module can be more cost effective than large ICs when the system can be effectively tiled without to much connectivity between the tiles. For ICs bigger than 300mm^2 the lead of tiled silicon solutions compared to system-on-a-chip can be estimated to about 3 to 4 years, then the reduced device feature size enables smaller ICs and therewith reduced costs.

2. Barriers and enabling technologies

The technical benefits in system design when incorporating co-design techniques have been explained. What are the barriers that could prevent the exploitation ? Firstly, there are structural and cultural differences between the IC and packaging world. IC design is clearly performance- and technology-driven with a high innovation rate, whereas the packaging is more cost- and system-driven. Secondly, system and module designers can exploit the added value of co-design. The crucial point is the possible benefit for IC manufactures should they have to adapt their products to specialized packaging with an increased dependence from the manufacturer. Alliances between the IC and packaging worlds become more and more unavoidable.

Several technologies have to be developed further on to offer the performance required for co-design, e.g. high-density substrats with lines pitches less than 30µm, integrated de-coupling capacitors, high-density interconnect with about 4000 interconnects/cm^2 [6], three-dimensional packaging technologies to shorten the signal lines and for high-speed communication also integrated optical interconnects. Co-design oriented CAD tools have to support the distributed functionality on the signal and clock level, in system partitioning [7], in thermics, and finally in the exploration of test, yield and costs [8].

3. Conclusion

The distribution of the system functionality between the IC and the packaging level offers various technical benefits. For high-speed digital applications. the main advantages are the reduced clock skew, power reduction, higher memory bandwidth, improved signal switching noise and finally an extended flexibility in system partitioning and in cost/performance optimization. Several research activities and international workshops [9,10] marked the beginning of this emerging technology as a new era in the multidisciplinary cooperation between the IC, packaging and CAD world.

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