A power estimation model for high-speed CMOS A/D Converters

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Abstract

Power estimation is important for system-level exploration and trade-off analysis of VLSI systems. A power estimator for high-speed analog to digital converters that exploits information from reported designs is presented. The estimator is an analytical expression which is independent of the actual topology used and can easily be updated with new published designs. Experimental results show a good predictor accuracy of better than a factor 2.2 for most designs.

1. Introduction

Decisions taken in the micro-electronics industry are often driven by the idea of cost reduction. The main solution to meet this reduction is the use of VLSI technology. This however means that making a design becomes a more and more complex task requiring more engineers to work on it and this would rather increase the cost. To counter this, the time-to-market for new designs has to go down reducing the total investment risk and the productivity of the designers has to increase. In order to master complexity and increase productivity designers have to use higher levels of abstraction.

With the emerging of mixed-mode designs however it became clear that high-level solutions for analog designs (levels higher than opamp level) where non-existent or not satisfactory. This leads to designs where typically the analog part only takes up 10 percent of the chip's functionality but much more percent of the design effort. In other words the analog part is a potential bottleneck in mixed-mode designs.

Another common problem encountered in mixed-mode design is that early in the design process the analog and digital parts have to be split up based on heuristics and experience. In this way global system optimization is impossible and the only way to handle growing complexity is by doing time consuming iterations. To tackle this problem two actions are needed. One is the development of (fast) mixed-mode simulation tools, a signal that is clearly intercepted by the CAD-tools industry (HP's ADS, Analogy's Saber, Cadence, Mentor,…). The second action is the development of high-level analog models and estimators to be used in system-level design tools. This however is a much more difficult task.

In this paper first an overview of possible approaches for the development of analog power estimators will be given in section 2. A power estimator is a function that returns an estimated value for the power consumed by a functional block when given some relevant specifications (section 3) as input. Next, in section 4, the top-down development of a power estimator for high speed CMOS analog to digital converters will be discussed and a solution presented. Finally the results will be discussed in section 5 and a conclusion is provided in section 6.

2. Approaches for analog power estimators

Basically two methods are available for developing analog building block models and estimators: the bottom-up method and the top-down method.

In the bottom-up method a certain topology is selected and then from this exactly known schematic, equations are derived. In this way the behavior of the analog block is modeled. The most obvious disadvantage of this approach is that first a topology has to be chosen. By doing this the generality is lost because other solutions are excluded. Including other topologies is to a certain practical extent possible but time consuming. The advantage is that the models and estimators are more exact and therefore are more accurate for real designs. Also within one topology several specifications can be traded-off quite accurately.

The top-down method is much more optimal for real system-level design. First of all no assumptions are made regarding the topology of the building block leaving all (and hopefully original) solutions open. Secondly the obtained equations are simpler and therefore better for implementation in fast system

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exploration tools. The drawback however is that the accuracy of the models is often difficult to achieve because of the typical nature of analog design where one transistor more or less can have a great impact on the behavior and specifications of the design. This also explains why it is more difficult to obtain a general, topology independent, model. The use of fitting parameters typically compensates this shortcoming towards different topological implementations of the same analog block. This approach still limits the use in system design because only discrete solutions can be used: every topology has its own fit values. The main differences and properties of the two approaches are summarized in figure 1.

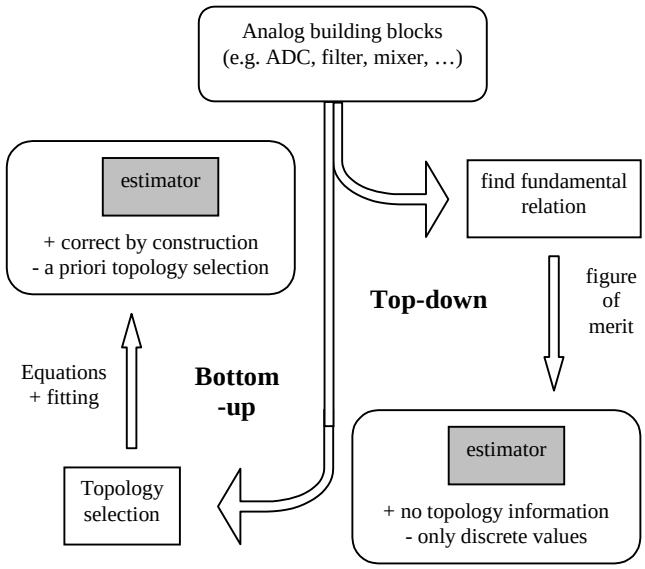

Figure 1: Short schematic overview of the top-down and bottom-up approach and their major properties

Next two examples are given that illustrate the two approaches. Both are taken from the field of high-speed ADC's.

The first one is taken from [1] and is an example of a bottom-up approach:

$$f_{\text{in, max}} = \frac{2 \cdot \text{BW}_{\text{fold}}}{\pi \cdot \text{F}_{\text{F}}} \qquad (1)$$

In equation (1), $f_{in,max}$, the maximum input signal frequency, is expressed as a function of the bandwidth of the folding preprocessing circuit and the folding factor F_F. It uses information specific to the used topology (F_F) to model the external specification $f_{in,max}$. It is clear that this equation is only valid for this exact topology and can only be used in system-level design tools if this restriction is not a problem. Likewise for this ADC one could derive a function expressing the power consumption as P=function(BW_{fold}, F_F, F_{sample}, Bits, F_{signal}, …) but this takes time and has to be repeated for every (even little bit) different topology or technology.

The second example taken from [2] is given in equation (2) and is an example of a top-down method:

$$\text{P}_{\text{ADC}} = \text{FOM} \cdot \text{DR} \cdot \text{SR} \cdot 10^{12} \qquad (2)$$

It expresses the power as a function of the dynamic range (defined as $DR=2^n$ with n the number of bits), the sampling rate (SR) and a figure of merit (FOM). The FOM of several ADC's are also given in [2]. The equation contains no information about the topology of the ADC, the only fit parameter used is the FOM. When a new ADC is published one can easily calculate the FOM. The estimator will always give discrete values and will in this way limit the effectiveness of the system-level design tool that uses it. No trend analysis is possible as interpolation between (completely) different designs is doubtful practice and probably leads to wrong results.

In this paper a meet in the middle solution is presented for high-speed CMOS ADC's. It is a top-down approach but without the use of specific fit parameters for every specific topology.

3. Design parameters of high-speed ADC's and their relevance for power estimators

When looking at an ADC, there are many parameters to be considered. Not only the speed and the accuracy are important but also parameters like power consumption, area, input capacitance, input swing, input signal frequency, etc. Depending on the application one is more important than another. When fabricated and measured ADC's are published however, a few parameters are always given. These are: sample frequency, number of bits, area, process (technology), power consumption, supply voltage, a measured graph with the effective number of bits as a function of the input frequency and the input swing.

In any of the two approaches given above for deriving models and estimators a choice has to be made on which parameters are included and which are unneeded or only of second order importance regarding the power consumption.

Before deriving the new power estimator an overview of the gathered data is given. All CMOS ADC's that were published in the IEEE Journal of Solid State Circuits from December 1994 up to now and all that were published in the proceedings of the ISSCC

conferences from 1996 to 1998 have been included in the data which gives a total of 23 designs (sigma-delta converters where not considered because of their completely different principle of operation). From every design the following parameters were selected: the sampling speed (F_S), the number of bits, the input signal frequency (F_{signal}), the effective number of bits (ENOB), the power consumption (P), the power supply (Vdd), the used technology characterised by the minimal channel length (L_{min}) and the silicon area. In most publications a measured graph showing the ENOB as a function of F_{signal} is included. Several points of these curves were taken per design in order to increase the number of data points. This can be defended by noticing that the announced number of bits usually are only met at low input signal frequencies and that real operation situations work with higher signal frequencies and are therefore relevant. By doing so, the number of data points is increased to 75. They are all shown in

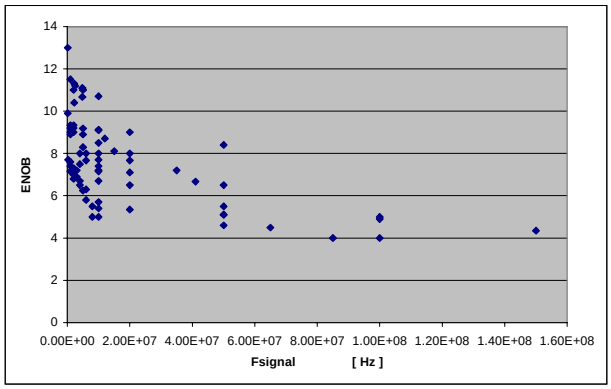

Fig. 2.

Figure 2: An overview of the obtained data points. The ENOB are given as a function of the input signal frequency

The power is not plotted on a third axis to keep the graph readable. It would just show that no simple correlation exists between the power consumption and the F_{signal} and ENOB. In the next section a general power estimation function will be derived.

4. Derivation of the power estimator function

The power is proportional to the supply voltage times a frequency and a charge:

$$P = Vdd \cdot I = Vdd \cdot f \cdot Charge \qquad (3)$$

This is quite trivial but the question is what frequency should be considered when talking about ADC's and then which charge is being transferred. A high speed ADC always has two parts: comparators and (pre)processing circuitry (the digital decoding logic is considered to behave as the comparators). The comparator is clocked at F_{sample} (and reset every clock-cycle) and the processing circuit varies at the frequency of the input signal. In pipelined ADC's also the Sample and Hold and the DAC are clocked at F_{sample} but the charges internally vary with the signal frequency amplitude. So it is better to split equation (3) up in two parts as well:

$$P = P_{comparators@Fsample} + P_{processing\ circuit@Fsignal} \qquad (4)$$

The charge is stored on internal capacitances so that for each part of the ADC equation (5) is valid:

$$P = Vdd \cdot freq \cdot (Voltage\ swing) \cdot C \qquad (5)$$

The voltage swing for the comparators is always the full supply voltage (digital values). For the rest of the circuitry the swing depends on the signal swing but if it is a good design it should be as large as possible and therefore for the sake of simplicity also Vdd is taken which results in an expression of the form of equation (6) for each part:

$$P = Vdd^2 \cdot C \cdot freq \qquad (6)$$

About the capacitances little can be said without going into topology details which has to be avoided to have a good top-down estimator. Therefore, the equality is replaced by a proportionality and the capacitance is taken proportional to the technology's minimal channel length which yields equation (7) for the total power estimator:

$$P \propto Vdd^2 \cdot L_{min} \cdot (F_{sample} + F_{signal}) \qquad (7)$$

However this is far from being a good power estimator because nothing has been said about the accuracy which of course is an important factor in ADC's. It is clear that through the size of the devices the accuracy is varied [3]. Using larger devices results in a higher accuracy but also increases the total capacitance thus limiting the speed and increasing the power consumption [4]. The accuracy is expressed as ENOB which is defined as shown in the well known [5] equation:

$$ENOB = \frac{20 \cdot \log(SNDR) - 1.76}{6.02} \qquad (8)$$

The accuracy (8) is related to the size of the devices and in this way to the power (7). This correlation has been investigated for the 75 data points as shown in figure 3 and results in the following regression relation:

$$\log\left(\frac{Vdd^2 \cdot L_{min} \cdot (F_{sample} + F_{signal})}{Power}\right) = -0.1525 \cdot ENOB + 4.8381 \qquad (9)$$

The correlation coefficient r is also given for this linear regression approximation in figure 3 and is 0.791. The mean square error equals 0.2405 and a 90% confidence band for the regression line is drawn.

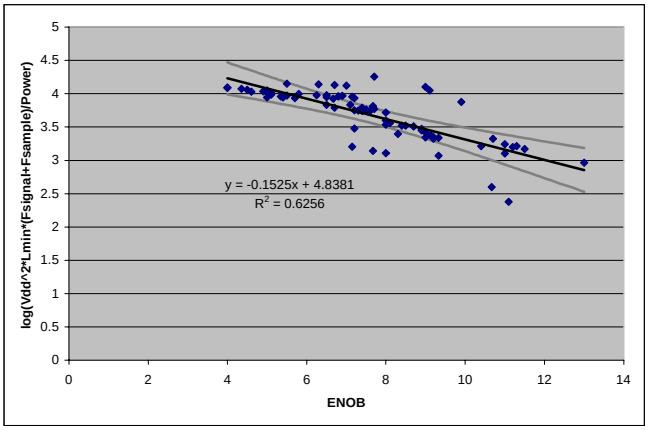

Figure 3: The result of the log of equation (7) divided by the power as a function of the ENOB, a linear trendline and its 90% confidence band.

From this trendline the final power estimator valid for all non-oversampling high-speed ADC's can be derived as:

$$P = \frac{Vdd^2 \cdot L_{min} \cdot \left(F_{sample} + F_{signal}\right)}{10^{\left(-0.1525 \cdot ENOB + 4.838\right)}} \qquad (10)$$

In the next section the results of this estimator function will be compared to the published results. This estimator combines the simplicity of the top-down approach with the flexibility of the bottom-up approach. It is indeed a continuous function, it is valid for many different ADC topologies and it can easily be extended towards other (or new) designs by adding the data and deriving a new trendline. Also, having a closed analytical function allows easy integration in a system-level design tool and makes it well suited for system exploration [10].

5. Results of the power estimator function

The estimated power can be compared to the published power based on absolute differences or on relative differences. Although when used in system design tools the absolute estimated power will be used, the validity of the estimator is better shown with the relative difference. Both are shown in figures 4 and **5** respectively.

The relative values are given in ascending order and the absolute values are put in that same sample order (figure 5).

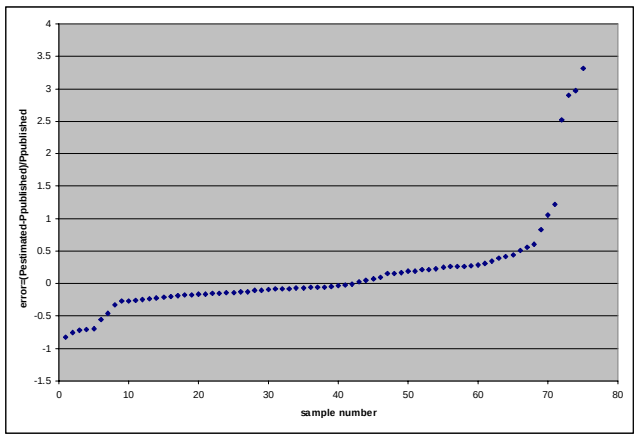

Figure 4: The relative error in ascending order

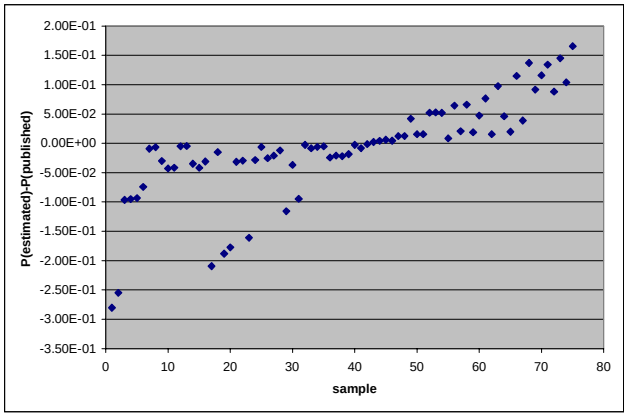

Figure 5: The estimated power consumption minus the published power consumption in the same sample-order as in figure 4

In figure 4 it can be seen that 85% of all the data points fall within a factor of 2.2 (samples 6 up to 71). A factor 2.2 is about 1.44 times the sigma calculated from the linear regression analysis. This result is accurate enough for a first order system-level design where a nominal value can be taken (the estimated value) and a certain margin on this value.

Samples that have a relative factor higher than one consume less power than estimated. When looking at figure 4, four points clearly consume much less power than estimated. These four data points are taken from 2 pipelined ADC's: [6] and [7]. In both designs special efforts have been made to reduce the power consumption. Both use dynamic comparators requiring more digital calculations next to the already present digital error correction in pipelined ADC's. This is a power consumption cost that is not included in the published numbers.

On the other hand samples that consume more power than estimated have a relative factor less than one. Again five samples tend to deviate more from the

estimated amount than the main group and these samples are taken from 2 different designs: [8] and [9]. In [8] an ADC is designed which is more immune to substrate noise. The ENOB published are measured while inducing substrate noise to the design. This means that special design tricks where used to keep a good performance and this can explain the higher than average power dissipation. In [9] the high power consumption can be explained by the presence of an extra pipeline stage needed for continuously calibrating the ADC. All the above shows that the "deviant" estimated values can be explained by the nature of the designs whereas the majority of the designs can be predicted with an accuracy better than a factor 2.2 (fig 4).

A possible comment that will always remain since it is related to the used data and therefore inherent to the method, is that the variance of the reported power dissipation of the set of samples is not known and thus not taken into account. Therefore, no absolute figure expressing the uncertainty of the estimator can be calculated. Only a relative figure, sigma, resulting from the regression fit was calculated to be 0.2405. Another way to prove the usefulness of the estimator is to take a design that was not used to derive the estimation function and to check the result or in other words by verification. A design that expresses the ENOB as a function of f_{sample} and f_{signal} is found in [11]. The estimated power consumption is calculated (10) to be 166mW and the published power consumption is 225mW or the relative error equals (166-225)/225=-0.26 which is about a factor 1.35 (well below the uncertainty margin of 2.2).

6. Conclusions

A power estimator for high-speed A/D converters has been presented. The estimator combines a top-down approach with the advantages of a bottom-up approach. This means that the estimator is simple and independent of the used topology (flash, pipelined, folding, interpolating) and that it can easily be updated when new designs are published. It also means that it is an analytical and continuous function allowing reliable system exploration during the system-level design phase. Time consuming iterations in the design can be avoided and an optimum regarding the system's power consumption can be achieved more closely. The estimator has an accuracy of better than a factor 2.2 for 19 of the 23 considered ADC designs.

Acknowledgements

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