A One-Bit-Signature BIST for Embedded Operational Amplifiers in Mixed-Signal Circuits Based on the Slew-Rate Detection

I. Rayane, J. Velasco-Medina and M. Nicolaidis
TIMA/INPG, 46 Avenue Felix Viallet, 38031 Grenoble France
E-mail : Iyad.Rayane@imag.fr

Abstract

A new BIST technique for embedded operational amplifiers in mixed-signal circuits is presented in this paper. The technique is based on the detection of the slew-rate deviation, which is a sensitive parameter to defects. The BIST circuitry requires a small area overhead. It is compatible with digital parts since it uses only logic gates, and generates a One-Bit-Signature (OBS), which offers a good observability of the test response. In order to validate the proposed BIST technique, an Op Amp circuit has been considered as test vehicle. Simulation results show that the proposed technique offers a high fault coverage.

1. Introduction

The importance of developing an efficient technique for testing of operational amplifier circuits is obvious since they are used widely in analog and mixed-signal integrated circuits. In addition, testing of analog functional blocks with embedded operational amplifiers is easier and the fault coverage is higher if one can assume that operational amplifiers are fault-free or if they are easily testable.

Analog circuits of small to medium complexity have been conventionally tested using functional specifications, where the functionality of the circuit is verified at some pre-specified test points. This method can result in either excessive or insufficient testing of the part. Fault-based testing is an attractive alternative to functional testing, which targets the presence of physical defects, thus providing a quantitative measure of the test process.[1]

Some BIST techniques presented in the litterature use the conversion of the circuit under test (CUT) parameters into a DC voltage and comparing it with a reference voltage [1] [2]. An oscillation test strategy is presented in [3]. This strategy is based on the reconfiguration of the CUT as an oscillator and measuring the oscillation frequency.

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The approach described in this paper is different from previous ones since it is based on the detection of a parameter that has not been considered previously which is the slew-rate.

2. Principle of the BIST

The slew-rate is an important high frequency parameter of an Op Amp, it is the maximum rate at which the output changes when input signals are large. It could be obtained by configuring the Op Amp as a voltage follower with a positive step on its input, and measuring the slope of the transient reponse which represents the slew-rate. Our investigation was carried out to see the behavior of the slew-rate with the presence of a defect in the Op Amp under test. Figure 1 shows typical transient responses of an Op Amp configured as a voltage follower with a positive step on its input. In this figure we present the transient response of a fault-free Op Amp and some transient responses of the Op Amp with faults inside it.

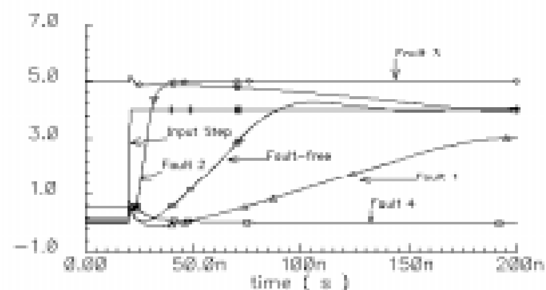

Figure 1 : Transient response of the Op Amp

As it can be seen, the presence of a fault deviates the slew-rate of the Op Amp. According to their effects on the slew-rate (Figure 1), faults could be divided as folllow: Faults that decrease the slew-rate (fault 1), faults that increase the slew-rate (fault 2), faults that stuck the output of the Op Amp at Vdd (fault 3), faults that stuck the output of the Op Amp at Vss (fault 4) and eventually faults that leave the slew-rate in the fault-free area.

In order to measure this time-domain information (transient response) we have realized a digitalization of

this using a CMOS inverter circuit. Figure 2 shows the output of the inverter corresponding to the voltages presented in figure 1. If we sample the output of the inverter at the two instants t_1 and t_2 (figure 2) using D-flip flops, we obtain a pair of values (v_1, v_2). This pair is equal to logical (1, 0) for a fault free Op Amp, and equal to (1, 1) or (0, 0) for faulty ones. XORing these two values generates the output of the BIST (OBS) that indicates the presence of a fault if it is at logical 0.

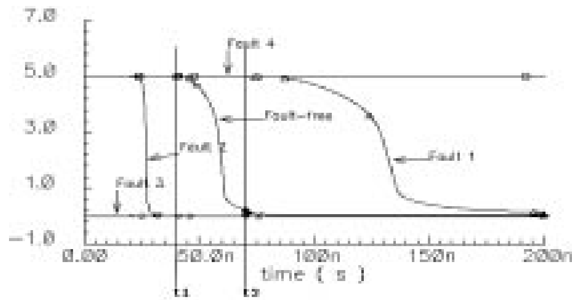

Figure 2 : Output of the inverter

The proposed BIST structure is presented in figure 3. The BIST is activated by the test control signal TST. This signal will configurate the Op Amp in the voltage follower configuration. The test stimuli is obtained from signal TST by using a delay element in order to ensure that the voltage follower configuration is established before applying it on the circuit. For creating the test response signature, two delay elements are used to generate the signals S1 and S2 corresponding to the sampling instants t_1 and t_2. They are used as clocks of two D-latches that sample the output of the inverter at these instants. Thus, in the fault-free case, the latches will sample the values 1 and 0 resulting on a 1-bit signature on the output of the XOR gate. This signature should be equal to 1 in a fault-free circuit.

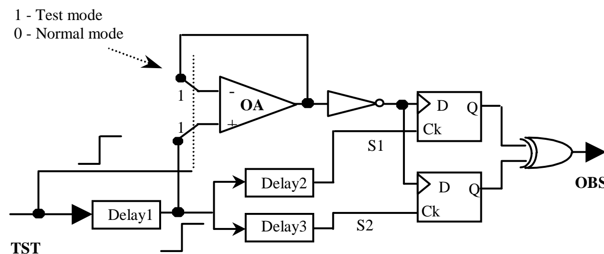

Figure 3 : The BIST structure

For illustration of the proposed technique, we use a classical Op Amp containing 11 MOS transistors, a bias resistance and a compensation capacitance, as a test vehicle. The first step consists of performing Monte-Carlo analysis in order to simulate the process tolerance effects on the response of the Op Amp and to set the sampling instants with a high accuracy of the test response analysis. For fault simulation purposes, we assume a complete set of the hard faults presented in [4]. For GOS faults, we use the model discussed in [5], 4 GOS faults were considered, they correspond to the following values of the model parameters, m = 0.2 and 0.8, R = 1Ω and 5KΩ. These faults were injected into the Op Amp and simulations were carried out in order to evaluate the fault coverage of the proposed technique. Table 1 resumes the fault coverage results.

	Shorts			Opens			GOS
	GSS	GDS	DSS	SOP	DOP	GOP	
Fault-Coverage	100%	100%	100%	100%	100%	100%	64%

Table 1 : The fault-coverage results

As it an be seen in table 1, this technique offers a full fault coverage for short and open faults.

The delay elements were implemented using inverter pairs. A special attention must be considered during the sizing of these elements in order to respect the corresponding delays. The area of the Op Amp used as test vehicle is ≅12000 μm^2, while the area of the BIST circuitry is ≅5500 μm^2 representing 46% of the Op Amp area, which can not be considered as a small area overhead. This is due to the simple Op Amp considered as a test vehicle. Real Op Amps contain up to 40-50 transistors, while the change that must be introduced on the BIST circuitry in the case of complex Op Amps is the sizing of the delay elements, this does not increase significiently the area of the test circuitry.

Presently we are extending our investigations to various classes of linear analog circuits with final goal a structured analog and mixed signal technique.

References

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