Parametric Built-In Self-Test of VLSI Systems

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Abstract

Conventionally, Automatic Test Equipment (ATE) has been used for parametric tests of VLSI systems to determine the influence of clock speed, supply voltage, and temperature on the specified functionality of the circuit under test. This method is likely to become infeasible in the near future due to an aggressive drive to increased Overall Timing Accuracy (OTA), as predicted in the SIA Roadmap.

In this paper, a method for Parametric Built-In Self-Test using on-chip Phase-Locked Loops (PLLs) is presented which is capable of overcoming the timing accuracy problem. A PLL-based test circuitry to determine the maximum frequency is described. Design constraints of the PLL control system, such as stability and resolution, are discussed for a specific design using 0.35µm CMOS technology. The functionality of the self-test circuitry is demonstrated to be competitive with parametric ATE tests such as Global Search Track without the need for expensive test equipment.

1. Introduction

The SIA Roadmap shows a steadily decreasing gap between the maximum frequency of Automatic Test Equipment and the maximum frequencies for near-future VLSI designs. There is no known solution so far to keep the Overall Timing Accuracy at or below ± 5.0 % of the on-chip clock period for frequencies above 1.25 GHz [1]. It is predicted by the Roadmap that, in contrast to the current situation where appropriate Automatic Test Equipment (ATE) for high-performance designs is available, accurate ATE will be unavailable for leading-edge designs with minimum feature sizes smaller than 0.18 µm. This leads to a strong interest in alternative test solutions. Post-fabrication circuit tests on ATE nowadays test for not only the logic functionality of the circuit but also for its dependencies on parameters such as clock frequency, supply voltage, and temperature. A common procedure for parametric testing is to create Shmoo Plots [2] of a restricted number of the fabricated circuits to visualize these parametric dependencies or to execute tests like Global Search Track to get the maximum frequency for a specific set of parameters.

For all applications with sufficient accuracy of ATE, the hardware costs will increase continuously, since the number of I/O pins of digital integrated circuits is increasing rapidly [1], while the cost-per-pin of commercial ATE will stay constant. Therefore, approaches that include hardware tester functionality on the ICs (*tester on a chip*), reduce the overall test cost per circuit. Recent complex VLSI designs contain Built-In Self-Test (BIST) circuitry for on-chip test pattern generation and test response compaction to test logic functionality, which facilitates tests with both a high fault coverage and an acceptable test application time. The presence of PLLs facilitates the design of on-chip parametric self-test circuitry that is capable of overcoming the timing accuracy problems of externally applied ATE tests.

In this paper, a method for parametric Built-In Self-Test using on-chip PLLs is presented that enables tests to be applied at on-chip circuit speed. The parametric BIST circuitry provides functionality similar to that of parametric ATE tests without the need for expensive test equipment. The design features and constraints of the parametric BIST design are compared to those of parametric tests provided by commercial ATE hardware. The rest of this paper is structured as follows. In Section 2, stability considerations of PLLs are presented as a background for the specific design constraints discussed here. In Section 3, the design of the proposed parametric maximum frequency self-test is described and an area estimation is given. Section 4 contains a comparison of parametric tests provided by ATE and parametric BIST circuitry in terms of functionality. Parametric BIST is proven to be competitive to ATE tests using a standard test problem. The results of this work are summarized in the conclusions in Section 5.

2. Stability of Phase-locked Loop control systems

In recent high performance IC designs such as microprocessors, on-chip PLLs are utilized to generate clock rates that are multiples of the fixed overall system clock rate or

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board clock rate. A PLL is a control system that synchronizes phase and frequency of the output signal of a voltage controlled oscillator (f_{out}, ϕ_{out}) to an input signal (f_{in}, ϕ_{in}). Although the PLL type utilized in this work is called *digital*, there are a number of analog signals, leading to a complex control system. Therefore, in the following sections, the constraints of PLL control systems are discussed. Common implementations of digital PLLs consist of the following main parts [3]: a phase detector (PD), a loop filter (LF), a voltage controlled oscillator (VCO), and a factor *N* divider in the feedback path of the control system. For this work, an additional programmable *M* divider is positioned at the frequency input to enable a local variation of the fixed board clock rate f_{in} (Figure 1).

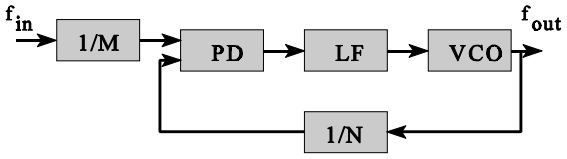

Figure 1: Block diagram of an extended PLL. The value of the output frequency is set, utilizing the two dividers, to $f_{out} = N/M \cdot f_{in}$.

The phase detector compares the phase of the input signal and the phase of the feedback signal and supplies an output current

$$I_d(t) = K_d \cdot \left(\frac{\phi_{in}}{M} - \frac{\phi_{out}}{N} \right) \qquad \textbf{(1)}$$

driven by a charge pump, where K_d is proportional to a constant current I_0. A passive loop filter usually consists of capacitors and resistors, representing a low pass filter of first or second order. The circuitry of the second order loop filter presupposed in this work is shown in Figure 2.

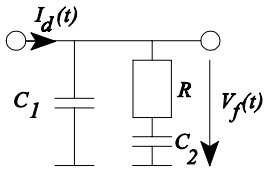

Figure 2: Passive second order loop filter

The transfer function of this filter is defined as:

$$F(s) = \frac{\mathcal{L}\{V_f(t)\}}{\mathcal{L}\{I_d(t)\}} = \frac{sRC_2 + 1}{sC_2 \left(sRC_1 + \frac{C_1 + C_2}{C_2} \right)} \qquad \textbf{(2)}$$

The output voltage of the loop filter controls the frequency of the *VCO* by adjusting the supply voltage of a chain of logic inverters. The transfer function is a constant value K_0. The phase transfer function $H(s)$ of the complete system is the product of the transfer functions of the single components:

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{N}{M} \cdot \frac{K_d \cdot K_0 \cdot F(s)}{N \cdot s + K_d \cdot K_0 \cdot F(s)} \qquad \textbf{(3)}$$

For the implementation of a parametric BIST circuit, the stability of the PLL control system in the lock-in case (i.e., the frequencies f_{in} and f_{out} are synchronized, and phase errors are adjusted continuously) has to be taken into account. If (2) and (3) are combined to get the final expression for $H(s)$, the resulting control system is of third order. To simplify the calculation of the damping, the order of the PLL is reduced using a method proposed in [4]. The behavior of a digital PLL of third order, that employs a charge pump in the phase detector, and a loop filter similar to the one shown in Figure 2, can be approximated by a second order model if the condition $C_1 << C_2$ is fulfilled. This is used to calculate the damping coefficient ζ of an equivalent reduced order phase-locked loop.

$$\zeta = \frac{RC_2}{2} \sqrt{\frac{I_0 \cdot K_0}{2\pi \cdot C_2 \cdot N}} \qquad \textbf{(4)}$$

Taking into account (4) with $N_{min} = 1$, ζ_{max} is calculated first. Next, N_{max} is derived from (4) as

$$N_{max} = \left(\frac{\zeta_{max}}{\zeta_{min}} \right)^2 \qquad \textbf{(5)}$$

Assuming that the minimal damping coefficient for stable PLL operation is $\zeta_{min} = 0.5$ [5], this results in $N_{max} \approx 28$ for the special case discussed in this paper. For this particular PLL, the damping coefficient ζ could be increased by changing the loop filter components R and C_2, as can be seen from equation (4). In general, ζ can be increased by a variation of all parameters that occur in (4). Yang et al. [5] propose the variation of I_0 to increase the damping of the PLL and achieve a frequency range for f_{out} of 0.3 to 165 MHz, while Goto et al. [6] proposed a VCO with variable amplification factor K_0.

If we design and implement parametric BIST circuitry, the above results for the stability of PLLs have to be taken into account.

3. Implementation of a Parametric Maximum Frequency Built-In Self-Test

The design of a linear search maximum frequency self-test is based on a commercial 0.35µm CMOS standard cell library and a CMOS compatible digital on-chip PLL. As shown in Figure 1, a programmable input frequency divider with factor *M* is proposed to be used in addition to the PLL circuitry. The maximum frequency self-test is realized in a way that allows utilizing existing BIST circuitry of the circuit under test (CUT). Previously-proposed approaches to parametric self-test did not take into account constraints of

realistic VLSI applications such as stability estimations [7] or determination of suitable frequency steps during test application [8].

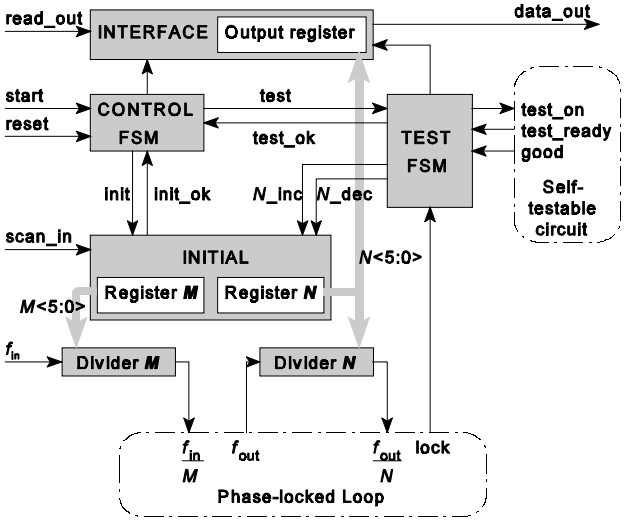

Figure 3: Block diagram of the proposed parametric BIST

The design proposed in this work consists of a PLL, programmable *M* and *N* dividers, initialization logic, interface logic containing the output register, and two finite-state machines: a control FSM and a FSM to apply the test. This subdivision has been done since the test application FSM may also be a part of the BIST logic of the CUT itself. To ensure a secure test operation, the *N* divider has to work at significantly higher frequencies than the maximum output frequency of the PLL. This is achieved by using a synchronous counter with parallel preset inputs for programming purposes. Figure 3 shows the block diagram of the proposed parametric BIST.

The total gate area of the parametric self-test logic using the 0.35µm standard cell library is estimated to be 0.0474 mm^2. Thus, only a negligible area is needed compared to the area of recent microprocessors. The PLL and the utilized BIST circuitry are assumed to be part of the circuit under test. Design verification of the parametric BIST has been done using a behavioral PLL model written in Verilog-HDL that contains calculated and measurement-data based parameters for all functional blocks of the PLL in combination with a LFSR/MISR-based self-testable circuit with programmable signal path lengths. All simulations have been performed using the Cadence Verilog-XL simulator. The minimum pin set of the parametric BIST includes three input pins for *start*, reading the output register, and *scan-in* of the counter registers, and a single output pin for *scan-out* of the resulting maximum frequency. Note, that the scan pins can be multiplexed with other signals of the CUT for further decrease in test pin count.

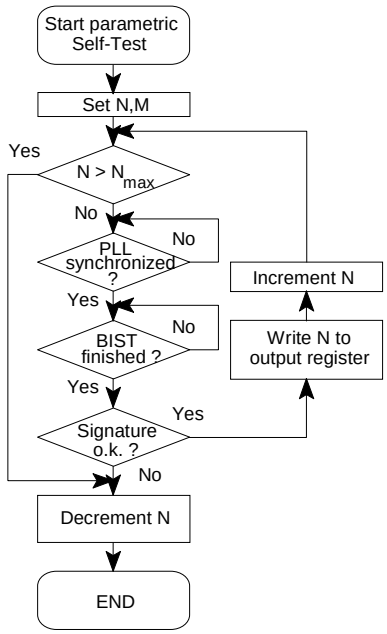

Figure 4: Flow diagram of the proposed maximum frequency BIST

The flow diagram of the proposed parametric self-test is shown in Figure 4. After the initialization of the *N* and *M* dividers, the test control unit waits for the PLL to synchronize. Synchronization is signaled by a *lock* signal created by the PLL's phase detector. Next, the built-in self-test is performed, using LFSRs and MISRs of the CUT, and the actual test response is compared to a golden signature. If the test is passed, the value of *N* is stored in the output register and *N* is incremented. The test is restarted as long as *N* does not exceed N_{max} and the test does not fail. The maximum frequency of the CUT can be easily calculated by multiplying the contents of the output register with the constant factor f_{in}/M.

The step width Δf of a linear search depends on the minimum input frequency of the PLL, factor *N*, and the maximum frequency of the CUT:

$$\frac{f_{CUT,\max}}{N_{\max}} \geq \Delta f \geq f_{PLL,\min} = \frac{f_{in}}{M_{\max}} \qquad \textbf{(6)}$$

The minimal input frequency of the PLL utilized in our design is $f_{PLL,min}$ = 2.0 MHz, the maximum frequency $f_{CUT,max}$ of the CUT is estimated to be 100 MHz with best case conditions, and the board clock rate f_{in} is set to 33 MHz. Therefore, from equation (6), we get M_{max} = 17 and N_{max} = 50. The latter value is beyond the theoretical range for PLL stability, as discussed in Section 3. However, this PLL is not optimized for a large bandwidth, which would be preferable for parametric BIST applications. With respect to our previous stability considerations, we set the divider coefficients by

default to be $M = 10$ and $N_{max} = 28$, resulting in a step width $\Delta f = 3.3$ MHz and a maximum BIST frequency $f_{max} = 92.4$ MHz. Based on the test constraints discussed in this section, the feasibility of parametric BIST and its competitiveness to ATE will be demonstrated using a typical test problem next.

4. Parametric BIST versus ATE testing

4.1. Properties of parametric BIST and ATE

The most important parametric ATE test setup for debugging and early characterization purposes of integrated digital circuits is the Shmoo plot [2]. A functional test is applied to the circuit under test for several different ambient conditions, usually for best-, typical-, and worst-case conditions. It is typically performed with voltage and clock period as the *primary parameters*. The slower parameter *temperature* can be visualized using the overlay plot option.

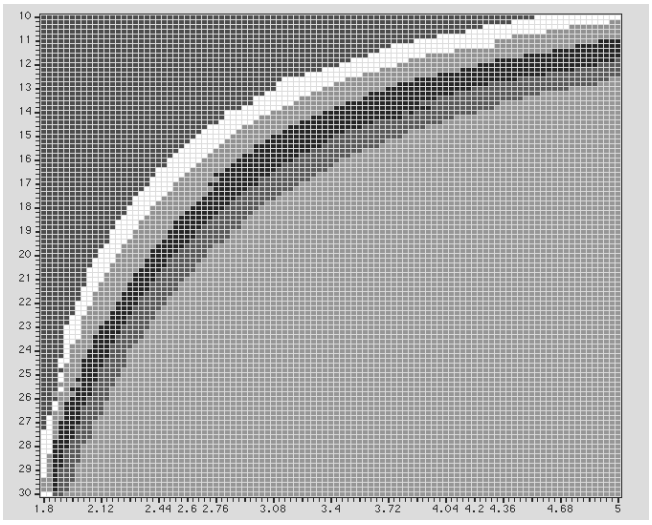

Figure 5: Shmoo plot of clock period vs. supply voltage for different temperatures based on a repeated functional test. For each parameter set consisting of voltage and temperature, a unique pass/fail boundary exists.

Figure 5 shows an overlay Shmoo plot of a video processor [9] in blockmatching mode. The overlay plot shows perfect characterisitics for all conditions.

In [2] it is argued that parametric tests visualized as Shmoo plots will increase in importance with future technologies since the necessary scaling of the supply voltages, as proposed in [1], will lead to inperfect MOS transistor properties and behavior. However, Shmoo plotting is done with a very restricted number of ICs only as a result of the high test time. In [8], test times for a DRAM Shmoo plot of 2 to 20 hours are reported. (Creating the Shmoo plot of Figure 6 took about 20 minutes.) To decrease the test time significantly, two approaches with ATE are possible, assuming that the test resolution must not be affected: the first is to perform Fast Shmoo plots, which create a plot of the pass/fail boundary if this boundary is uniquely defined. The second approach is to set one parameter (e.g., *supply voltage*) to a fixed value and perform a one-dimensional search such as Global Search Track [10] to determine the maximum frequency for best, typical, or worst case conditions. The proposed parametric BIST performs a test that is similar to the latter.

With parametric ATE tests, different search algorithms can be chosen: linear and binary search, and combinations of both. As long as there exists a unique and unambigous pass/fail boundary, all algorithms will lead to the same result. In the next subsection, an example is given where binary search algorithms may fail to detect the right pass/fail value. ATE tests often utilize a constant step width Δt_p. This decreases the resolution of the primary parameter in that regime that has to be tested. For example, at clock rates of 10 ns, a minimum step width of 0.1 ns leads to a step width of 0.99 MHz. During variation of the primary parameter (e.g., *period*), the additional parameters (e.g., *threshold voltages* V_{OH} and V_{OL}) have to be proportionally swept to keep track. In [11], the results of ATE and BIST based parametric tests differ slightly since V_{OH} and V_{OL} have erroneously been kept constant during ATE test application.

The main advantages of ATE tests are a high flexibility regarding the variety of different primary and secondary parameters and a high resolution of the test parameters. The main disadvantages are (1) the external test application with the need to disable the on-chip PLL [2], (2) the upcoming Overall Timing Accuracy problem with increasing clock rates, (3) the use of external test patterns with insufficient fault coverage, and (4) the restricted controllability and observability of parts of the circuit under test. As discussed above, different clock rates during ATE test application require external re-adjustment of the complete I/O timing.

In contrast, parametric BIST allows at-speed application of test patterns with deterministic high fault coverage to every circuit that is manufactured without the need for expensive ATE resources. Timing Accuracy problems during test will not occur for any recent or future technology, since the test signals are created inside the CUT. However, the connections between the pads of the CUT and the BIST-style registers have to be tested separately, as is done when scan testing is utilized with logic ICs. On-chip PLLs do not have to be disabled but instead can be utilized for maximum frequency tests. (Operation of the PLL may be even mandatory for the CUT, since it avoids application of infeasibly high external clock rates.) Parametric BIST suggests itself to be implemented with a constant step width of the test frequency Δf, resulting from the use of an on-chip PLL. The design of parametric BIST is straight forward, resulting in very small area overhead on top of a CUT area that includes conventional BIST circuitry.

4.2. Demonstration of the functionality of parametric BIST

In this subsection, a typical test problem is used to demonstrate the functionality of the PLL-based parametric BIST design.

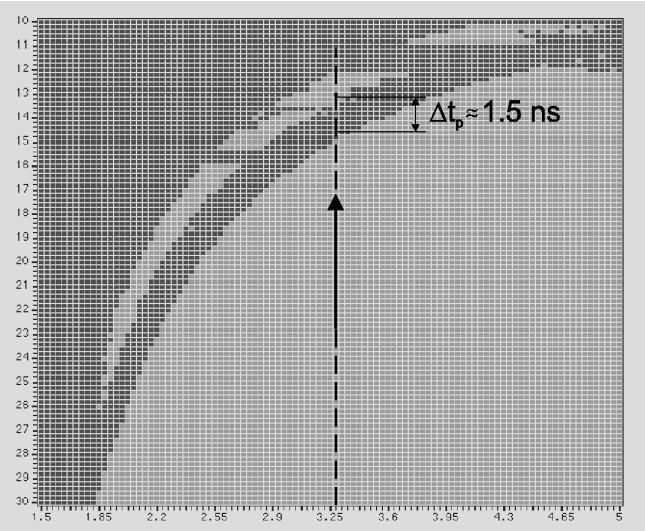

Figure 6: Shmoo plot of clock period vs. supply voltage. For most voltage levels, an unambigous assignment of a pass/fail boundary value is not possible.

In Figure 6, a Shmoo plot is shown that was created by testing an externally accessible functional unit of a complex video processor [9]. Besides the closed pass/fail boundary, a number of unintended *pass regions* occur for high frequencies, respectively low clock periods and different voltages. Therefore, a second pass/fail boundary may be present for the actual test parameter set. To securely avoid deriving this second boundary as the maximum circuit frequency, a linear search algorithm with an appropriate step width Δf or Δt_p has to be utilized. A binary or binary/linear search algorithm may erroneously detect the pass/fail boundary of an *island*.

To determine the value at the correct pass/fail boundary, it is necessary that the applied search algorithm touches the fail region between the main pass region and the islands. From Figure 6 we see that the boundaries are located at 12.8 ns (78.125 MHz) and 14.3 ns (69.93 MHz). Thus, the difference is 1.5 ns, and therefore Δf_{Gap} = 8.195 MHz. In Section 3, we calculated a step width Δf for the parametric BIST of 3.3 MHz, so the gap is touched twice in worst case. ATE using a maximum resolution of Δt_p = 0.1 ns touches the region between the main pass region and the island up to 15 times. However, also with ATE a larger and more realistic step width is likely to be chosen to decrease the total test application time.

This practical example shows, that parametric BIST is capable to perform tests such as Global Search Track of commercial ATE without the need for expensive external test equipment and without timing critical external pattern application.

5. Conclusions

In this paper, a method for Parametric Built-In Self-Test with realistic design constraints has been presented. Parametric BIST is proven to be capable of overcoming the increasing Overall Timing Accuracy problem of Automatic Test Equipment since it provides competitive functionality without the need for expensive ATE resources. In contrast to ATE testing, on-chip PLLs, which are more common with recent high frequency circuits and future technologies, can be utilized to apply at-speed patterns to the circuit under test. Based on a 0.35 µm CMOS design of a maximum frequency self-test circuitry, a high functionality has been demonstrated for a standard parametric test. The designed parametric BIST circuitry leads to a very small area overhead of 0.0474 mm^2 for CUTs which utilize PLLs and Built-In Self-Test logic.

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