Experiences with Modeling of Analog and Mixed A/D Systems Based on PWL Technique

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Abstract

The paper discusses the implementation problems of the PWL macrosimulation technique relevant to functional/ RTL level. Principles of the actual PWL approximation algorithm are briefly elaborated with respect to basic building blocks used for synthesis. Based on it the aspects of analog modeling in VHDL environment are considered. Different approaches to modeling of simple blocks and complex structures including some higher order effects are presented. Special attention is paid to feedback loop structures that require iterations. In mixed A/D modeling the signal conversion between PWL and logic domains is emphasized.

1. Introduction

Since the actual design strategies for ICs are hierarchical, also the need of mixed modeling at higher levels of abstraction begins to emerge. Besides, higher level models (e.g. functional-level) tend to comprise more specifications, to provide a designer with more detailed verification results prior to step down to lower design levels. In particular, the piece-wise linear (PWL) approach proved to be efficient in the functional-level A/D macrosimulation [2]. In this case for analog models usually inertial building blocks are used, whereas the digital units are modeled mainly by a logical description including delay effects. Signals propagating between the analog units are PWL waveforms, and when necessary they are converted to standard logic (and vice versa).

In order to put this approach into a broader perspective, the VHDL implementation has been performed for the PWL technique [3,4]. The developed analog models, although continuous in nature, are viewed there as discrete (in time) simulation objects based on the unique explicit formulas. As a consequence, the standard VHDL provided with some mathematical and PWL function packages shows to be sufficient for this purpose. Apparently, prior to these efforts, some work has already been done, however in only simple and traditional algorithms have been implemented in VHDL [1].

2. PWL Simulation Technique

Two main issues, modeling and signal approximation, constitute the PWL approach to simulation of analog and mixed A/D units. The PWL functional-level models make use of basic algebraic operators to characterize the static behavior, and simple inertial blocks or integrators (referred to as the basic building blocks) to mimic the transient effects. The required nonlinear functions (e.g. to model saturation) are represented in PWL form.

All the analog signals are assumed to be PWL waveforms as well. Clearly, when processed by the mentioned above static operators (with the exception of multiplication), they keep their PWL form. In contrary to this, the smooth waveforms produced by the dynamic blocks or multipliers must be converted into the PWL form. A unique noniterative approximation procedure may be used for this purpose.

In this way we avoid the CPU intensive traditional algorithms used to solve for differential equations. Moreover, during simulation we are able to work with much larger time steps, and always follow discrete points that satisfy the original solutions.

A wide class of analog and mixed A/D models has been simulated with the PWL technique [4].

3. PWL Analog Models in VHDL

The preliminary models, aimed at validation of the PWL approach, have been defined as stand alone behavioral VHDL objects. We have controlled them with a single process without sensitivity list using the WAIT FOR statement. It has been followed by the variable Tstep, calculated with the PWL algorithm, which suspended the execution of the process.

However, when creating a model that consists of more analog building blocks this simple construction fails. It is because the blocks usually produce their own PWL segments, which are often shorter than the input PWL segments. To cope with this problem we have supplied each block with an additional self-strobing mechanism, which allows a multiple execution of the process for a given input segment. In other words, the process has to

be activated by the sensitivity list, and the events of the self-strobe signal have to be produced, when necessary inside the model. Additionally the model must be "woken up" by the input signal. As a consequence, the sensitivity list comprises the following signals: (InputSlope, Tend, SelfStrobe), so that the order of the events is controlled by the 'delta time' mechanism.

Higher order effects, like the slew rate in case of an amplifier may be also modeled using the PWL approach. For this purpose the behavioral slope limiting mechanism (SLM) has been introduced. It begins to act not until some threshold voltage is crossed (approx. 100 mV for bipolar input stage and 1-2 V for MOS) and the input slope exceeds the prescribed value. The implementation of the SLM mechanism has to account for the scheduling of events, and when necessary to reduce the input signal slope. The SLM causes the effect of "time shift"; i.e. the length of the original PWL segment may be increased. The simple signal assignment with AFTER statement is not sufficient, since the signal driver might overlook some signal transitions. To avoid such errors we had to use a different delay modeling mechanism with TRANSPORT statement, so that all events are scheduled and assigned to the outputs at the proper time instants (e.g.: EndOut <= TRANSPORT Xactual AFTER Tstep).

With respect to the feedback loops, we can distinguish two classes of analog systems. The first one may be referred to as the "switching loop", where for a given portion of time only a part of that loop structure is active. Unlike the switching loops, the loops of analog nature tend to be closed (tight feedback). Apparently, different approaches are required to model the behavior of those two classes. While the switching loop models employ the typical features of the PWL mechanism, the analog ones usually need iterations. The iterative approach has a substantial influence on the modeling technique. Because of the feedbacks the proper values of output signals have to be calculated with iterations, and we have to stop in some sense the simulation clock ("to freeze the time") until the iterations are brought to convergence. To cope with this problem we employ the natural iterations (subsequent delta's generation) built into the VHDL simulator. Usually only several steps have to be done to complete the iterative process.

4. Mixed A/D Systems.

A connection between the analog and digital domains seems to be a particular problem in modeling of mixed A/D systems. The required interface is provided with the PWL-to-logic and logic-to-PWL virtual converters. At least a few solutions may be proposed here. The simplest models of converters are based on two logical levels and a single PWL segment between them. More accurate solutions take into account signal delays, different rising and falling edges, multivalued logic etc. Too complicated models may be not useful in practice. We have to avoid the situation when the unknown state is generated by the PWL-to-logic converter during the rising or falling edge of the signal (and vice versa). This unnecessarily produced state tends to spread through the digital part and may appear at the analog input. A trade-off is recommended in this case; the converter with two logical levels, which models inertial delay and a rising/falling edge seems to be a reasonable solution.

5. Summary

The piece-wise linear approach to modeling of analog and mixed A/D systems represented at the functional level proved to be computationally efficient. Also higher order effects, like capacitive output loading or slew rate may be accounted for. The implementation of the relevant models in VHDL environment is feasible thanks to the discrete nature of the PWL signals, for which the segment boundaries may be assumed as simulation events. We have addressed a variety of the implementation aspects. The simple processes of the individual models have been compared with the component processes of complex structures activated by the input signals as well as the special self-strobing mechanism. The implementation of the non-linear effects has been exemplified with the slope limiting mechanism used for the amplifier model. For the tight feedback loops that require iterations we have proposed the multi-process architecture with an extra output process controlling the iterations. In case of mixed A/D models we have emphasized the problem of signal conversion between digital and PWL domains. The ambiguity having its origin in unknown logical states may be avoided by means of a relatively simple converter model. The mixed A/D modeling based on the PWL technique provided with those virtual converters proved to be well suited to the unified VHDL environment.

References

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