Systematic Biasing of Negative Feedback Amplifiers

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Abstract

A biasing method is described, intended to make automated biasing of at least some classes of analog circuits straightforward. It has been tested for linear amplifiers, though it is not restricted to that class. A systematic way to introduce bias sources in a circuit is discussed. Also methods for reducing the number of bias sources and bias feedback loops are given. Application of the method has shown that at least for the class of amplifiers the theory is well suited for automation.

1. Introduction

Presently, biasing linear analog circuits is one of the more "vague" steps in a design. There are many rules of thumb, many commonly used configurations and little clear unambiguous design rules. This implies that generally an experienced designer has little problems in biasing a circuit, but that starting designers, like students and designers that cannot really deal with heuristics, like computers, have great difficulty in doing the job.

For negative-feedback amplifiers, a structured design methodology without heuristics has been developed [1, 5, 6]. It has been implemented in an amplifier design program [7, 9], that is, unlike many other programs, also able to synthesize the topology, using single transistors as basic building blocks.

For negative-feedback amplifiers, during the first steps of the design small-signal models are used for the active devices to design the signal behavior. During these "small-signal-design steps" biasing quantities do appear, but only as parameters to set the small-signal behavior. During the biasing step, DC bias voltage and DC bias current sources are introduced. Until now, a complete set of rules for biasing was not available and therefore it was not always possible to automatically bias the generated "small-signal solution". In this paper a bias methodology is introduced, that seems to be complete enough, to start automating this last design step.

2. The purpose of biasing

The parameters of the small-signal models are the first-order derivatives of the transfers in the large-signal model in a chosen operating point. The device is set at the operating point by *bias* currents and voltages. The signal that contains the information is superimposed on these bias quantities. At the output of the device the bias signals are subtracted and the information carrying signal remains. In figure 1 the principles of operation are shown.

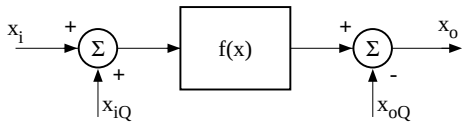

Figure 1. The principles of linearization with biasing signals.

First at the input a signal x_{iQ} is added to the input signal x_i in order to center it around the operating point of $f(x)$. At the output a signal $x_{oQ} = f(x_{iQ})$ is subtracted to center the result around zero again. Now the overall transfer of the system of figure 1 has become centered around zero, which is required for a linear transfer.

3. Biasing a device

A linear circuit is a combination of linear one-ports and linear two-ports. Linear circuits need no biasing, so they also have zero bias at their ports. When the linear circuit is implemented with practical devices, that do need biasing, the first step is to arrange the biasing such that it is not visible at its ports. It is arranged within the one- or two-port.

Fig.2 shows how this is done for a bipolar transistor. Four bias sources are added around the transistor. The sources are chosen such that the DC input and output voltages and currents of the twoport are all equal to zero, while the transistor is correctly biased.

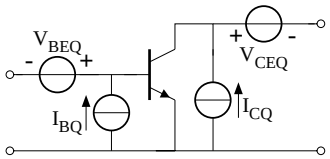

Figure 2. A transistor combined with biasing sources to form a linear two-port with zero bias condition at the input and output.

3.1. Setting the bias quantities

The devices that commonly need biasing are the mosfet and the bipolar transistor. (There are other non-linear devices that may need biasing also, but the techniques used there do not fundamentally differ from the principles described in this paper.)
All four biasing quantities have their influence on the small-signal behavior of the transistor. Any two of them can be chosen freely, the remaining two then follow from the input-output relations of the transistor. The bias quantities that have the most direct relation to the small signal (key)parameters are usually the drain current (I_{DQ}) and the drain-to-source voltage (V_{DSQ}) for the field-effect transistor and the collector current (I_{CQ}) and the collector-to-emitter voltage (V_{CEQ}) for the bipolar transistor. The biasing method described in this paper takes these two bias quantities as input from the signal design procedure and matches the other to sources by providing the necessary control.

In the remainder of this paper circuits with bipolar transistors will be used to explain the theory. For mosfets, the procedure is *identical*.

Rule: Four bias sources are introduced for every two-port device, as can be seen in the example of figure 2. They all should be such that the bias conditions both at the input and output port can be zero. Of these four sources, I_{CQ} and V_{CEQ} are set, the other two sources need control to match.

3.1.1 The voltage at the output

The voltage source V_{CEQ} is inserted as an independent voltage source. *The environment* has to keep the bias voltage at the output port equal to zero, since the two-port cannot do it by itself. The voltage source V_{CEQ} is at one side connected to the collector, that acts as a current source, which cannot define the voltage level. Therefore also at the output the bias voltage is undefined. When the environment sets it to zero, the collector voltage of the transistor will be correct.

Rule: At the output, a two-port containing a mosfet or a bipolar transistor, does not impose a voltage relation between the output terminals. The voltage depends on the environment, which should set it to zero.

3.1.2 The current at the output

The current source I_{CQ} is inserted as an independent current source. However, connecting an independent current source to a collector does not set the transistor to the desired collector current just like that. Either I_{BQ} or V_{BEQ} has to be controlled such that the error ΔI_C, with:

$$\Delta I_C = I_C - I_{CQ}, \tag{1}$$

in which I_C is the actual collector (bias) current, reduces to zero. Depending on the environment, a choice is made for one of them.

When the environment can not keep the input bias voltage to zero, controlling V_{BEQ} is no option for controlling I_{CQ}. The environment has an "open" character, which means that it delivers zero bias current and does not set a voltage relation between its terminals. The base current (I_{BQ}) needs to be controlled. For now, no control loop is added to the two-port, the current I_{BQ} is just marked as being controlled by ΔI_C.
When the collector current is set in this way, the base-to-emitter (V_{BE}) voltage is determined by this. Therefore, together with bias source V_{BEQ}, the two-port sets the input voltage bias to zero. Note that this follows from the fact that setting the collector current to a fixed value also fixes the base-to-emitter voltage, resulting in a zero input impedance of the two-port. It does not follow from the fact that there happens to be a conducting PN-junction from base to emitter. So also in the case of a mosfet, the two-port fixes the bias voltage at the input. The source V_{BEQ} is also controlled, but only to make the voltage bias at the input equal to zero, not to control I_{CQ}. Generally this control can be omitted, as will be discussed later.

Rule: At the input, a two-port containing a mosfet or a bipolar transistor, imposes a voltage relation between the input terminals, when I_C is controlled via I_{BQ}. The voltage relation cannot also be set by the environment.

When the environment actively keeps the input bias voltage to zero, V_{BEQ} has to be controlled based on ΔI_C. The environment has a "voltage-source character" and is certain to set a zero bias voltage between its terminals, without defining a current.

This could e.g. be the case at the input of an amplifier connected to an inductive source. Then the inductor sets the input bias voltage to zero but could sink an undetermined

amount of I_{BQ}, thereby making the relation between I_C and I_{BQ} undetermined. Still I_{BQ} needs control, but only to make the current bias at the input equal to zero, not to control I_{CQ}. Also in this case this control can often be omitted, as will be discussed later.

Note that for mosfets, the procedure is identical, so also *four* sources are inserted. Though a mosfet might not need an input bias current, still control of the bias current at the input must be there, at least to supply the charge on the gate capacitor to get to correct V_{GS}. So a controllable current is inserted, even if its steady state value would be zero. It may be that this control input is needed later. This can not be determined at this moment yet.

3.2. Passive devices

Passive devices need to biasing. No sources have to be inserted. A strict rule at the initial biasing step is that no linear device is allowed to support any bias current or voltage. This means that at this point non of the bias sources belonging to the active devices can be deleted because it has a "suitable" passive device in series or in parallel. Because of this also the well-known Thevenin–Norton transforms can not be applied.
(This means for example, that a resistor connected from a supply to a collector does not set the voltage on that collector. The value of the collector voltage is still undetermined.)

Shifting and merging of sources, which is done in a later stage, can lead to a current source in parallel and/or a voltage source in series with a passive device. In some cases, *purely accidentally*, it could be that the nature and the value of the passive component are such that the sources can be deleted. E.g. a linear capacitor with a bias voltage source in series could probably support the voltage across its own terminals.

4. Bias source manipulation

In figure 3a, the result of the first stage of the biasing method can be seen. Some currents are controlled, but to show the shifting operations it is not necessary to know which.

4.1. Current sources

Floating current sources are split into two sources that have one terminal referred to a common node called ground. Ground is the potential of the environment of the circuit.

Current source I_2 in figure 3b is split into two sources, one from ground to the collector of the cascode transistor, the other anti-parallel with I_1. Current source I_3 is also split into two sources, one from ground to the base of the cascode transistor, and the other anti-parallel with I_1. In figure 3b

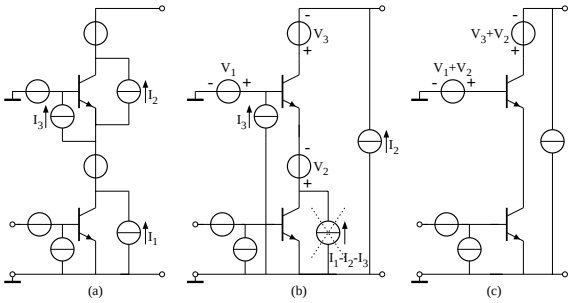

Figure 3. Biasing a cascoded transistor, (a) the initial situation, (b) manipulation of the current sources, (c) manipulation of the voltage sources.

the new situation can be seen. The source I_3 from the base of the cascode transistor to ground comes in parallel with voltage source V_1 and can therefore be deleted. When the parallel connection of the three sources at the collector of the lower transistor is evaluated, it is found that just I_3 remains (if $I_2 = I_1$ which is usually the case for circuits like this, if not, a larger source is left over, but this is not essential for the procedure that follows). Minimization of the number of current sources can be continued by evaluating the influence of the signal behavior of the amplifier when a current source is switched off.
This makes sense for current sources that connect to nodes that have more than two currents flowing in or out. Into the node mentioned above to which the the remaining I_3 is connected, 3 currents flow. When I_3 is set to zero, in this case the collector current of the cascode transistor is reduced. This will have influence on the small signal parameters of that transistor and so on the signal behavior of the amplifier. Therefore this small signal behavior has to be re-evaluated to see if this is still within the margins that are in the specification of the amplifier. If the behavior is still within the specifications, the source can be deleted.
A faster procedure is possible when margins for the collector currents are made available during the small signal design.

4.2. Voltage sources

The bias voltage sources can be shifted through the network by means of the E-shift rule[1, 5]. The target is to shift the sources through the network in such a way, that they end up in a branch that is connected to the central node called ground. The cascade of voltage sources that arises in those branches become the so-called supply voltages of the circuit. Note that with this method, the supply voltage is not given as a specification, but is found from the biasing conditions. It is possible to minimize the required supply voltage

by adequate shifting of the sources. The great advantage of this method is that it is clear which devices and which performance parameters are involved in setting the value of the supply voltage. If a lower supply voltage is demanded than found in this way, it is immediately clear which tradeoffs are possible to reduce the required supply voltage. When a higher supply voltage is allowed than the circuit actually needs, probably the performance of the circuit could be improved.

Sometimes it is not possible to shift a voltage source into a branch connected to ground. This e.g. happens for voltage sources that are in a mesh that does not contain the ground node. Then it is tried to cluster floating source in one branch as much as possible. This reduces the number of floating sources to be implemented and may even remove the floating sources if they happen to cancel.

An example can be seen in figure 3c, where voltage source V_2 is shifted through the cascode transistor and comes in series with V_1 and V_3. Research on an algorithm is currently going on.

4.3. Changing device types.

During the shift operation of current and voltage sources, currents sources can come in parallel and voltage sources in series. Their values are added. It is possible to reduce this sum, by changing the polarity of one or more of the sources. This is done by changing the type of the transistors. An NPN-transistor is replaced by a PNP-transistor, and an N-channel mosfet is replaced by a P-type. When the technology used is complementary (enough) in the essential parameters for the signal behavior, this can be done without redesigning the signal behavior. In other cases unfortunately one iteration in the signal design is necessary.

In figure 3c, V_2 and V_3 both represent a collector-emitter voltage. In this case they have the same polarity. When one of the two transistors is changed to a PNP transistor and the collector-emitter voltages are (or can be made) equal, the voltage source $V_3 + V_2$ becomes zero and can be removed. However, in that case the current sources I_1 and I_2 do not cancel any longer. The allowed supply voltage can be a guide in deciding which option is best used.

The number of bias-current sources is minimized and each current source has one terminal grounded. The most of the voltage sources are referred to a common terminal (ground).

5. Floating nodes

In a circuit, all nodes must have a well defined bias voltage relation to each other. Transistors can relate the two input nodes (B-E and G-S) as shown before. They do not relate their output nodes. *Linear (passive) components do not relate nodes either.* It can be investigated which nodes have a defined voltage relation. Nodes that are related form a cluster. In figure 4 it can be seen how two separate clusters of related nodes originate. For proper operation of a circuit *with respect to biasing*, there should be just one cluster. For the signal behavior more than one cluster is allowed. If more than one cluster is found, the clusters are floating with respect to each other. The clusters are only interconnected via bias current sources, device ports with current source character and linear components, that most likely need a certain voltage across them but can not enforce it. The bias voltage relation between the clusters is undetermined and if the total current (I_Σ) between the clusters is not exactly zero even unstable. It is necessary that the bias voltage relation is stabilized by controlling the error in the interconnection current (I_Σ), which means that at least one of the bias current sources that connects the clusters becomes controlled. Control is done by comparing the voltage difference between the two clusters and by using this difference to control one or more current sources. The device that is between the two nodes used for the comparison, determines the bias voltage difference that should exist between them. This is a know value. In the case of figure 4 the resistor between the nodes 1 and 2 requests, but cannot (by rule) enforce a zero difference.

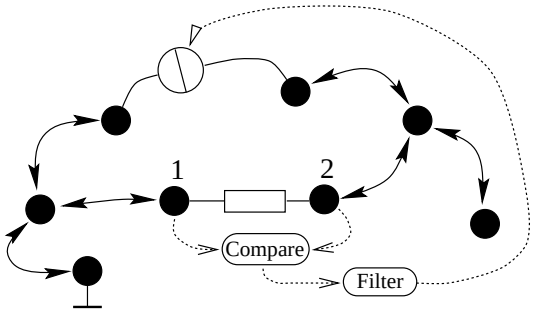

Figure 4. Controlling the bias voltage difference between separate clusters. Nodes that do have a defined voltage relation are connected with arrows.

Special measures have to be taken such that the introduction of the control loop does not influence the signal behavior. Interference of the loop can be prevented by placing a frequency filter in the loop or by making use of balancing techniques (common mode/ differential mode). However, this is beyond the scope of this paper.

In cases like figure 4, it may be that the value of the transfer (transconductance) from voltage difference, to a correction current that could be inserted in parallel with the resistor is close enough to the trans-conductance of the resistor. In that case the control could be done by the resistor and no

extra loop is needed. Cases like this are easily found during evaluation of the clusters by inspecting the values of the resistors (and inductors) that are between the clusters.

6. Bias-source control

A number of sources have been indicated as controlled. Every control loop could be implemented separately, which is feasible for simulation purposes. For a practical circuit the number of loops must be reduced to a minimum. A number of reduction techniques exists. For example, when two transistors Q_1 and $Q2$ are cascaded, the controlled input bias current I_{BQ2}, comes in parallel with the output bias current I_{CQ1}. Then the control of I_{BQ2} can be passed on the the controlled source that is related to I_{CQ1}, which could be I_{BQ1}. I_{BQ2} can than be chosen constant and added to the value of I_{CQ1}. In this way, by controlling one current (I_{BQ1}), the collector currents of the two transistors involved will be correct. In most cases the reduction results in one remaining overall loop that needs to be implemented and perhaps some simple local loops. Also in this case, special measures have to be taken such that the introduction of the control loop does not influence the signal behavior. Details on this can be found in [1].

Most of the controlled voltage sources, like V_{BEQ}, come in series with constant sources, like V_{CEQ}, of which the value is not very critical. Then these sources can be made constant. When a voltage source does need control, to equate voltage bias conditions to zero, implementing it as a coupling capacitor can be a simple solution. In cases where this causes an unacceptable alteration of the signal frequency behavior, an actual control loop needs to be implemented. Also on this topic, details on this can be found in [1].

7. Conclusions

A non-heuristic bias methodology has been presented, that is suitable for automation. Special attention was paid to the way the biasing of the active components is introduced and to the way the control of the bias sources is arranged. The methodology has proven to work for negative-feedback amplifiers and other simple amplifiers, but should work for more linear circuits. This is still a topic for further research. Presently, prototype software is being developed to arrive in the end at a tool that is able to bias any (automatically) generated amplifier with no restrictions on topology.

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