A Fault List Reduction Approach for Efficient Bridge Fault Diagnosis

Jue Wu† Gary S. Greenstein†† Elizabeth M. Rudnick‡

†Sun Microsystems, Menlo Park, CA, USA †† Synopsys, Inc., Marlboro, MA, USA
‡Center for Reliable & High-Performance Computing, University of Illinois, Urbana, IL, USA

Abstract

A new fault list reduction approach is proposed for use in the first stage of a two-stage bridge fault diagnosis procedure. Modified structural analysis and layout extraction procedures are performed to obtain a reduced realistic bridge fault list that can be used in the second stage, which employs diagnostic fault simulation. The fault list reduction approach can reduce the final candidate bridge fault list by 92% to 99% compared with the diagnosis results achieved by the diagnostic fault simulator alone.

1 Introduction

Failure analysis can be performed by doing fault diagnosis to isolate a defect down to a set of candidate locations on a device, based on information about the faulty response and the expected responses of possible faults, and then using a hardware technique such as electron-beam probing to resolve the failure down to a specific defect. For state-of-the-art VLSI chips containing millions of transistors, fault diagnosis starting from the complete fault space is not practical. A two-stage fault diagnosis procedure is a necessity for very large designs. In the first stage, heuristics are used to reduce the fault list to a reasonable size and localize the fault to one or more modules. In the second stage, diagnostic procedures are then used to locate the defect using the reduced fault list and the portion of the design identified in the first stage. The *two-stage fault isolation* approach proposed in [1] for combinational and sequential circuits is an example in which a *limited fault dictionary* is used for fault list reduction in the first stage. An alternative approach for combinational circuits uses circuit structure information to narrow down the possible defect sites by taking the intersection of fanin cones of all failing outputs [2]. Both of these approaches apply to defects that behave as single stuck-at faults.

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We propose a new approach to fault list reduction for combinational circuits that targets two-node bridge faults. A complete diagnosis procedure will contain similar procedures for various fault models, and an accurate diagnosis may require several passes where the various fault models are considered in turn. The proposed procedure has some similarities to the one described in [3], but it achieves better resolution.

2 Fault List Reduction

Layout extraction finds all nodes that are adjacent to a given node and that can possibly be bridged to the node in the physical design. Layout extraction can reduce the fault list size from $O(N^2)$ to $O(N)$. However, the fault list resulting from layout extraction alone can still be very large for a complex VLSI design. We use a modified structural analysis procedure in addition to bridge fault extraction using FAULTAN [4] to further reduce the fault list size. All realistic bridge faults related to the nodes in the fanin cone of a failing output are extracted. Since at least one of the bridged nodes exists in the fanin cone of each failing output, the bridged node pair must also be contained in the realistic bridge fault list associated with each failing output. By taking the intersection of the bridge fault lists associated with all failing outputs, the original fault list can be significantly reduced, and the bridged node pair will be contained in the resulting fault list.

The bridge fault reduction algorithm is carried out in two steps. The first step involves backtracing each failing primary output (PO) and finding all nodes in their fanin cones. The backtracing step is followed by layout extraction, which discovers all realistic bridge faults involving at least one of the nodes in the fanin cone of each failing output. In order to reduce the execution time of each diagnosis, the backtracing step and layout extraction are performed as preprocessing steps, and the resulting realistic fault list associated with each PO is stored. Therefore, backtracing and layout extraction for every PO are executed only once for each circuit and layout design.

The second step of the bridge fault reduction process involves intersecting realistic bridge fault lists associated with all failing outputs contained in the faulty responses. This step is performed dynamically during fault diagnosis. A failing PO can be detected by different test vectors, but the intersection of its associated realistic bridge fault list with other fault lists needs to be performed only once. Therefore, the number of list intersections being executed is bounded by the number of POs in the circuit.

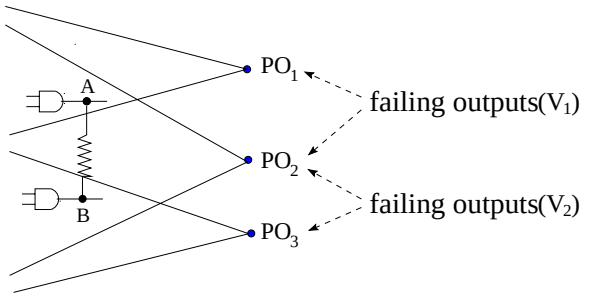

Figure 1: Bridge fault example

In the example shown in Figure 1, node A is in the fanin cones of PO_1 and PO_2; node B is in the fanin cones of PO_2 and PO_3. Node A is driven to a faulty logic value when test vector V_1 is applied, and the fault effects are then propagated to PO_1 and PO_2. When test vector V_2 is applied, node B is driven to a faulty logic value, which is then propagated to PO_2 and PO_3. During backtracing from PO_1, A is found in its fanin cone. When layout extraction is performed for every node in the fanin cone, node pair (A, B) is included in the resulting realistic fault list. During backtracing from PO_2, both A and B are found in the fanin cone, and node pair (A, B) is also included in the fault list. Finally, B is found in the fanin cone of PO_3, and node pair (A, B) is again contained in the realistic fault list for PO_3. Therefore, (A, B) is included in the final candidate fault list when the intersection of the three fault lists is taken.

3 Results

Experiments were carried out on an HP 9000 J200 with 256 MB RAM to evaluate the proposed fault list reduction procedure. Compact test sets generated by HITEC were used, and the E-PROOFS bridge fault simulator [5] was used to model the faulty device responses for 200 random nonfeedback bridge faults in each ISCAS85 benchmark circuit studied. The sizes of the bridge fault lists resulting from the bridge fault reduction procedure are presented in column 4 of Table 1. The percent reduction compared to layout extraction alone is shown in column 5. The average execution time for taking the intersection of the realistic bridge fault lists associated with all failing POs is displayed in column 6. The fault list reduction is moderate for most small ISCAS85 circuits, since the fanin cones of their POs are overlapped to a great extent. In practice, many complex circuits consist of multiple modules whose fanin cones overlap very little. For these circuits, the proposed procedure can localize the defect to a small portion of a complex circuit and can significantly reduce the fault list size.

Table 1: Bridge Fault Reduction Results

Circuit	All-Pair Bridge Faults	Bridge Faults		Reduction	Time
		Layout Extr.	Structural Anal.		
c432	28.2K	1585	1324	16.5%	1.31s
c499	32.8K	2791	2279	18.3%	6.54s
c880	126.3K	3275	1358	58.5%	2.13s
c1355	195.0K	4434	3545	20.0%	23.2s
c5315	140.2K	40,442	2859	92.9%	1.84m
c6288	3.8M	21,899	11,367	48.1%	3.63m
c7552	15.0M	53,785	6821	87.3%	3.54m

The fault list reduction procedure was combined with diagnostic fault simulation [6] in a second set of experiments. A 92% to 99% reduction in fault list size was achieved by using the fault list reduction procedure in a two-stage diagnosis procedure instead of using the all-pair bridge fault set. For most ISCAS85 circuits, over half of the diagnoses generated a single candidate fault, and the average number of candidate faults was reduced to less than 30. On average, 90.4% of the diagnoses produced fault list sizes less than 20, and 6.3% produced fault list sizes between 20 and 100. Less than 3% of the diagnoses generated fault list sizes greater than 100.

References

[1] P. G. Ryan and W. K. Fuchs, "Dynamic fault dictionaries and two-stage fault isolation," *IEEE Trans. VLSI Systems*, vol. 6, no. 1, pp. 176–180, March 1998.

[2] F. Hsu, P. Solecky, and R. Beaudoin, "Structure trace diagnosis for LSSD board testing – An alternative to full fault simulated diagnosis," *Proc. Design Automation Conf.*, pp. 891-897, June 1981.

[3] Y. Gong and S. Chakravarty, "Locating bridging faults using dynamically computed stuck-at fault dictionaries," *IEEE Trans. Computer-Aided Design*, vol. 17, no. 9, pp. 876–887, Sept. 1998.

[4] T. Chen and I. N. Hajj, "A hierarchical bridging fault extraction approach for VLSI circuit layouts," *Proc. Int. Symp. on VLSI Tech.*, 1997.

[5] G. S. Greenstein and J. H. Patel, "E-PROOFS: A CMOS bridging fault simulator," *Proc. Int. Conf. Computer-Aided Design*, pp. 268-271, Nov. 1992.

[6] J. Wu and E. M. Rudnick, "A diagnostic fault simulator for fast diagnosis of bridge faults," *Proc. VLSI Design Conf.*, Jan. 1999.