A Digital Partial Built-In Self-Test Structure for a High Performance Automatic Gain Control Circuit

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Abstract

It is now widely recognised that Design-for-Testability and Built-in Self-Test techniques will be mandatory to meet test and quality specifications in next generation mixed signal integrated systems. This paper describes a new digital on-chip post processing function capable of reducing production test time for a high performance automatic gain control circuit by 70%.

1 Introduction

Projections on the likely trend in silicon technology such as those given in the SIA roadmap have confirmed that the current difficulties being experienced in the mixed-signal community related to test, will grow unless testability is seriously considered as a primary specification in the design process. As device sizes fall below 0.25µm and transistor counts escalate, it will become impractical to run a full specification test on a multi-configurable system. This is already proving to be a problem with current mixed-signal designs where the main contribution to test cost is the typically smaller analogue section. These testability issues have to be addressed early in the design cycle before layout generation. It is expected that Design for Testability (DfT) optimisation, partial & full BIST (Built-In Self-Test) will be driven by experience and knowledge generated from a range of case studies. This paper represents one of these studies and a partial BIST solution for an automatic gain control circuit.

The paper is organised as follows. In section 2 an overview of key advances in mixed signal DfT and self-test are presented. In section 3, the AGC structure and the DfT study is summarised. In sections 4 & 5, the test evaluation procedure is presented that has resulted in a proposal for efficient on-chip digital test support. The simulation results and the implementation are summarised in section 6. Finally the paper concludes with a discussion and future issues.

2 State-of-the-Art in Analogue and Mixed-Signal Design for Test

In the digital domain, design for testability (DfT) is well established [1], with full or partial scan [2] being implemented successfully in the majority of complex products. In addition, the IEEE standard 1149.1 test access port and boundary scan architecture [3] has been well accepted by digital designers. Due to the dramatic increase in the complexity of digital circuits, built-in self-test (BIST) has been realised mainly in highly structured commercial designs to implement some of the test functions on-chip.

Currently, functional testing is performed on analogue circuits after wafer processing, where every IC is checked against critical specifications [4, 5]. The optimisation of such circuit specific test programs is difficult and expensive. Generic DfT guidelines and practical mixed signal BIST which can be applied in the early design stages could pave the way to satisfying industrial demands for the use of digital only testers [6, 7]. Increasing test costs, aggressive demands on time to market, and the need to improve product quality currently drive this change in test philosophy.

An overview of defect oriented testing and DfT optimisation of mixed signal ICs is presented in [5, 8, 9, 10]. Several DfT studies have been published, including work on a current mode DAC where test vectors are optimised and redundancies removed [11], on analogue filters where the controllability and observability is improved to test a number of stages separately [12, 13, 14] and on flash ADC [15, 16]. Motivated by the success of the 1149.1 scan bus, the IEEE Mixed-Signal Testability Bus Standard P1149.4 has been developed [17, 18] which is likely to radically improve test access at the system level. The Analogue Circuit Observer Block [19] reduces the need for precision by encoding the data during circuit test. A DfT system level architecture, using the sw-opamp concept [20], improves the controllability and observability in a multi stage circuit and includes off- and on-line tests with BIST capabilities [14]. A similar

demonstrator has been chosen for AUBIST [21] which compares the output response of cascaded biquads. The multifunctional ABILBO structure includes a test stimulus generator (TSG), output response analyser (ORA) and an analogue scan path. Further proposals have been made to realise a pure analogue BIST. The TBIST [22] translates parameters at certain circuit nodes into a proportional DC voltage to verify whether a parameter (gain or phase) is inside specification. The ABIST [23, 24] allows parallel loading of test data (voltages or currents) into a buffer and serial transfer to the output. The structure has been extended for mixed signal circuits in order to implement one structure that enables digital and analogue BIST [25]. The HBIST concept [26] includes an on-chip TSG that converts digital test patterns to a test stimulus, and is realised by the reconfiguration of cells already present to perform the digital BIST. Other concepts suitable for mixed signal circuits where the digital kernel is surrounded with analogue sub-circuits on the input and output, are the MADBIST concept for ΣΔ converters [27] and a BIST for the converters on a single-chip CODEC [28]. The OBIST technique [29], suitable for both functional and defect oriented testing, is based on the oscillation test methodology. Finally, a promising approach to calculate analogue parameters for DAC's and ADC's has been presented by Sunter and Nagi [30].

In the majority of cases, the effort and initial financial investments required to integrate DfT are justified, as either test cost or test quality is improved. Additional benefits are gained where the design becomes part of a cell library or is intended for re-use. Most DfT methodology should also be re-usable to be industrially practical.

3 Detailed DfT study on an Automatic Gain Control Circuit (AGC)

In this section a summary of the DfT study is provided, and further details can be found in [31].

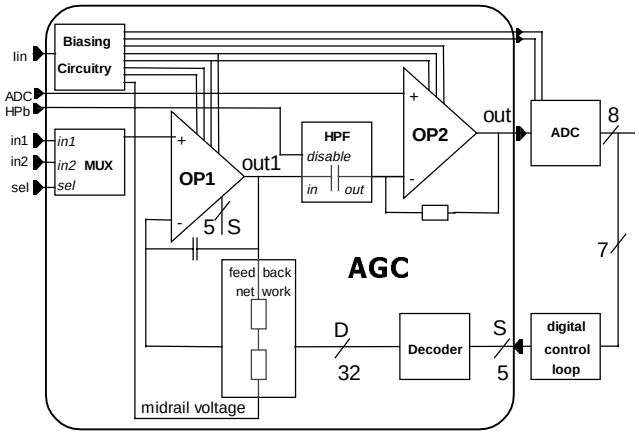

Figure 1: Simplified AGC structure

The demonstrator is an AGC macro used to digitise sound signals. As shown in Figure 1, the input stimulus is fed to an adjustable high bandwidth OTA (*OP1*) in a non-inverting configuration whose gain is controlled digitally. The gain can be varied in 32 steps by a decoder on the 5-bit gain set *S* provided by the digital control loop. The high pass filter (*HPF*) with a 3 dB corner frequency of 3.5 MHz is controlled by the top level signal *HPb* and can be by-passed. The second stage of the AGC is an inverting folded cascade OTA (*OP2*) providing a level shift, as the output (*out*) is referenced to the 24.57 MHz flash-ADC mid-ladder potential.

The AGC, containing 544 CMOS transistors, 394 in the digital converter, has been designed in a 1.0μm single poly double metal CMOS process and occupies 0.4mm^2 of silicon. A typical test plan for the AGC circuit is listed in Table 1.

1	AC performance in all gain sets (gain peaking, group delay)
2	DC offsets in 3 gain sets using Monte-Carlo analysis
3	Transient response to switched capacitor load.
4	Transient response to input sinusoid at two frequencies

Table 1: Functional test program

The main test problem for this circuit is the variable gain. Furthermore, two inputs and the configuration with en-/disabled *HPF* need to be tested. A massive reduction in test time could be achieved by simplifying the gain step test by on-chip test response evaluation or pre-processing circuitry.

3.1 DfT Solutions

The objective of reducing test time, improving fault coverage and if possible providing on-chip test support has been based on intuitive assumptions supported by fault simulation. The initial study has carried out a detailed investigation into the layout, schematic and system level testability problems through detailed fault simulation using a layout extracted fault list. The results from this study have catalysed the design of a digital on-chip test function that is described in section 4. The maximum Fault Coverage and Weighted Fault Coverage (weighted by fault probability) achievable by the proposed DfT optimisation is **99.04%** and **99.39%** respectively. In addition, the following DfT rules and guidelines were generated from the study:

- *Resistor layouts: Adjacent polysilicon (diffusion) tracks should not belong to the same resistor to prevent parametric faults caused by extra resistive material. Additionally, adjacent tracks should not*

belong to resistors connected to each other, as shorts affecting these tracks are difficult to detect.

- *Cascode transistor shorts: The current consumption and / or the output voltage has to be made more sensitive in stand-by mode in order to detect drain to source shorts at cascode transistors.*
- *On-chip test support: Reduce demands on ATE (Automatic Test Equipment), pre-process test response on-chip through re-use of existing mixed signal and digital structures.*
- *Reconfigurable circuits: Run simple separate test in reconfigurable structures, such as the AGC feedback network.*

3.2 System Level Self Test

As a result of the detailed study of the AGC design [31], the DfT guidelines above have been proposed. Based on this knowledge, a new AGC design has been studied, similar to that presented in Figure 1 but with resistor ladder layout structure according to the above DfT rule. In addition, a number of other design modifications have reduced the probability of many difficult to detect defects. As a result, any fault in the reconfigurable part of the AGC caused by an extra material spot defect will result in one or more entirely missing gain step(s).

For this design, the testability data compiled in section 3.1 has been used to design a test response evaluation function at the top hierarchical level of the design based on the following DfT guideline: *Re-configurable cells should be proven fault free for every configuration in a simple separate test.* This will result in a major reduction in test time, as the complete system needs to be tested in fewer configurations. In addition, the possibility of using this structure to support the additional tests proposed in [31] has been carried out (ramp test to verify the output voltage swing (OVS) of AGC & simple DC measurements).

In the current test program, a sine wave is applied to the AGC and its gain calculated off-chip by a FFT for every gain set applied to the AGC. Aiming for a decrease in test time and on-chip test support, a different routine can be proposed to verify the presence of gain steps. Applying a DC voltage to the analogue AGC input and incrementing the gain set (*S*) via a 5-bit counter will generate a predictable output response. The digital output (*D*) has to show an increase for each new gain set applied. By selecting a threshold, it can also be verified that the gain step is of a certain size. In the test program, for each gain set applied, the sampled output of the ADC has to be proven larger than the previous sample plus a minimum gain step size.

Several implementations of this test methodology can be proposed. Here we have chosen to add additional circuitry, including binary buffers, counters, adders and a comparator to enable on-chip test evaluation. The test circuitry is added to the top level of the design.

4 Test Evaluation Circuitry

Figure 2 shows the blocks that have to be added to the AGC design at the top level to allow on-chip test evaluation. The sum of a set number of ADC output patterns is calculated within the *sampling circuitry*. The sample taken can then be compared against a previous sample and the difference can be checked to be larger (or smaller) than a set threshold within the *test evaluation* block. Test parameters can be set by initialising the contents of the registers and the counters. These blocks will be embedded in a digital scan chain that will also be used to read out the test signature.

This purely digital circuitry allows the generation of a simple pass/fail output for the gain step size test and the verification of the OVS when a ramp stimulus is applied to the AGC input.

The purely digital partial BIST structure has the following main advantages compared to conventional testing:

- *ATE supplies only speed control and test access*
- *Use of digital access structures, e. g. IEEE 1149.1 test access port*
- *Synthesisable from Verilog/VHDL*
- *Requires no or minor changes to AGC (section 5)*
- *Simple pass/fail result*
- *Easily enhanced through the addition of diagnosis features*

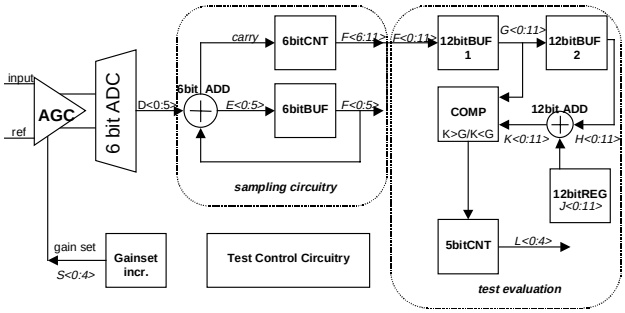

Figure 2: Test evaluation structure for AGC

4.1 AGC Gain Step Size Test

The test routine has been described above. For the implementation of this test, the cells *6bitADD, 6bitCNT* and *6bitBUF* are used to add a set number of ADC output codes (*D<0:5>*, see Figure 2). *F<0:11>* holds the sum of the samples taken. *12bitADD* adds the test threshold

(*J<0:11>*), set in a *12-bit register*, to the previous sample (*H<0:11>*) which has been buffered in *12bitBUF2*. The sum (*K<0:11>*) is compared to the new sample (*G<0:11>*) held in *12bitBUF1*. If *G>H+J*, the minimum gain step has been proven present. Every time the gain set (*S<0:4>*) is increased by *gainset_incr* the comparator output is added to form *L<0:4>* in *5bitCNT*. When the test is completed, *L* has to be equal to 32. The use of two 12-bit registers allows testing each gain step for a minimum and maximum size. When the test threshold (*J<0:11>*) holds the maximum gain step size, it has to be proven that *G<H+J*.

A more detailed block diagram is illustrated in Figure 3. Four test parameters can be set by the use of a scan chain. *N* defines the number of ADC outputs that have to be added in the sampling circuitry (2^N, for $1 \le N \le 5$). *GI* defines the gain step increase and can be varied between 1 and 7 (for more details see section 5.1). The minimum or maximum difference (*I*) in the samples taken can be set in the *12-bit register*, while *MinMax* has to be set high/low to test for a minimum/maximum difference.

The circuitry proposed can be run at the same speed as the A-to-D converter in the analogue front-end. The expected test time is:

$$t_{gainsteptest} = t_{ADCclk} \cdot 2^N \cdot 32,$$

where t_{ADCclk} is the ADC clock period, 2^N the number of ADC output codes sampled, and "32" is the number of gain sets.

Noise effects are eliminated by summing a set number of ADC outputs using the result as the parameter processed within the test evaluation block. The more output codes summed, the better noise cancellation.

Offset effects have also been cancelled, as they influence every sample set in the same way. Only if the offset drives the ADC input out of the valid input range, will the sample sum become faulty (smaller than it should be). However, this would result in a decreased gain step, and also the following gain steps will be too small. The magnitude of tolerable offset can be taken into account by properly selecting the DC input voltage of the AGC and its reference voltage.

By implementing this top-level test evaluation circuitry, the expected test time for the AGC can be reduced by about 70% without a decrease in test coverage.

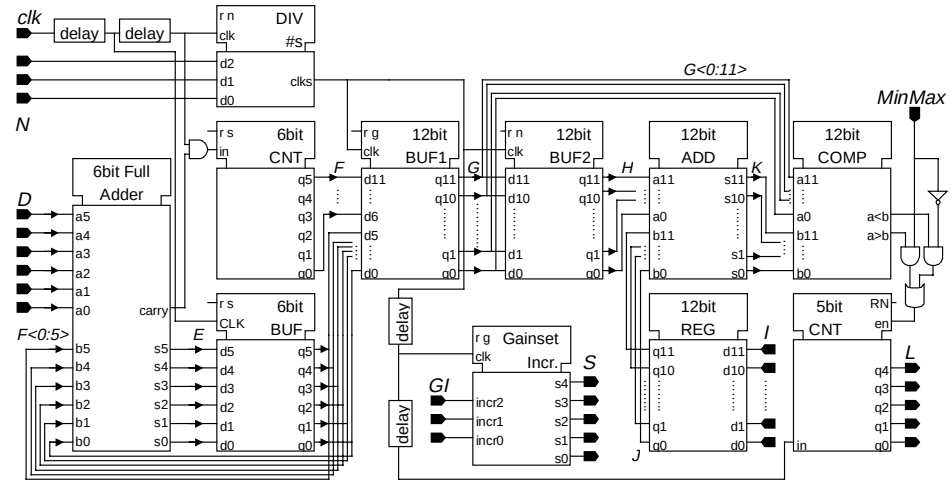

Figure 3: Test evaluation circuitry

4.2 AGC Ramp Test

Most faults affecting the AGC can be detected by testing the OVS of the AGC, as they cause a 'stuck at voltage' or 'stuck at voltage range' at the AGC output. The test response to a ramp stimulus applied to the analogue input of the AGC can be evaluated on-chip by the circuitry described above.

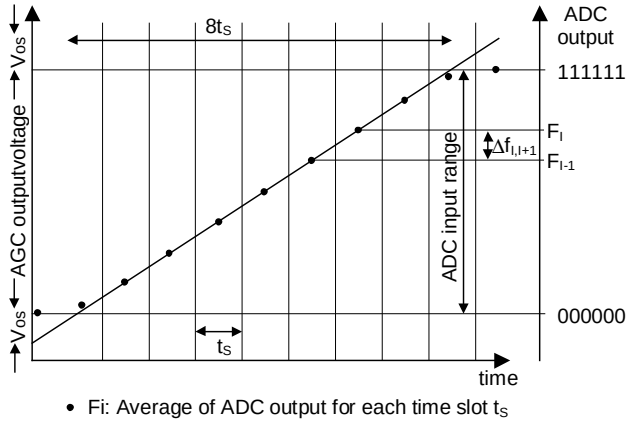

Figure 4: Ramp test evaluation

For each time slot t_S, the ADC output is sampled (Figure 4). The samples F_i represent the average of the ADC output for each section. The *test evaluation* block (Figure 2) is then used to count the number of time slots where the difference ($\Delta f_{I,I-1}$) between the sample taken (F_I) and the previous sample (F_{I-1}) is in a specified range. The contents of *5bitCNT* can be directly related to the OVS of the AGC.

The ADC sampling frequency, the number of ADC outputs to be sampled in the *sampling circuitry*, and the thresholds for *test evaluation* can be set by initialising the contents of the registers and counters.

To test the AGC output voltage swing, the required measurement resolution has a significant impact on the test

time. The resolution is mainly influenced by the number of ADC output samples that have to be taken (see Figure 4). The authors propose to add 64 ADC outputs in order to extract a precise and noise tolerant averaged response over each time slot t_s. The test time can be give as:

$$t_{ramp} = t_{ADCclk} \cdot 2^N \cdot s,$$

where t_{ADCclk} is the ADC clock period, 2^N the number of ADC outputs to add, and s the number of time slots (32 maximum). The OVS can be calculated from the test signature L (see Figures 2&3):

$$OVS_{meas} = l \cdot j$$

where l is the decimal representative of the test signature and j the minimum difference (set in *12bitREG*, Figure 2).

5 AGC Gain Step Size and ADC Resolution

To determine the minimum difference in the samples taken for two gain sets (*J*, Figure 2), the ADC resolution and the change at the AGC output has to be taken into account. The DC input voltage has to be selected properly to tolerate offset effects and to be close to the upper limit of the ADC input range. The smallest ADC input voltage is determined by the reference voltage of the AGC. If the increase at the AGC output is smaller than the ADC resolution when the gain set is incremented, two different techniques can be applied.

5.1 Vary Gain Set Increase

The test evaluation circuitry allows an increase in the gain set by 1 to 7. For the demonstrator design, the ADC resolution is 21mV while the increase at the AGC output for a gain set increment is approximately 15mV. Simulations have shown that setting the gain step increase (*GI*, Figure 3) to 2 allows testing for minimum gain step sizes. In this case, the gain set is increased from 0 to 30 and in a second run from 1 to 31. For both test evaluations the test signature (*L*) has to be equal to 15. An alternative technique is the manipulation of the AGC reference voltage.

5.2 Increasing AGC Output Swing

As described above, the change at the AGC output for an increment in the gain set is smaller than the ADC resolution. Reducing the AGC reference voltage can decrease the output of the AGC for the lower gain set. A proper selection of the reference and the DC input voltage results in an AGC output that covers most of the ADC input range when the gain set is increased form 0 to 31. As a result, the AGC output increases by more than 30mV for each gain set increment.

As illustrated in Figure 5, an adequate selection of DC input and reference voltage maximises the AGC output voltage range and keeps the ADC input within the input range for offsets up to 30mV. For the demonstrator design this corresponds to an offset of approximately 8mV at the AGC.

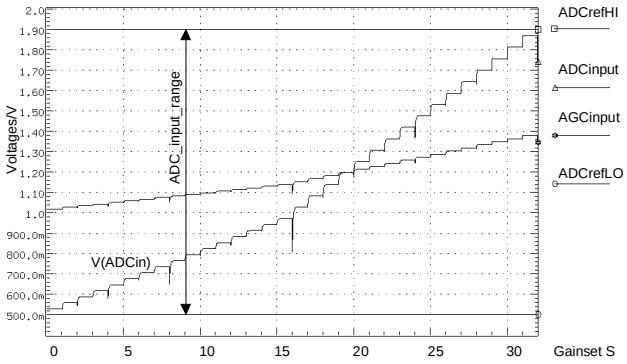

Figure 5: Increased AGC output swing

6 Design & Simulation Results

The test evaluation circuitry has been designed in a 0.8µm standard CMOS process. The abstract layout, showing the interconnects without the gate layouts, is given in Figure 6; the structure contains 453 gates.

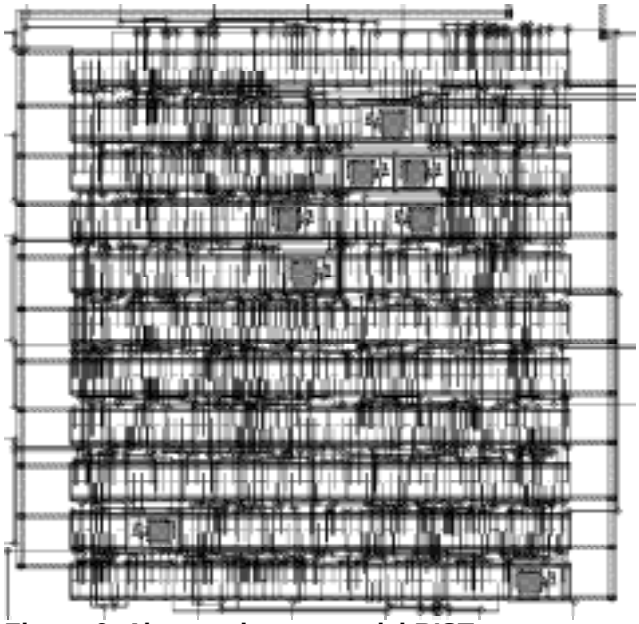

Figure 6: Abstract layout partial BIST structure

The area overhead for the partial BIST structure can be reduced if the 12 bit buffers, register, adder and comparator are reduced in size according to the required precision.

For the simulation of the partial BIST structure, a simple AGC and ADC behavioural model has been generated. The clock frequency has been set to 20MHz.

6.1 Gain Step Size Test

The partial BIST circuitry has been verified by simulating the minimum gain step size test for various settings, while the AGC output swing has been increased by the technique described in section 5.2.

Initial simulations have been performed without any noise effects. The number of ADC output codes to sample has been set to 16, 32 and 64, while the minimum sample difference was initialised to 16, 32 and 64, respectively. This means that a test signature (L) of 32 indicates that all gain steps caused the average ADC output to increase by 1 at minimum.

Offset effects have been simulated and have verified the statement given in section 4.1. An offset voltage at the AGC that drives the AGC output outside the ADC input range for the lowest (or highest) gain set causes a test signature below 32. Thus the DC input and the AGC reference voltage can be determined in such a way that an out of tolerance offset causes a test failure.

A noise signal has been added to the ADC input signal with a maximum amplitude of 15mV (3/4 LSB). Keeping the threshold for the minimum sample difference at 16, 32 and 64, respectively, causes test failures. If a sample contains 64 ADC output codes, a test threshold of 50 has to be used to pass the test. This means that the average ADC output increased at minimum by 0.8LSB when the gain set was incremented. With a decreasing number of ADC outputs to sample, the test threshold becomes wider. However, it has to be pointed out that the noise characteristics depend on the AGC and ADC, thus the test thresholds and the number of ADC outputs to sample have to be determined by estimating the noise effects for each design separately.

The partial BIST structure can easily be enhanced to provide failure diagnosis facilities. The test routine can be stopped as soon as one gain step size is outside the tolerance window. The values for the samples G and H can then be read if the 12 bit buffers (Figure 2 & 3) are embedded in a scan chain.

For the demonstrator design the test time (64 codes summed) will be approximately 20 µs (2048 clock cycles), plus initialisation time. Currently the gain step size test takes several hundred milliseconds, due to the time consuming capturing of data to perform a FFT off-chip. The entire test time for the analogue circuitry can be reduced by 70%.

6.2 Ramp Test

For the ramp test, the gain set is kept constant at 31, and 64 samples are taken for each time slot (see section 4.2). To avoid timing and synchronisation problems between the digital test evaluation circuitry and the analogue input stimulus, the BIST structure can be activated and a ramp stimulus applied that begins and ends outside the ADC input range. Figure 4 illustrates the ramp test where the AGC output is within the ADC input range for 8 time slots. By selecting a ramp stimulus that exceeds the input range by ±30mV (*Vos* in Figure 4) offset effects can be eliminated. Simulations, taking noise effects into account, have been carried out for ramp stimuli covering 8, 16, and 32 time slots, respectively. The obtained test signatures L_{pass}, the ideal differences in the average ADC output $\Delta f_{I,I-1,ideal}$, and the minimum difference $\Delta f_{I,I-1,thres}$ tested for are summarised in Table 2. Simulations for 32 time slots indicated that a threshold of 1.5 LSBs is too tight and causes faulty signatures (L below 31).

#time slots	$\Delta f_{I,I-1,ideal}$	$\Delta f_{I,I-1,thres}$	L_{pass}
8	8 LSB	6 LSB	7 & 8
16	4 LSB	3 LSB	15 & 16
32	2 LSB	1 LSB	31 & 32

Table 2: Ramp test simulation results

A faulty test signature L can be caused by:

L=0:
- AGC output outside of ADC input range
- AGC output is stuck at voltage
- Or the AGC (or ADC) gain is far too low

$0<L<L_{pass}$:
- AGC output covers subsection of input range only
- Or AGC (or ADC) gain is too high

$L>L_{pass}$:
- AGC (or ADC) gain is too low

For the demonstrator design the test time (64 samples, 16 time slots) will be approximately 10 µs (1024 clock cycles), plus initialisation time.

7 Conclusions

A partial BIST structure has been designed to implement on-chip test evaluation for an AGC gain step test and the verification of the AGC output voltage swing. This study has shown that digital solutions to partial self-test are feasible for circuits of this type and that in many cases reconfiguration of digital control loops may well be a highly optimal DfT enhancement.

The AGC gain step and ramp test can be implemented at the macro level using digital logic only and hence will require minimal design effort if synthesis techniques are used. This solution has been shown to improve test time by up to 70% without any degradation in fault coverage. Where the proposed solution is implemented in parallel with careful design for fault tolerance, very high fault coverage is feasible. Future research will address enhancements for test diagnosis and the extension of this structure to a full BIST (including dynamic tests) with capabilities for ADC testing.

Finally it should be noted that this study has identified further the need for a test support environment compatible with mixed signal design tools to support both DfT optimisation and efficient optimisation of test strategies. This will be particularly important for designers of mixed signal intellectual property and cell libraries for use in systems-on-silicon, as the trend is for more efficient and higher quality macro test [9].

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