SPECIAL SESSION
Virtual Socket Interface Alliance

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1 VSI Builds Momentum to Solve Design Reuse Imperative

(Larry Rosenberg, Chair, VSI Technical Committee, USA)

For over twenty years now, alarmists have been warning the electronics industry of an emerging “design productivity gap”. This is based on the exponential growth of silicon implementation capacity - which grows at a compound annual growth rate of over 58% per year. This should be compared to the most optimistic projection for productivity growth, which is around 23% per year. Hence, there should have been an exponentially growing gap between what silicon can hold and what designers can define into the silicon.

This tutorial will explain in detail how the semiconductor/EDA industries have coped with this problem up to now - and why the techniques that have served us so well for over 30 years, will no longer work in the future. In addition, silicon capacity finally has reached the point where true product convergence can occur i.e. complete designs comprising disparate technical domains can be merged onto a single System-Chip (SoC). The solution to both the “design productivity gap” and the “convergence challenge” can both solved by design reuse of Virtual Components. This is the vision on which the VSI Alliance was created.

2 The VSI System-Level Perspective on the mix and match of Virtual Components

(Mark Genoe, Chair SLD DWG of VSI, Alcatel, B)

Reuse of Intellectual Property (IP), or Virtual Components (VCs), from different sources in Systems-on-Chip, allows companies to focus the R&D to their own core competencies. The complexities of future systems-on-chips will largely exceed the ones that we know today at a board. Therefore, it will be required to model, analyze, debug and validate such system chips and all their interfaces before processing the real silicon. This is what is meant today with 'Virtual Prototyping'. Virtual prototyping of complete hardware (HW) - software (SW) systems is really key, but need to be raised to much higher levels of abstraction than today's design practices. This shift will result in totally new system level design environments to capture requirements, to specify functionality and architectures, to explore different mappings and schedulings, to select and encapsulate reusable Virtual Components.

To be used at 'system level', Virtual Components require several abstract models. It is exactly the goal of the System Level Design (SLD) Development Working Group (DWG) of the VSI Alliance. As a first result, the DWG has defined a system-level model taxonomy together with a classification of system, architectural, hardware and software models, used at different abstraction levels in system design. The design methodology which is promoted is based on a clear separation of the VC functionality and the VC interface. Therefore, the DWG is establishing a well-defined hierarchical and multi-level standard description of VC interfaces, covering abstract transactions down to detailed component protocols, implemented in hardware and/or software.

3 Introduction to Virtual Component Interface

(Graham Matthew, STMicroelectronics, UK)

The charter of the VSI OCB (on-chip bus) working group is to define a family of Virtual Component Interfaces (VCI) to facilitate communication between Virtual Components (VCs) assembled on a single semiconductor device. There is a need to integrate components which have been designed for different processor families.

A layering scheme based on the OSI Reference model is used as a framework for abstracting from particular bus protocols. This fits in with the more general interface-based layering scheme being defined by the VSI SLD. The Virtual Component Interface is seen as a family of interfaces which support a Bus Transaction Layer.

Systems are first decomposed into modules which communicate using a generic set of transactions. A second stage of decomposition maps the VCI onto a particular on-chip interconnect. An overview of the VC interface signals and protocols will be given.

An example of comparing the VCI against a standard on-chip bus will therefore be used to show how an existing bus maps to the more abstract concepts introduced at the Transaction Layer, while a second example shows how the more advanced features of the VCI can be used to support higher performance interconnect schemes.