

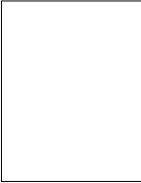


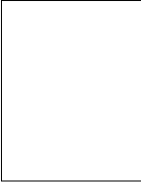


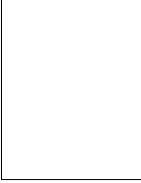


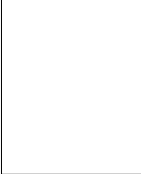

*Conference Committee (continued)*

	<b>Programme Support</b> Pierre Plaza		<b>Americas' Representative</b> Tony Ambler		<b>Eastern Europe Representative</b> Marta Rencz
	<b>General Chair Support</b> Kees Schot		<b>Asian Representative</b> Takayuki Yanagawa		<b>Russian Liaison</b> Alexander Stempkovsky

**Programme Topic Co-Chairs**

	<b>System Design</b> Wolfram Glauert		<b>System Design</b> Flavio Wagner		<b>Embedded Systems</b> Jean-Paul Calvez
	<b>Embedded Systems</b> Nikil Dutt		<b>HW/SW Co-Design</b> Klaus Buchenrieder (with Rolf Ernst)		<b>Microsystems</b> Klaus Mueller-Glaser (with Bernard Courtois)
	<b>Architectural Synthesis</b> Fadi Kurdahi		<b>Architectural Synthesis</b> Ahmed Jerraya		<b>Mixed Signal</b> Georges Gielen
	<b>FSM Synthesis</b> Michel Berkelaar		<b>Formal Verification</b> Carlos Delgado Kloos		<b>Low Power</b> Jacques Benkoski (with Wolfgang Nebel)

*Programme Topic Co-Chairs (continued)*

	<b>Physical Design</b> Erich Barke		<b>Physical Design</b> Bernd Schuermann		<b>Test Programs</b> Joan Figueras
	<b>Test Programs</b> Christian Landrault		<b>Simulation</b> Peter Schwarz		<b>Simulation</b> John Forrest
	<b>Testability</b> Einar Aas		<b>Unit Testing</b> Rene Segers		<b>HDL Design</b> Wolfgang Ecker
	<b>VHDL</b> Eugenio Villar		<b>Design Re-Use</b> Ralf Seepold (with Jim Heaton)		<b>ASIC &amp; ASIP Design</b> Yervant Zorian (E)

## Vendors Committee

Hanns Windele  
Catherine Weiss  
Irene McCarty  
Mike Northwood  
Hans Detlef Boesch  
Hein Van Der Wildt  
Shubha Shukla

*NB Members of more than one committee are only pictured once with indication of other contributions*

*(E) Event Steering Board (C) Conference Committee (T) Topic Chairs  
(P) Technical Programme Panels (V) Vendors Committee*