Highly Testable and Compact 1-out-of-n Code Checker with Single Output*

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Abstract

This paper presents a novel 1-out-of-n checker that, compared to the other implementations up to now presented, features the advantages of: i) satisfying the TSC or SCD property with respect to all possible internal faults representative of realistic failures; ii) presenting a single output line; iii) requiring significantly lower area overhead.

1. Introduction

Enhanced reliability is becoming a requirement for an always wider spectrum of computer applications, varying from space and avionic, to telephone switching networks, on-line transaction processing, etc. A common strategy to satisfy this need is to perform concurrent error detection by Self-Checking (SC) circuits, followed by recovery.

Since it has been estimated that more than half of all computer failures is caused by faults in RAMs, several studies have been devised to the design of self-checking and fault-tolerant RAMs [1]. A common cause of RAM failures is the occurrence of faults in the address decoder, resulting in the inability to access some portions of the memory array, or in the access of incorrect portions.

Address decoders'outputs are typically encoded by 1-out-of-n codes[1]. Thus, a SC decoder can be obtained by properly designing its functional block and using one or more (depending on the adopted decoding scheme) suitable 1-out-of-n (1/n) checkers. Consequently, several papers have been specifically devised to the design problems of 1/n checkers ([2, 3, 4] are some examples).

None of the proposed 1/n checkers has been shown to satisfy either the Strongly Code-Disjoint (SCD) [5] or the Totally Self-Checking (TSC) [6] property with respect to all its possible internal faults representative of realistic failures (i.e. all internal node stuck-ats, transistors stuck-on, transistors stuck-open and resistive bridgings).

Moreover, all the proposed 1/n checkers present two output lines. Instead, the availability of single output checkers would feature several advantages over that of only double-railed output ones [7, 8]. Moreover, the single output could be required for the checkers to be used in applications with constrained number of input/output terminals.

2. The proposed checker

The single output 1/n checker here proposed is shown in Fig. 1,where we have denoted by: i) $(X_1, ..., X_n)$, the checker input word; ii) Z, the checker single output; iii) G_S and G_M, the conductances of the transistors; iv) CK, the system clock signal.

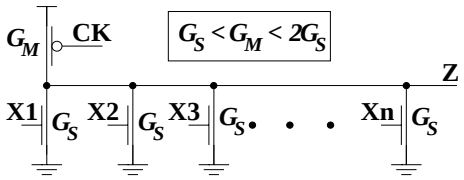

Figure 1. Electrical structure of the proposed single output 1/n checker.

We assume that the checker inputs can be considered stable for the whole CK period, or additional flip-flops (with clock signal equals CK) are inserted at the checker input.

Under the design constraints in Fig. 1, it can be easily verified that when the input word belongs to the 1/n code, the proposed circuit gives at its output: i) a high logic value, when CK=0 (charge phase, *CP*); ii) a low logic value, when CK=1 (discharge phase, *DP*). Instead, if the input word does not belong to the 1/n code, the proposed circuit produces at its output: i) a low logic value during both *DP* and *CP*, if

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[1] 1-out-of-n codes are codes whose codewords consist of only 1 bit (out of n) with high logic value.

X_i = 1 *for at least two* i ($i = 1, ..., n$); ii) a high logic value during both *DP* and *CP*, if X_i = 0 $\forall$ i ($i = 1, ..., n$).

Consequently, supposing that Z is checked at the end of both *CP* and *DP*, this circuit implements a single output $1/n$ checker. In particular, indications of correct operations are recognized if the logic values present at the checker output at the end of *CP* and *DP* are different, while the presence of equal logic values is interpreted as error indication.

In particular, Z can be checked by a flip-flop using a clock signal equal to CK (and suitably delayed to account the checker input/output delay and the flip-flop setup time), and sampling Z on both the clock rising and falling edges.

Of course, as in the fault-free case Z assumes both high and low logic values, both stuck-at 0 and stuck-at 1 faults affecting Z can be revealed. Moreover, if CK is stuck-at, the checker gives an output error message.

The behavior of our checker has been verified by means of conventional and Monte Carlo electrical level simulations, supposing uniform distribution of all electrical parameters. We have found that, in case of nominal values of the circuits' electrical parameters, the worst case condition noise margins equal 1V (with V_{DD} = 5V). Moreover, our checker can well tolerate variations of all electrical parameters up to 10%.

3. Testability Analysis

We have considered a realistic set of checker internal faults composed of all possible: 1) node stuck-ats (SAs); 2) transistors stuck-on (SONs); 3) transistors stuck-open (SOPs); 4) resistive bridgings (BFs), with values of connecting resistance in the range $[0, 6k\Omega]$, thus representative of realistic failures [9].

Moreover, we have considered the fault hypotheses typically assumed for SC circuits.

We have verified that our checker is TSC with respect to all possible SAs, SOPs, SONs, and TSC or SCD for all possible BFs with values of connecting resistance $\in [0, 6k\Omega]$.

As previously introduced, no $1/n$ checker has yet been presented which has been verified to satisfy the TSC or the SCD with respect to all possible SAs, SOPs, SONs, BFs.

4. Comparison with other implementations

Our checker has been compared, from area overhead, on-line self-testing ability and power consumption points of view, with the double-railed output $1/n$ checker presented in [4] which, in turn, had been verified featuring the highest on-line self-testing ability and the most compact structure over alternative double-railed output solutions.

Assuming the transistor count as a rough estimate of area overhead, our single output implementation enables a relative area reduction A = 100 $\times$ (n+1)/(2n+2). For instance, for n=256, A = 50%.

As previously stated, our single output checker is TSC with respect to all possible SAs, SONs, SOPs, and TSC or SCD with respect to all BFs. Thus, it features higher on-line self-testing ability than that in [4], which is neither TSC, nor SCD with respect to all its possible SOPs.

As for power consumption, considering as example CK frequency = 250MHz, n=16, and capacitive load = 0.1pF, we have verified that our checker allows a reduction of the average power (including also that due to CK) $\simeq 65\%$ compared to [4] (whose static power consumption had been shown [4] to be fully compensated by a significant reduction of dynamic power with respect to alternative solutions).

5. Conclusions

This paper has presented a novel $1/n$ checker with single output, which can be used for any value of n.

Compared to the other available checker implementations, that here proposed features the main advantages of: i) being TSC or SCD with respect to all its possible, internal faults, representative of realistic failures; ii) presenting a single output line; iii) requiring lower area.

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