

# Constraints Space Management for the Layout of Analog IC's

Bogdan G. Arsintescu, Ralph H.J.M. Otten  
Delft University of Technology  
Mekelweg 4, 2628CD Delft, The Netherlands  
Bogdan, Otten@CaS.ET.TUdelft.nl

## Abstract

*An automated technique to narrow down the number of parameters for linear constraint transformation models of analog circuits is described. The sets of more important circuit parameters and specifications are confined in an efficient constraint transformation model. The method is based on least square approximation and principal component analysis of the sensitivity matrix of the transformation. The resulting model encompass the constraints confined using designers' expertise for approximated circuit calculations.*

## 1 Introduction

Analog design is known to be highly dependent on layout induced parasitics. The extreme criticality of analog circuits and the difficulty to meet the specifications is generally the source of long design iterations and multiple fabrication runs. Recently, a number of attempts have been made to cope with this problem. The common denominator of the proposed approaches is the use of a top-down design methodology [1] to ensure that high-level specifications be translated hierarchically onto module parameters and finally onto a suitable layout through a mechanism, known as *constraint transformation*. At each level of hierarchy all pertinent constraints are then enforced by a *constraint-driven tool-set* [2].

For analog linear circuits, constraint transformation and generation methods based on parasitic bounding and degradation evaluation were proposed in [3, 4]. These methods use circuit sensitivities to define a linear model of the circuit. However, the models created are over-defined, due to (1) the correlation between the circuit specification and (2) the very low influence of a subset of circuit parameters considered. To make the transformation efficient, these methods rely on heuristics or user interaction to select the more important constraints, critical for constraint generation.

In this paper a systematic method for automatic selection of the more important circuit specifications and parameters with respect to a linear transformation model between these sets is proposed. The target of the method is to determine a set of low-level

parameters that induce the larger specification deviation of the more important uncorrelated high-level constraints, discarding the ones with little or no influence. The method presented reduces the search space for the design tools by finding the active constraints with respect to the constraint transformation. This increases the chance that a constraint-driven optimization can be achieved without iterations.

## 2 Method description

Analog AC constraint transformations uses a linearization of the circuit around the nominal working point based on sensitivity analysis. Following the notations introduced in [2], for a given circuit with performance vector  $[\mathbf{K}] \in \mathbb{R}^n$  and parameter vector  $[\mathbf{P}] \in \mathbb{R}^m$ , a  $n \times m$  sensitivity matrix  $[\mathbf{S}]$  is found s.t.  $[\Delta\mathbf{K}] = [\mathbf{S}] \cdot [\Delta\mathbf{P}]$ . The model reduction problem should confine the more important specifications and parameters for the purpose of creating an efficient model. The efficient model should contain only those variables or equations which are necessary and sufficient for the model:

**Problem 1 Model Reduction Problem:** *For a given linear approximation  $[\Delta\mathbf{K}] = [\mathbf{S}] \cdot [\Delta\mathbf{P}]$  of a circuit, find the necessary and sufficient specification subset  $[\mathbf{K}']$ , the parameters subset  $[\mathbf{P}']$  and their corresponding sensitivity matrix  $[\mathbf{S}^\diamond]$  which approximates the model with a maximum error  $\varepsilon$ :*

$$[\mathbf{K}'] = [\mathbf{S}^\diamond][\mathbf{P}'] + \varepsilon \quad (1)$$

The reduced model is obtained as follows. By means of least squares approximation, the initial sensitivity matrix is reduced to one with the rows corresponding to the principal circuit functions  $[\mathbf{K}']$ . These circuit functions are more sensible to parameter change. Subsequently, the more important circuit parameters that will create a change in the circuit functions are selected. That is, a column subset of the sensitivity matrix is moved in the "noise" space of the transformation, to obtain a reduced and efficient model. A good approximation of the transformation sensitivity matrix is therefore obtained with a set of principal circuit functions with respect to the more important circuit parameters.

In order to be able to compare the influences of the high-level constraints, they must be uncorrelated. For

this purpose, a singular value decomposition (SVD) [5] of the sensitivity matrix  $[\mathbf{S}]$  is computed:

$$[\mathbf{S}] = [\mathbf{U}][\Sigma][\mathbf{V}]^*, \quad (2)$$

where  $[\Sigma] = \text{diag}\{w_1, \dots, w_r, 0, \dots\}$  and  $r \leq \min(m, n)$  is the rank of the matrix.

To select the important circuit functions, ordered monotonic by importance, the sensitivity matrix  $[\mathbf{S}'] = [\mathbf{U}'][\Sigma'][\mathbf{V}]^*$  is obtained by least square approximation with the first  $k$  singular values of the SVD,  $[\Sigma'] = \text{diag}\{w_1, \dots, w_k, 0, \dots\}$ . The approximation error is equal to the first singular value zeroed,  $w_{k+1}$ :

$$\|[\mathbf{S}] - [\mathbf{S}']\| = w_{k+1}. \quad (3)$$

Hence, the first  $k$  performance functions  $[\mathbf{K}']$ , corresponding to the rows in  $[\mathbf{U}'] = \{U_1, U_2, \dots, U_k\}$ , are to the more important circuit functions with respect to the linear transformation.

The columns of  $[\mathbf{S}']$  still represent all  $m$  initial circuit parameters that can influence the circuit behavior. In order to find the more important parameters with respect to the transformation, a subset from the columns of the unitary matrix  $[\mathbf{U}']$  is selected. Firstly, the column vectors of  $[\mathbf{U}']$  are permuted in increasing energy order  $\|U_j\|^2 = \sum_{i=1}^k u_{ij}^2$ . Subsequently, the column vectors below an energy threshold  $\delta$  are moved in the noise space of the transformation, zeroing the corresponding columns in  $[\mathbf{U}']$ :

$$\|u_i\|^2 \leq \delta \Rightarrow u_i \in [\mathbf{U}^n], \quad [\mathbf{U}'] = [\mathbf{U}^\circ] + [\mathbf{U}^n]. \quad (4)$$

where  $[\mathbf{U}^\circ]$  creates the space of “interesting” signal (strong components) and  $[\mathbf{U}^n]$  is the space of noise (weak components). The approximated sensitivity matrix  $[\mathbf{S}']$  becomes as a sum of the matrix  $[\mathbf{S}^\circ]$  corresponding to the critical space of the transformation model and the matrix  $[\mathbf{S}^n]$  of the noise parameters with respect to the vector of circuit specifications  $[\mathbf{K}']$ :

$$[\mathbf{S}'] = ([\mathbf{U}^\circ] + [\mathbf{U}^n])[\Sigma'][\mathbf{V}]^* = [\mathbf{S}^\circ] + [\mathbf{S}^n]. \quad (5)$$

The maximum error made by approximating  $[\mathbf{S}']$  with  $[\mathbf{S}^\circ]$  yields:

$$\|\mathbf{U}' - \mathbf{U}^\circ\| = \|\mathbf{U}^{\text{noise}}\| \leq \delta \cdot (m - m^\circ), \quad (6)$$

where  $m^\circ$  is the number of non-zero columns in  $[\mathbf{U}^\circ]$ , that is, the dimension of the important parameter subset  $[\mathbf{P}']$ . The total error for obtaining the matrix  $[\mathbf{S}^\circ]$  corresponding to the set of the more important  $k$  circuit specifications with respect to  $m^\circ$  more important circuit parameters yields from Equations (3,6):

$$\varepsilon \leq w_{k+1} + \delta \cdot (m - m^\circ). \quad (7)$$

The main advantage of the method is that one can derive tighter local constraints for the circuit speci-

fications and parameters in the reduced model and more relaxed general constraints. This will reduce the search space of the optimization tools used in constraint driven design and reduce the number of iteration necessary to reach a feasible solution.

### 3 Results and Conclusions

In this paper an original method for critical constraints characterization of analog circuits constraint transformations is described. Using sensitivity analysis and principal component analysis by means of singular value decomposition, a set of constraints that induce the larger specification deviations is found. Several circuits were tested with this constraint space management method [6]. The set of constraints obtained includes the set selected by experienced analog circuit designers in state-of-the-art manual design. The method described in this work can discover as well groups of constraints for local and hierarchical optimization. Hence, the method automates the circuit approximation techniques for constraint driven optimization, defining an efficient model for the constraint transformation.

The major advantage of the method is that a set of *local constraints* is obtained through which the layout can be optimized very much like designers’ art. Automated methods usually tend to deal with the constraints globally and to enforce constraints for devices and nets were they are not necessary.

The method was implemented and is included in an analog layout framework in development at Delft University of Technology and Delft Institute for Microelectronics and Submicron Technology (DIMES).

### References

- [1] H. Chang, et al. *A Top-down, Constraint-Driven Design Methodology for Analog Integrated Circuits*. Kluwer Academic Publ., Boston, MA, 1996.
- [2] E. Malavasi, E. Charbon, E. Felt, and A. Sangiovanni-Vincentelli. Automation of IC Layout with Analog Constraints. *IEEE Trans. on CAD*, 15(8):923–942, 1996.
- [3] U. Choudhury and A. Sangiovanni-Vincentelli. Automatic Generation of Parasitic Constraints for Performance Constrained Physical Design of Analog Circuits. *IEEE Trans. CAD*, 12(2):208–224, 1993.
- [4] C. A. Makris and C. Toumazou. Analog IC design: Part II - Automated Circuit Correction by Qualitative Reasoning. *IEEE Trans. on Computer Aided Design, CAD-14(2)*:239–254, February 1995.
- [5] R. H. Golub and C. F. Loan. *Matrix Computations*. John Hopkins University Press, 1996.
- [6] B. G. Arsintescu and R. H. J. M. Otten. Constraints Space Management for the Layout of Analog ICs. Technical Report, TU Delft, 1996. <ftp://cas.et.tudelft.nl/pub/bogdan/forces.ps.gz>.