IOCIMU - AN INTEGRATED OFF-CHIP I_{DDQ} MEASUREMENT UNIT

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Abstract

The implementation of an Off-Chip I_{DDQ} monitor to support the test of complex ASICs is presented in this paper. The monitor can be incorporated into a standard automated test equipment (ATE). It is capable of driving a 2µF capacitive load and can perform measurements of the I_{DDQ} of a device under test (DUT) in the 0-1mA range. According to measurements the monitor can operate at the test rates up to 30kHz and offers an resolution better than 0.1µA. The on-chip integrated bypass switch is capable of handling DUT transient currents up to several amps. The IOCIMU prototype was fabricated in the 2-µm Mietec BiCMOS technology and has an active chip area of 20 mm^2.

1. Introduction

I_{DDQ} testing is useful to detect physical defects, such as gate-oxide shorts and bridging defects, which result in an increase of the quiescent current consumption of the affected circuit. It is widely used as a supplement to the functional tests to enhance the test quality. The effectiveness of the I_{DDQ} tests depends mostly on the number of measurements carried out, which is related to the test rate possible, and the accuracy of the current measurement itself.

The development of I_{DDQ} measurement hardware has been intensively treated by research groups during the last years, and it is now becoming either commercially available as add-on units, or as an ATE option. Most of the existing monitors are designed using discrete components. Their realizations differ in the performance and circuit complexity [1]. The power supply pins of the DUT are always loaded by a decoupling capacitance C_{DEC}, which delivers the transient current to DUT and minimizes the supply wiring effects. Complex ASICs often feature multiple supply pins, resulting in a high total C_{DEC} value (100nF/pin). An integrated I_{DDQ} monitor can be placed on the test board close to the DUT and hence C_{DEC}, which loads the monitor and slows down the measurement, can be minimized. A first attempt to design a monolithic monitor implementation was done at Philips. However, their IDUNA-2 monitor was designed to test a specific class of circuits, featuring a good performance but only for a small C_{DEC}. This contribution demonstrates the feasibility of an integrated general-purpose I_{DDQ} monitor, the IOCIMU prototype, implemented in a standard BiCMOS technology.

2. IOCIMU Architecture

The architecture of IOCIMU has evolved from its discrete predecessor, the OCIMU. Several of the improvements are based on practical experiences gathered with the discrete POCIMU and DOCIMU [1] monitors. The IOCIMU is designed as a semi-digital monitor featuring 3 analog (Vdd-dut, DUT, Vpf), 2 digital (Trig. P/F), and 2 power supply pins. The monitor is to be inserted between the positive power supply and the DUT. The hierarchical structure is illustrated in Figure 1.

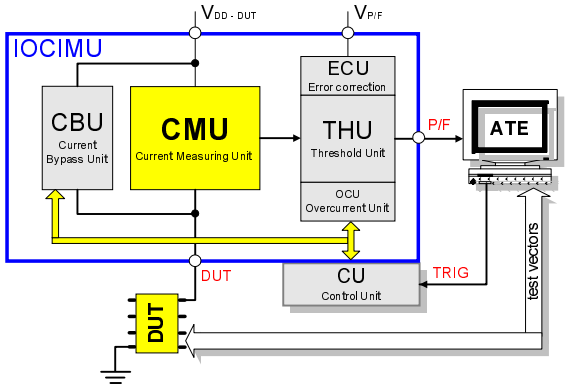

Fig. 1: IOCIMU architecture and application

The main part of the monitor is the current measuring unit CMU, which performs the current sensing and pre-processing. The Vdd-dut pin is the reference for the DUT power supply voltage, which is stabilized and supplied to the DUT output pin. The measured I_{DDQ} current is converted to a voltage and amplified. The threshold unit THU compares the resulting voltage V_{IDDQ} with the reference pass/fail level V_{PF}, which is equalized by the error cancellation unit ECU. The output pass/fail flag P/F is the result of the comparison. There are also three

supplementary units: the control (CU), the current bypass (CBU) and the overcurrent (OCU) unit. The control unit is the interface to the ATE or to other test equipment, which controls the operation of the monitor. It has not been integrated in the first IOCIMU prototype to allow full external control of all monitor functions. The main purpose of the CBU is to bypass the monitor during changes in the DUT current when a new test vector is applied. It offers a channel to supply the transient current to the DUT, providing also the reference voltage Vdd-dut to the DUT supply pin. If required, the CBU can steadily bypass the I_{DDQ} monitor without the need for any additional external reconfiguration circuits. The OCU is activated when the output of CMU OA is approaching saturation and it temporarily supplies the overcurrent to the faulty DUT. A simplified monitor circuit diagram is shown in Figure 2.

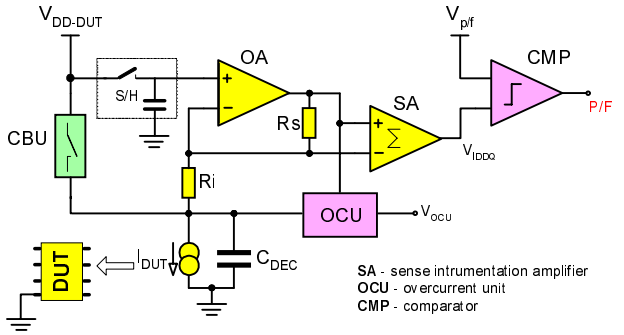

Fig. 2: Simplified monitor structure

The measuring period is initiated by the trigger signal TRIG, which when active enables the CBU. When the CBU is turned off, the CMU is activated to perform an accurate I_{DDQ} measurement and the monitor outputs the pass-fail flag P/F.

3. Implementation and Measurement Results

The monitor is designed for a maximum power supply voltage of 15V and to operate at a test rate of 10kHz. The fabricated prototype configuration has been chosen so that it allows full user control and access. An external low-pass filter and a feedback resistor in series with DUT were added to the IOCIMU for measurement purposes. The monitor features an excellent performance for I_{DDQ} currents in the range from 0 to 1mA, a decoupling capacitance between 20n and -2µF, and for DUT supply voltages Vdd-dut in the range of 0.5 to-7.5V. A maximum test rate of 30kHz, with a resolution 0.25µA has been reached for a decoupling capacitance Cdec of 0.1µF. A resolution better than 0.1µA can be reached if the monitor's load capacitance is less than 200nF and the test rate is less than 5kHz. The resolution measurements were done using a 12-V monitor power supply voltage and at 5-V DUT supply voltage Vdd-dut. The resolution of the IOCIMU in function of the test rate f and the decoupling capacitance Cdec is shown in Figure 3.

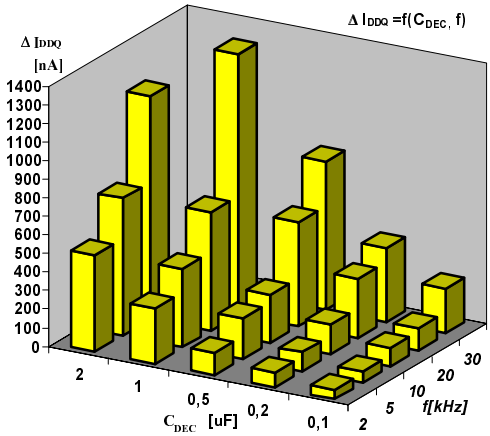

Fig. 3: IOCIMU resolution

The IOCIMU off-chip I_{DDQ} monitor is implemented and fabricated in the 2-µm Mietec BiCMOS technology using the Europractice MPC services. The active area of the circuit occupies 20 mm^2. The microphotograph of the IOCIMU die is shown in Figure 4.

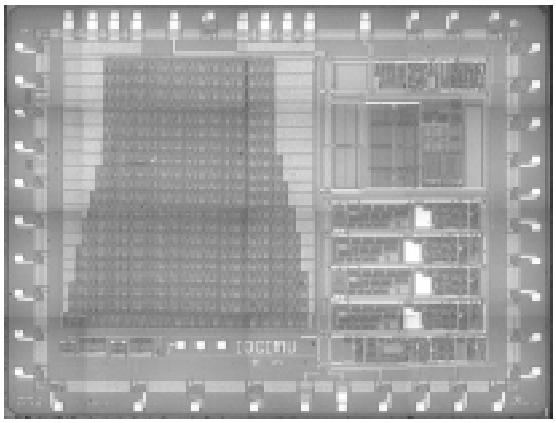

Fig. 4: Microphotograph of the IOCIMU

The IOCIMU ASIC prototype is intended to verify the feasibility of monolithic implementation of a general-purpose off-chip I_{DDQ} monitor. According to measurement results, the typical IOCIMU resolution at the test rate 10kHz and the decoupling capacitance of 1µF is better than 1µA.

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4. References

[1] B. Straka, H. Manhaeve, J. Vanneuville, M. Svajda " A Fully Digital Off-Chip I_{DDQ} Measurement Unit ", accepted to DATE 98 conference, Paris, France,