Core Interconnect Testing Hazards

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Summary

The SIA Roadmap [1] predicts a very aggressive path of technologies from 0.35 μm technology design to 0.10 μm technology design. Increasing frequencies together with decreasing geometries lead to a number of issues which need to be examined. Testing is clearly one main issue. Another area of concern is that of signal integrity of the interconnects.

The interconnects must not only be analyzed with regard to opens and shorts but also with regard to the signal delays. Up to now, opens and shorts in bus systems on boards have been tested using boundary scan, mostly neglecting delay test. In addition, it has to be considered that the signal delay (i.e. the time when the signal crosses the switching threshold of the following gate) on a certain line within a bus system depends on the set of input signals of all bus lines. Furthermore, hazards can occur due to coupling between bus lines which can lead to an incorrect function of the whole circuit.

Different interconnect systems with different test patterns have been analyzed and the results for 0.10 μm technology will be given. The geometric data for the interconnects in 0.10 μm technology has been derived or directly extracted from the SIA-Roadmap. With this data the line parameters for the simulation of the interconnects have been calculated with the help of a tool which takes into account conducting subtrates. For the analysis of the interconnects we used a time-domain simulator for lossy coupled lines which takes into consideration wave propagation effects [2].

With the help of an examplary geometry with five metal layers we examined how scaling in deep submicron affects the quality of signals. The geometric data for the different technologies has been derived or extracted directly from the SIA Roadmap (see table 1).

technology	**0.35µ**	**0.25µ**	**0.18µ**	**0.13µ**	**0.10µ**
line width µm	≥0.8	≥0.6	≥0.44	≥0.3	≥0.22
spacing µm	≥2.0	≥1.5	≥1.1	≥0.75	≥0.55
line height µm	1.2	1.2	1.1	0.9	0.77
oxide µm	7.9	7.9	7.2	6.0	5.6
epitaxy µm	3.0	2.0	1.4	1.0	0.8
substrate µm	400	400	400	400	400
freq. Mhz	333	500	666	900	1100
V_{DD} V	3.3	2.5	1.5	1.35	1.2

Table 1 Geometric data from SIA Roadmap

In the first step, we extracted the transmission line parameters (resistance, inductance, capacitance and admittance per unit-length) using a tool developed in our institute [3] which is based on a two-dimensional quasi-analytical formulas while the cross-sectional geometry is assumed to be homogeneous along the lines. This tool takes into account lossy substrates. For random samples, the results have been verified with the help of a finite-element field calculation program. All cross-sectional information about a particular line system (material, geometry, return-path of the current) is contained in these per-unit-length parameters.

In the second step, we simulated different line systems with different driver resistances and load capacitances for the technologies given in table 1 for three different sets of input signals. In the first case, the outside lines are fixed to ground and the middle line changes from low to high. In the second case, all lines switch in the same direction (even mode), and in the third case, the middle line switches against all other lines (odd mode).

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The driver resistances are Z_D = 50 Ohm and the output capacitances decrease from C_L = 0.05 pF for 0.35 μm technology to C_L = 0.01 pF for 0.1μm technology.

We examined the effects of signals propagating along a 9-line system located in metal 5 which is suited best for busses since it displays the lowest resistivity.

The interconnects have been analyzed in view of the signal delay. The delay of a certain line within a bus system depends on the set of input signals of all bus lines. The signal travels on a line with its intrinsic delay when only this certain line is switched and all the other lines are quiescent. The intrinsic delay is used as a reference. In the even mode all bus lines switch in the same direction which may lead to a minimum delay (shorter than the intrinsic delay) whereas in the odd mode the middle line switches against the outer eight lines resulting in a maximum delay which can be much longer than the intrinsic delay. Fig. 1 illustrates the dependency of the signal delay from the set of input signals.

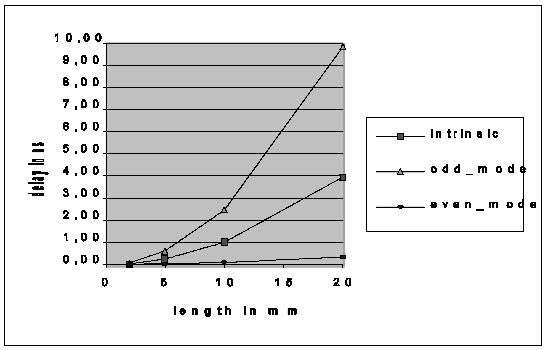

Fig. 1 Signal delay for different sets of input signals in 0.10 µm technology

Furthermore, we have done a number of simulations with odd mode input signals with the center line changing within realistic delays earlier and later relative to the outside eight lines, i.e. the falling edge of the middle line occurs within 500ps earlier or later than the rising edges of the outer lines in order to determine the worst delay. The signals at the ends of the middle line of a 2mm and of a 10mm line system are shown in the figs. 2 and 3.

For a 2mm line system the signal delay is increased and hazards can occur depending on the skew between the individual input signals (see fig. 2). For the 10mm line, hazards no longer occur but the signal delay is increased drastically.

By doing extremely accurate solutions to Maxwell's equations of line systems one can see the strong impact on neighbouring lines. This results, in the best case, only in

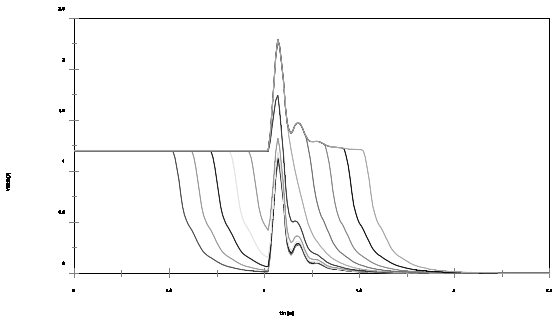

Fig. 2 Output voltage of the middle line of a 2mm odd mode driven 9-line system in 0.10 µm

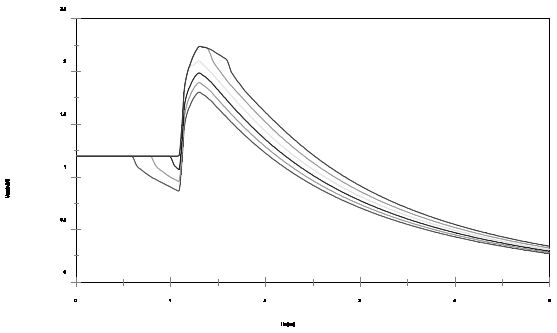

Fig. 3 Output voltage of the middle line of a 10mm odd mode driven 9-line system in 0.10 µm

a wide difference between minimum and maximum delays. This difference can be as much as 20:1 for a 20 mm line in 0.10 μm technology. In the worst case, dynamic hazards can occur asyncronously and totally invalidate data on busses interconnecting cores. Clocks are particularly vulnerable as a result of the ability to change states of cores receiving them, if a static hazard occurs. Thus, testing now must enter the world of solving wave equations to be certain of proper operation.

References

[1] SIA, "The National Technology Roadmap for Semiconductors", 1994.

[2] H. Grabinski, "An algorithm for computing the signal propagation on lossy VLSI interconnect systems in the time domain", VLSI journal on Integration, vol. 7, no. 1, April 1989, pp. 35-48.

[3] E. Grotelüschen, L.S. Dutta, S. Zaage, "Full-wave analysis and analytical formulas for the line parameters of transmission lines on semiconductor substrates", VLSI journal on Integration, vol. 16, 1993, pp.33-58.