A Cell and Macrocell Compiler for GaAs VLSI Full-Custom Design

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Abstract

A Gallium Arsenide automated layout generation system (OLYMPO) for SSI, MSI and LSI circuits used in GaAs VLSI design has been developed. We introduce a full-custom layout style, called RN-based cell model, that it is suited to generate low self-inductance circuit layouts of cells and macrocells. The cell compiler can be used as a cell library builder and it is embedded in a random logic macrocell and an iterative logic array generator. Experimental results demonstrate that OLYMPO generates complex and compact layouts and the synthesis process can be interactively used at the system design level.

1 Introduction

In a hierarchical VLSI design, a cell is a circuit of approximately the complexity of SSI components such as half-adders, full-adders, D-latchs, Muller-C or Toggle gates, and edge trigered D-flipflops; MSI or LSI components such as a 4-2 compressor, an 8-1 multiplexer, a Brent and Kung adder, a Booth multiplier, an 11-tap FIR Filter, among others.

Cell-based layout methodology is suitable for ASIC design since the layout process can be fully automated, the turnaround time is short, and the manufacturing reliability is high. Weak points of the methodology are in the design and maintenance of the cell library for every upgrade to the fabrication process and the number of the variations in the performance of cells are limited.

2 Ring Notation Based Cell Model

There are two alternative locations of power and ground rails of the inverter in DCFL [1]. The first option is the conventional approach used by nMOS designers, in which the transistors are placed in-between these two rails, as shown in Figure 1(a). Pull-up transistors are placed in a row, and pull-down transistors are placed in the adjacent row. Their gate channels are laid out parallel to the power supply and ground (Vdd and GND) rails. The self-inductance associated with the transmission line is a first order parameter which is troublesome for power supply and ground interconnections, both on-chip and off-chip.

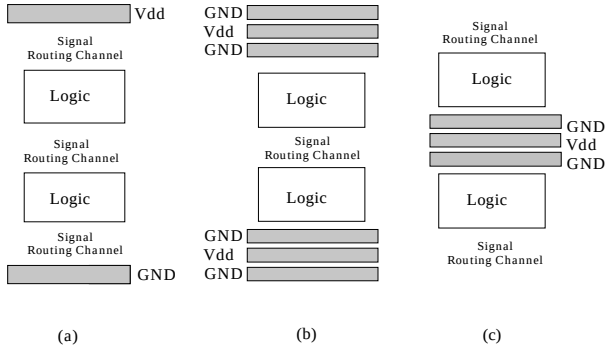

Figure 1: Power supply and ground rails arrangement: (a) classical nMOS-based cell model; RN-based cell model using (b) dual bus pair and (c) single bus pair.

Table 1: Self-inductance of different modules using nMOS-based cell model and RN-based cell model. The technology is H-GaAsIII from Vitesse.

macrocell/ module	$L_0(nH/cm)$	
	RN	nMOS
16-b Carry Save Adder	1.53	6.80
16-b 4-2 compresor	1.53	8.89
4-bit Brent and Kung adder	1.27	9.98
16-bit Brent and Kung adder	1.27	11.74
8x8-bit Booth multiplier	1.20	13.43

Experimental results (see Table 1) show that the height of RN-based cell model does not influence the self-inductance of the power supply or ground lines. However in nMOS-based cell model this height is a critical factor, and consequently, if the transistor

Table 2: Performance Comparison of Experimental Results. The technology is H-GaAsII† or H-GaAsIII‡ from Vitesse.

Cells	Delay (ps)		Area ($mm^2 \times 10^{-3}$)		($\frac{transistors}{mm^2}$)		Time
	by hand	OLYMPO	by hand	OLYMPO	by hand	OLYMPO	(s)
Half adder‡	186	179	2.9	3.2	4491	4070	0.71
D-latch‡	178	181	4.7	4.6	3404	3478	0.68
Muller C-element‡	287	273	4.3	4.7	3180	2909	0.81
Toggle gate‡	246	252	7.2	6.4	3301	3714	0.79
D-flipflop‡	240	243	7.0	6.5	2971	3200	0.84
Full adder†	467	425	12.5	10.7	3530	4123	1.68
1-b tap $x/sin(x)$ FIR‡	-	592	-	20.2	-	3614	4.35
4-2 compressor†	750	790	20.7	25.0	4396	3640	3.04
4-b Brent and Kung adder‡	347	284	147.0	121.6	4524	5468	6.53
16-b Brent and Kung adder†	736	740	1625.5	1331.9	4536	5537	12.34
11-tap FIR Filter†	-	2100	-	2962.0	-	6135	-

channels are oriented perpendicular to the power and ground lines, e.g. standard cells, the self-inductance is increased 1.5 times.

3 Cell and Macrocell Layout Generation

OLYMPO features a great capability, that is, layout on-the-fly. An intermediate format (OLYNET) permitted the integration of the system into Commercial tools like CADENCE/OPUS. A full-custom cell layout synthesizer, an iterative logic array and a random logic macrocell generators are embedded in the tool.

The OLYMPO cell compiler comprises of a translator from a SPICE netlist at gate-level and transistor-level or a EDIF netlist to the OLYMPO input description in an intermediate format (OLYNET), and two functional modules: a floorplaner and topological partitioner, and a layout generation module. Design rules for different process technologies are retrieved from a technological library. Users specifications as the positions of inputs and outputs terminals can be given.

The OLYMPO's general purpose macrocell layout generator is used for bit-sliced modules such as adders, multiplexers, registers and array-based modules as PLA, Memories, Multipliers, among others. It assembles the layout for the macrocell from leafcells generated by OLYMPO's cell compiler.

Finite state machines, combinational networks, among others, are generated by the random logic macrocell generator. A random logic macrocell contains full-custom SSI cells in single bus pair or primitives gates in dual bus pair. Generation algorithms of the macrocell depends on the cell architecture.

The system has been implemented in C programming language on a SUNSPARC 10 workstation under the UNIX operating system. Table 2 gives the results for a number of SSI and MSI cells including: an edge trigered D-flipflop, a D-latch, a T-gate, a C-gate, a half adder, a full adder, and a 4-2 compressor, among others. An 11-tap FIR filter [2] was generated by OLYMPO's iterative logic array generator. The leafcells was generated by OLYMPO's cell compiler. The last three rows of Table 2 are refered to the generation of LSI and MSI cells. The CPU time that OLYMPO consumed is presented in last column.

4 Conclusions

A Gallium Arsenide automated layout generation system for cells and macrocells used in GaAs VLSI design has been developed. Experimental results show that OLYMPO generates complex and compact layouts. The entire synthesis process is fast enough to be interactively used at the system design level.

References

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[2] S. Nooshabadi, J.A. Montiel-Nelson, G.S. Visweswaran, and D. Nagchudhuri. Micropipeline Architecture for Multiplier-less FIR Filters. In IEEE Computer Society Press, editor, *Proc. 10th IEEE Intl. Conference on VLSI Design*, pages 451–456, 1996.