

Static Analysis Tools for Soft-Core Reviews and Audits

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Abstract

Three navigation tools are presented to statically and interactively analyze Soft-Cores described in VHDL, [1]. These tools ease the adoption of mechanisms to perform reviews and audits procedures similar to those adopted in software development, [2]. These navigation tools help to better understand and reuse VHDL Soft-Cores. The three navigators are integrated in a VHDL-ICE environment, [3], to get design data management support.

1. Introduction.

According to the situation analysis provided by VSI Alliance¹, as semiconductor technology advances, the business pressure to design large ICs in a short time increases. Design reuse is expected to be a prevalent method for improving design efficiency of large ICs. In many cases, the reused blocks or cores are internally developed, but not always. Consequently, it is becoming critical for companies to increase their access to a variety of functional blocks, called Virtual Component (VC). VCs can be three forms: Soft, Firm, or Hard. Soft VCs are delivered in the form of behavioral or synthesizable Hardware Description Language (HDL), and have the advantage of being more flexible and the disadvantage of not being as predictable in terms of performance. Soft VCs typically have increased Intellectual Property (IP) protection risks because source code is required by the integrator.

The adoption of review and audit procedures coming from the software development world enhance reusability, and capitalizing on the IP library components investment.

Next section presents three new navigation tools² to support the adoption of Soft-Cores review and audit procedures. These interactive static analysis tools are fully and transparently integrated in the VHDL-ICE environment³ to ease their use without taking care of particular handling of the corresponding design data. Finally, section 3 presents the conclusions and future work.

2. Static Analysis Tools.

Static analysis methods include anything that can be done by formal (with mathematical bases) or informal analysis of the HDL description of a Soft-Core in conjunction with its processing steps (analysis, elaboration and simulation model creation), but not during them or while the simulation time advances. In order to reduce the scope of the possible analysis methods to be applied we have started by considering interactive navigation on the source code of the VHDL Design Units (DUs), the hierarchical components structure of a given Design Entity (DE) and its corresponding underlying simulatable model. These tools are specially useful when documentation and comments is not enough to properly understand and reuse the HDL descriptions of a given Soft-Core.

2.1 VHDL Design Unit Navigation.

This tool works on DE Declarations, Architecture Bodies, Package Declarations and Package Bodies. Its navigation capabilities are complementary to the source code edition. Its use is particularly indicated while developing a new Soft-Core, and specially when acquiring one that it is not very well documented, or their in-line comments are not enough to understand the functionality or the usage of the IP.

¹ VSI Alliance stands for Virtual Socket Interface Alliance. This alliance was formed from a common understanding of a looming bottleneck for the continued rapid evolution of the electronics industry and a shared vision for its solutions based on the continued use or “reuse” of existing functions, but which are designed in such a way as to make possible the mix-and-match of such functions from different sources onto a single silicon solution. See <http://www.vsi.org>.

² These tools are part of the VHDL Simulation Assessment tools under development in OMI-ESPRIT Project REQUEST. See <http://www.omimo.be>.

³ VHDL-ICE is a leading VHDL Integrated Common Environment, for UNIX and Windows NT, under development in the OMI-ESPRIT Project TOMI. See <http://www.omimo.be>.

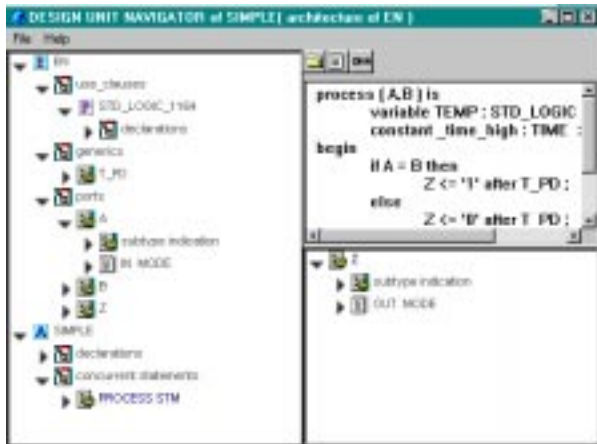


Figure 1.- VHDL Design Unit Navigator.

2.2 VHDL Design Hierarchy Navigation.

This tool deals with the hierarchical structure of a given DE. It also informs about connectivity and the places where a given component is used. It automatically generates a configuration declaration DU from a given VHDL Design Hierarchy.

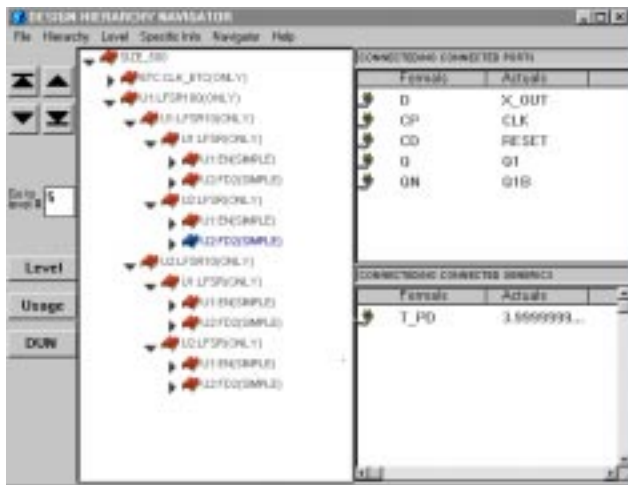


Figure 2.- VHDL Design Hierarchy Navigator.

2.3 VHDL Simulation Model Navigation.

This tool is “constrained” by simulation semantics underlying to any VHDL description, [1,3]. The other two navigators are not constrained by this semantics and the result of their use for assessing a Soft-Core is independent of the further usage to which the VHDL description is oriented. This navigator allows to statically analyze the underlying simulatable model based on a heterarchy of VHDL processes interconnected by nets. The tool makes a

correspondance between the VHDL source and simulatable codes.



Figure 3.- VHDL Simulation Model Navigator.

This tool shows information about the VHDL processes and nets of the simulatable model. This helps to understand which components, processes or statements are reading or writing a given signal and how it is transformed before providing the corresponding driving value.

3. Conclusions

The availability of these navigation tools ease the introduction of mechanisms to statically analyze VHDL Soft-Core by means of applying reviews and audits. These processes are tremendously important specially when foreign reuse of the cores is considered. The more IP commercialization the bigger need for easily understanding its hidden know-how. For these reasons, companion tools to the ones presented in this work will presumably appear very soon as complementary tools to the already existing design tools (simulators, synthesis tools and so on). Current navigators deal only with static and interactive assessment but the extension to cover dynamic analysis of the simulation model is already under development.

References.

- [1] "1076-93 IEEE Standard VHDL Language Reference Manual", IEEE Inc., New York, N.Y., U.S.A., September 1993.
- [2] "IEEE Std. 1028-1988 for Software Reviews and Audits," IEEE Inc., New York, N.Y., U.S.A., 1988.
- [3] S. Olcoz, Lorenzo Ayuda, Ana Castellví, María García, Iván Izaguirre, Olga Peñalba, "Implementing a VHDL Design Manager: VHDL-ICE." VHDL International Users' Forum, Spring Conference, April 1997, pp. 93-102.