

Keynote Adresses: Summaries

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Design and Test Challenges Behind Systems-on-Silicon

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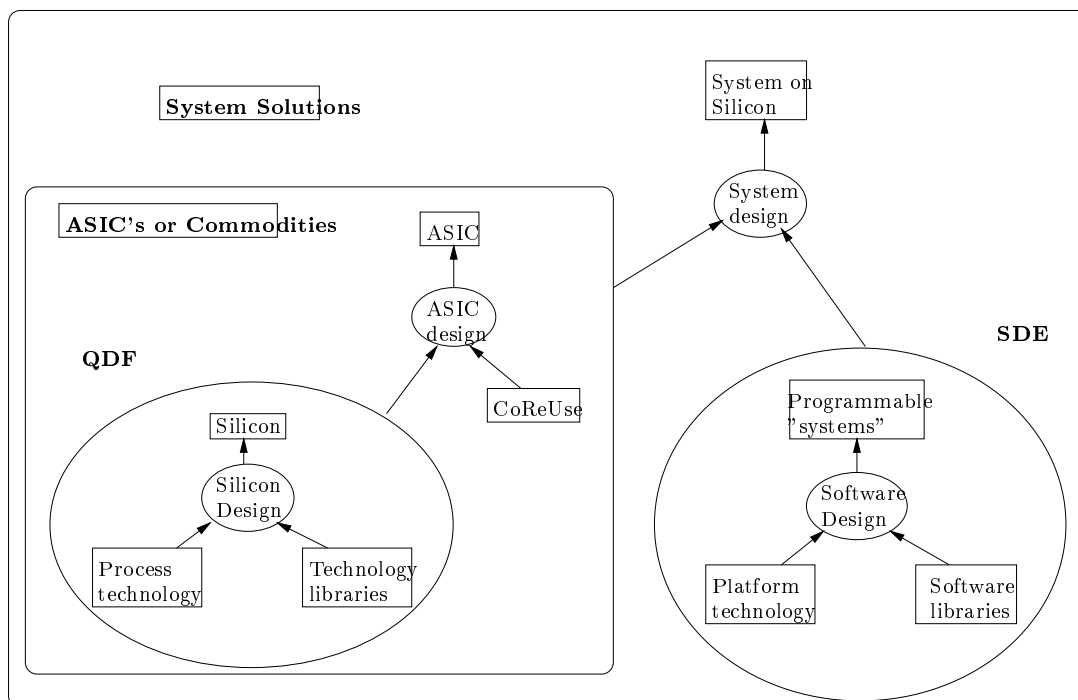
The semiconductor industry is going through a major change. Firstly, the total size of the industry is continuously growing with an average of roughly 17% per year, though never reaching this percentage in any year. It is either low growth, or even shrink, or fast growth with 30% or so. Further we see some specialization in the industry. There are new companies that have focused on the foundry business. They provide access to the most advanced technologies, mastering to the extreme the manufacturing process. Others have specialized in providing (a large range of) components such as CPUs or memories. The set of companies I want to concentrate on however are those that can be identified as system-on-silicon providers. They merge the capabilities of efficiently designing and manufacturing silicon components with those of developing system architectures for specific application domains. Philips Semiconductors is one example of such a company, and I dare to say that all major European semiconductor suppliers have selected to be engaged in such a business. I will present some of the design and test challenges that are the result of such a business position. As this then holds for all these European companies (as well as for a number of those based in the US and Japan) this may also pose a major opportunity for a revitalization of the European EDA industry.

The picture shows the changes which are taking place, as well as the challenges for a system-on-silicon supplier. The left hand part of the picture shows the situation where we are right now: we develop ASICs, which together with other ICs and components will form an (electronic) system. Time to Market and Quality

requires the creation of a well defined and stable development environment. Often forgotten, but such a Qualified Design Flow (QDF) consisting of a flow, the tools itself and the libraries, is key. Further, in order to speed up Time to Market, we invest heavily in reuse capabilities and approaches. Changes observed are the move from analog to digital (apparent for the Consumer IC area) and the convergence of applications (audio, video and communications). Needless to mention, though still not easy to master, is the ever increasing complexity of course. The new challenge, and opportunity, then clearly comes from the right hand part of the picture, the software. Also here the need for a stable and uniform Software Development Environment (SDE, the software QDF equivalent) exists. Looking at the total picture, observed changes are the usage of (de facto) standards and the definition of platforms. A platform is a generic architecture for a specific application domain comprising of the essential functional blocks and interfaces, both hardware and software, including the development environments. For example a platform may comprise of a CPU, a DSP core, an Operating System, and a (C) compiler. The system-on-silicon supplier(s) need to clearly define those platforms, where a close co-operation with system houses is an absolute necessity.

For the system-on-silicon supplier, this changing business means that they have to focus on even more topics than they are used to do:

- Process Technology remains an important topic. The Deep Sub Micron impact is eminent, technically as well as from an investment point of view.



- Assembly Technology is an often overlooked area, though increasingly important with business drivers like for instance portable equipment.
- Intellectual Property is already, and will become even further, an issue. For the system-on-silicon supplier IP exists on every level of the development chain (*soft* high level VHDL code, netlist descriptions and *hard* layout blocks). It is up to the companies to exploit their IP as much as possible. At the same time they have to keep an eye on other IP providers, and make use of those offerings when relevant and when fitting in the strategy.
- System level design. In fact this means HW/SW codesign, where the issue of being able to quickly and correctly making the HW/SW trade-off, is key.
- Last but not least (Design for) Test plays a role on all levels. We have to make sure that we use the correct fault models, which should reflect the potential defects from the processing in the most economic way. At the same time Design for Test will play an increasing role at the system level, certainly when the need for debug is recognized.

I hope you will agree with me that all this is a tremendous challenge for the European industry, with great opportunities for many companies (silicon suppliers, system houses, EDA suppliers, ...), for research institutes and for the universities. Let's make it happen.

Design Methodologies for the Information Age: Moving up the Totem Pole

Rajeev Jain,
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Just as the obsession with computing power and CPU speed has driven system design strategies in the past decades, the future design methodologies will be driven by the exponentially growing demand for information services. More and more designers will have to transition from the realm of CPUs and cache memories to the world of network and communication components such as internet protocols, modulation and coding. Since billion transistor chips can accomodate almost every function for networking, communicating and computing, the design methodologies will have to address the needs of these diverse functions on a single device. While Intellectual Property (IP) integration provides the mechanics for integrating these functions on a die it does not support the system optimizations needed to develop competitive products. Design methodologies will have to move yet another notch up the totem pole to perform these optimizations.

Build-in Quality for System Chips and Beyond

Yervant Zorian
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The basic concept of embedding quality insurance functions onto the very piece of electronics product is simple. The complexity and opportunities offered by the emerging system chip technology and electronics industry at large dictate that adequate and cost effective test, measurement, diagnosis and repairs is impossible without some form of build-in quality insurance functions.