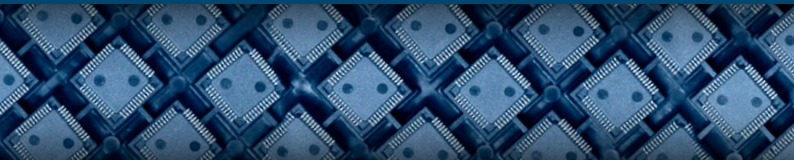


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CORPORATE SPONSORS



Media Partners	002
Welcome	004
General Information	011
<hr/>	
KEYNOTE SPEAKERS	
Amnon Shashua, Mobileye Intel Corporation, US	006
Christopher Voigt, MIT, US	007
Jelena Vuckovic, Stanford University, US	008
Thomas Form, Volkswagen AG, DE	009
<hr/>	
EXECUTIVE SESSIONS	015
Giovanni De Micheli, EPFL, CH	
Marco Casale-Rossi, Synopsys, IT	
<hr/>	
FUTURE AND EMERGING TECHNOLOGIES	016
Robert Wille, Johannes Kepler University Linz, DE	
Subhasish Mitra, Stanford University, US	
<hr/>	
DESIGNING AUTONOMOUS SYSTEMS	017
Rolf Ernst, Institut für Datentechnik und Kommunikationsnetze, DE	
Marco Platzner, University of Paderborn, DE	
<hr/>	
SPECIAL & EU SESSIONS	018
Giovanni De Micheli, EPFL, CH Marco Casale-Rossi, Synopsys, IT	
Paul Pop, Technical University of Denmark, DK	
<hr/>	
DATE 2018 – AT A GLANCE	021
A brief overview of the event	
<hr/>	
MONDAY TUTORIALS AND EVENTS	029
Seven afternoon tutorials	029
Forum: Advancing Diversity in EDA	138
2nd IoT Student Challenge, sponsored by IEEE CEDA and Texas Instruments	021
<hr/>	
TECHNICAL SESSIONS	040
Full listing of DATE technical programme, special sessions	
<hr/>	
FRIDAY WORKSHOPS	104
Six full-day workshops	
<hr/>	
EXHIBITION THEATRE PROGRAMME OVERVIEW	120
Free for exhibition visitors	
<hr/>	
UNIVERSITY BOOTH	122
<hr/>	
FRINGE TECHNICAL MEETINGS	138
<hr/>	
CO-LOCATED WORKSHOPS	141
<hr/>	
EXHIBITION GUIDE	143
<hr/>	
Committees & Topic Chairs	167
Detailed Index	173
Venue Plan	C04

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Engineering & Technology is packed with articles on the latest technology covering the areas of communications, control, consumer technology, electronics, IT, manufacturing & power engineering. It is

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Each member of the Institution of Engineering & Technology (IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users.

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www.eandtmagazine.com

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Dear Colleague,

We proudly present the Advance Programme of **DATE 2018**. DATE combines the world's favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

Out of a total of 766 paper submissions received, a large share (39%) has come from authors in Europe, 26% of submissions are from America, 34% from Asia, and 1% from the rest of the world. This distribution clearly demonstrates DATE's international character, global reach, and impact.

For the 21st successive year, DATE has prepared an exciting technical programme. With the help of 335 members of the Technical Program Committee who carried out 3079 reviews (mostly four reviews per submission), finally 185 papers (24%) were selected for regular presentation and 85 additional ones (cumulatively 35%, including all papers) for interactive presentation.

The DATE conference takes place from 19 to 23 March 2018, at the International Congress Center Dresden, Germany. On the first day of the DATE event, **four in-depth technical tutorials** on the four main topics of DATE as well as **three industry hands-on tutorials** are given by leading experts in their respective fields. Technical topics covered are emerging technologies for computing, industrial internet-of-things (IoT), reliability from physics to CAD, virtual prototyping and low-power design, as well as industrial topics on building ARM powered IoT, computer vision for automated driving in MATLAB, and how to implement domain-specific modeling languages.

Also on Monday, DATE hosts the first edition of a new forum, "**Advancing Diversity in Electronic Design Automation (DivEDA)**", which aims to increase the number and visibility of women and underrepresented minorities in the research community.

The **plenary keynote speakers on Tuesday** are Prof. Amnon Shashua, CEO & CTO of Mobileye, whose talk is about "The Responsibility Sensitive Safety (RSS) Formal Model toward Safety Guarantees for Autonomous Vehicles" and Dr. Christopher Voigt, Professor of Biological Engineering at MIT, to talk about "Programming Living Cells: Design Automation to Map Circuits to DNA". On the same day, the **Executive Track** offers a series of business panels with executive speakers from companies leading the design and automation industry, discussing hot topics.

The main conference programme from Tuesday to Thursday includes 79 technical sessions organized in parallel tracks from the four areas

D – Design Methods & Tools

A – Application Design

T – Test, Reliability, and Robustness

E – Embedded and Cyber-Physical Systems

and from several special sessions on hot topics, such as emerging technologies, low power challenges and approximate computing for IoT devices, security-aware design in cyber-physical systems, new benchmarking methods and applications for emerging devices, circuits, and architectures, methodologies to design and manage exascale computing system technologies, as well as results and lessons learned from European projects.



Jan Madsen



Ayse K. Coskun

Two Special Days in the programme focus on areas bringing new challenges to the system design community: **Future and Emerging Technologies** and **Designing Autonomous Systems**. Each of the special days has a full programme of keynotes, panels, tutorials and technical presentations.

During the Special Day on "Future and Emerging Technologies" on **Wednesday**, a keynote is given by Prof. Jelena Vuckovic from Stanford University, on "From Inverse Design to Implementation of Robust and Efficient Photonics for Computing". On **Thursday** in the frame of the Special Day on "Designing Autonomous Systems", Thomas Form, Head of Electronics and Vehicle Research, Volkswagen AG, and co-ordinator of the Pegasus research project on safety of automated driving gives a talk about "Autonomous Driving: Ready to Market? Which are the Remaining Top Challenges?".

Additionally, there are numerous **Interactive Presentations** which are organized into five IP sessions.

To inform attendees on commercial and design-related topics, the **Exhibition Theatre** provides a full programme, combining presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and interviews with keynote speakers form the conference. The conference is complemented by an **exhibition, running for three days (Tuesday – Thursday)**, including campus booths with focus on special topics such as **autonomous driving, 5G, FDSOI and IoT Security**. The exhibition provides a unique networking opportunity and sets the perfect venue for industry to meet university professors to foster their university programme and also for PhD Students to meet future potential employers.

On Friday, there are **6 full-day workshops**, covering a large number of hot topics like software for IoT, emerging memories and interconnects, and new platforms for future cars.

We wish you an exciting and memorable DATE 2018, a successful exhibition visit and an entertaining DATE party on Wednesday evening which takes place in the "Deutsches Hygiene-Museum Dresden".

DATE 2018 General Chair
Jan Madsen
Technical University
of Denmark, DK

DATE 2018 Programme Chair
Ayse K. Coskun
Boston University, US

**Amnon Shashua**

March 20, 2018, 0915 – 1000, Großer Saal

1.1.1

The Responsibility Sensitive Safety (RSS) Formal Model toward Safety Guarantees for Autonomous Vehicles

Prof. Amnon Shashua, CEO & CTO, Mobileye, an Intel company, and Senior Vice President, Intel Corporation, US

In recent years, car makers and tech companies are racing toward self-driving cars. A critical component in getting society acceptance to the technology is to find a way to guarantee safety. The prevailing common wisdom is a data-driven empirical approach for safety validation where the more mileage driven the better the maturity of the system must be. I will describe a model in which the sources of errors due to Planning (the actions and decisions for negotiating motion in traffic) can be fenced out from the data driven approach through a formal model of the common sense behind human judgment of what it means to cause an accident and how to define actions that will guarantee that the AV will never cause an accident due to Planning. The model creates a clear distinction of what can be certified by regulators and what should be left to the judgment of AV manufacturers. The RSS model also puts in context the conversation of “ethical dilemmas” by providing a formal framework for the discussion.

**Christopher Voigt**

March 20, 2018, 1000 – 1030, Großer Saal

1.1.2**Programming Living Cells: Design Automation to Map Circuits to DNA**

Christopher Voigt, Professor of Biological Engineering at MIT, US

Platforms are being established to facilitate large genetic engineering projects. A desired cellular function is divided into systems that can be developed independently and then combined. Genetic sensors allow cells to receive environmental and cell state information. Sensory information is integrated by genetic circuits, which control the conditions and timing of a response. The circuit outputs are connected to actuators that control what the cell is doing, from building molecules to moving and communicating. Design automation tools from the electronics industry are applied to map a circuit design to a DNA sequence. Collectively, this enables a wide range of applications, for example cells that communicate to build a material, navigate the human body to treat a disease, or protect plants by responding to the environment.



Jelena Vuckovic

March 21, 2018, 1350 – 1420, Saal 2
Supported by IEEE CEDA

7.0

From Inverse Design to Implementation of Robust and Efficient Photonics for Computing

Jelena Vuckovic, Stanford University, US

It is estimated that nearly 10% of the world electricity is consumed in information processing and computing, including data centers [D.A.B. Miller, *Journal of Lightwave Technology*, 2017]. It is clear that the exponential growth in use of these technologies is not sustainable unless dramatic changes are made to computing hardware, in order to increase its speed and energy efficiency. Optical interconnects are considered a solution to these obstacles, with potential to reduce energy consumption in on-chip optical interconnects to atto-Joule per bit (aJ/bit), while increasing operating speed beyond 20GHz. However, the state of the art photonics is bulky, inefficient, sensitive to environment, lossy, and its performance is severely degraded in real-world environment as opposed to ideal laboratory conditions, which has prevented from using it in many practical applications, including interconnects. Therefore, it is clear that new approaches for implementing photonics are crucial.

We have recently developed a computational approach to inverse-design photonics based on desired performance, with fabrication constraints and structure robustness incorporated in design process. Our approach performs physics guided search through the full parameter space until the optimal solution is reached. Resulting device designs are non-intuitive, but are fabricable using standard techniques, resistant to temperature variations of hundreds of degrees, typical fabrication errors, and they outperform state of the art counterparts by many orders of magnitude in footprint, efficiency and stability. This is completely different from conventional approach to design photonics, which is almost always performed by brute-force or intuition-guided tuning of a few parameters of known structures, until satisfactory performance is achieved, and which almost always leads to sub-optimal designs.

Apart from integrated photonics, our approach is also applicable to any other optical and quantum optical devices and systems.

From 1345 - 1350, there will be the Presentation of the IEEE TCCPS Technical Achievement Award to Prof. Alberto Sangiovanni-Vincentelli (handed over by Shiyun Hu, Chair of TCCPS) directly before the start of the keynote address.

**Thomas Form**

March 22, 2018, 1320 – 1350, Saal 2

11.0

Autonomous Driving: Ready to Market? Which are the Remaining Top Challenges?

Thomas Form, Head of Electronics and Vehicle Research, Volkswagen AG, and co-ordinator of the Pegasus research project on safety of automated driving

During the last years a lot of prototypes for automated/ autonomous driving vehicles have been presented to the public. Depending on the use case car manufacturers or tech companies have used an evolutionary or a revolutionary approach. While the evolutionary way should be more reasonable applied for owned cars due to cost restraints and the need for the functionality to work more or less by “something everywhere”, the revolutionary approach following the strategy “everything somewhere” seems to be the better solution for fleets of autonomous cabs or shuttles.

Although we have seen a lot of functional concepts for both approaches to automation, there are still some big challenges to be solved. On one hand the whole automation function has to be designed redundantly to ensure a sufficient functional safety level. In this context the use of Artificial Intelligence based networks could be a solution in particular neuronal networks based on deep learning.

On the other hand there is still the question “how good is good enough” having in mind that perfectly working systems cannot be realized and how can the necessary verification/validation process be implemented. The public funded project PEGASUS is working to provide first answers.

However: do we have considered all impacts of automated mobility?



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This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2018. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website www.date-conference.com

Dates and Venue

The conference will take place from 19 to 23 March, 2018, in the MARITIM Hotel & International Congress Center Dresden (ICCD).

Maritim Hotel & Internationales
Congress Center Dresden
Ostra-Ufer 2 / Devrientstr. 10 – 12
01067 Dresden
www.dresden-congresscenter.de

The accompanying exhibition is scheduled from 20 to 22 March, 2018, and will take place on the Terrace Level of the ICCD, which also hosts the coffee break area.

Interactive Programme Online

A fully interactive DATE 2018 programme is available on the website www.date-conference.com where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

Free wireless internet access is available on-site throughout the whole congress center during the entire DATE week. The WLAN login code will be provided at the registration desk upon arrival (entrance foyer of the congress center).

Proceedings

The conference proceedings are available on USB Stick on-site (sponsored by Texas Instruments) for every fully registered conference delegate.

WHOVA Conference App

The Whova app can be downloaded via the following link or in the Apple/Google stores for free: <https://whova.com/download> Please install the app and search for the conference “DATE 2018”
→ **Password: “DATE”**

A browser version can be accessed at
https://whova.com/webapp/e/datec_201803/

Online Conference Evaluation via the WHOVA App (“survey” button): every fully registered delegate who fills in the online conference evaluation via the app, will receive one of the exclusive DATE collector mugs at the registration desk (when showing the confirmation page).

A browser version can be accessed at
<https://www.date-conference.com/survey>

Coffee Break in the Exhibition Area

On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks at the below-mentioned times in the exhibition area (Terrace Level of the ICCD).

Lunch Break (Großer Saal + Saal 1)

On all conference days (Tuesday to Thursday), a seated lunch (lunch buffet) will be offered in the rooms “Großer Saal” and “Saal 1” (Saal Level of the ICCD) to fully registered conference delegates only. There will be lunch voucher control at the entrance to the lunch break area.

Tuesday, March 20, 2018

Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Coffee Break	1600 – 1700

Wednesday, March 21, 2018

Coffee Break	1000 – 1100
Lunch Break	1230 – 1430
<i>Awards Presentation and Keynote Lecture in “Saal 2”</i>	1345 – 1420
Coffee Break	1600 – 1700

Thursday, March 22, 2018

Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
<i>Keynote Lecture in “Saal 2”</i>	1320 – 1350
Coffee Break	1530 – 1600

Welcome Reception & PhD Forum Monday, March 19, 2018

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2018 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 19, 2018, from 1800 - 2100 in “Saal 1” of the ICC Dresden.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIG-DA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

Exhibition Reception

Tuesday, March 20, 2018

The Exhibition Reception will take place on Tuesday, March 20, 2018, from 1830 – 1930 in the exhibition area (Terrace Level), where free drinks for all conference delegates and exhibition visitors will be offered. All exhibitors are welcome to also provide drinks and snacks for the attendees.

DATE Party | Networking Event Wednesday, March 21, 2018

Wednesday, March 21, 2018 The DATE Party traditionally states one of the highlights of the DATE week. As one of the main networking opportunities during the DATE week, it is a perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. It is scheduled on March 21, 2018, from 1930 to 2300.

As in 2017, the DATE Party will again feature the awards presentation of the Best Paper Awards and Best IP Award.

This year, it will take place in one of Dresden's most recognized museum locations, the Deutsches Hygiene-Museum Dresden, which attracts over 300,000 international visitors per year. The Deutsches Hygiene-Museum was founded in 1912 and is a unique museum location. Unlike its traditional name, the museum offers nowadays not just hygiene in the medical or colloquial way. Moreover, visitors may explore in the permanent collection "Adventure Human Being" how people shape their environment and affect society as a physical and intellectual being, and how they are influenced by it vice versa. The museum is located close to the city center and will offer a special setting for the DATE Party 2018.

→ **Please kindly note that it is not a seated dinner.**

All delegates, exhibitors and their guests are invited to attend the party. Please note that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Price for extra ticket: 70 € per person.

How to get there: A bus shuttle from the congress centre to the Hygiene-Museum Dresden will be organized, starting at 1900 from the main entrance of the ICC Dresden.

Afterwards, busses will be at your disposal for getting back to the city centre, at the following times: 2230 and 2300. You will have the choice between a bus that stops at "Postplatz" and a bus that will stop at the Maritim Hotel & International Congress Centre Dresden.

Route description → www.dhmd.de/en/your-visit/directions

By public transportation: Take the tram line 4 (Direction: Striesen) from the ICC Dresden (Kongresszentrum/ Haus der Presse stop) to the stop Deutsches Hygienemuseum. Check times here: www.dvb.de

By car: Take the A4 motorway, Hellerau exit or Altstadt exit, Direction Zentrum and follow the signage. Street parking is available.

Walking distance: 10 minutes from the tram stop Deutsches Hygiene-Museum 35 minutes from the ICC Dresden

Interactive Presentations*(sponsored by the Cadence Academic Network)*

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress, which may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the foyer of the Conference Level in 30-minute time slots on the following days:

Tuesday, March 20, 2018

IP Session 1	Conference Level, Foyer	1600 – 1630
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Wednesday, March 21, 2018

IP Session 2	Conference Level, Foyer	1000 – 1030
IP Session 3	Conference Level, Foyer	1600 – 1630
Presentation of the Best IP Award	during the DATE Party (Hygiene-Museum Dresden)	2100 – 2115

Thursday, March 22, 2018

IP Session 4	Conference Level, Foyer	1000 – 1030
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Thursday, March 22, 2018

IP Session 5	Conference Level, Foyer	1530 – 1600
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ACADEMIC NETWORK

Co-Chairs:**Giovanni De Micheli**, EPFL, CH**Marco Casale-Rossi**, Synopsys, IT

Innovation runs strong in our industry: artificial intelligence hardware and software have recently achieved superhuman performances [1]; general purpose quantum computers will be available within the next five years [2], and all the top 10 automakers have already announced plans toward SAE level 4, and 5 availability before the end of this decade. Sensors, and actuators will be the essential arms, ears, and eyes of all these technologies. This year Executive Track begins with a panel which gathers world experts to discuss the opportunities and the challenges of these emerging technologies, which may change our lives.

Whether for the good or the bad, depends also on the engineering community: new processors architectures are emerging, superconducting electronics and quantum computing shake the foundations of EDA, and autonomous driving pushes performance, power consumption, and reliability envelope beyond any previous limit. The Executive Track continues with a session on the advances required for the design automation of quantum computing devices, followed by a session on the most recent advances in logic synthesis.

2.1

Executive Panel: How Electronics May Change Our Lives, and the World**Moderator: Antun Domic**, Synopsys, USA

→ See Page 41

3.1

Executive Session: Design Automation for Quantum Computing**Chair: Edoardo Charbon**, TU Delft, NE & EPFL, CH**Co-Chair: Daniel Große**, University of Bremen, DE

→ See Page 46

4.1

Executive Session: Exact Synthesis and SAT**Chair: Patrick Vuillod**, Synopsys, FR**Co-Chair: Luca Amarù**, Synopsys, US

→ See Page 52

Future and Emerging Technologies

Co-Chairs:

Robert Wille, Johannes Kepler University Linz, DE

Subhasish Mitra, Stanford University, US

The demands of future applications far exceed the capabilities of today's computing systems. Yet the progress in traditional computing hardware technologies has begun to stall at the exact moment when these exciting applications are demanding large improvements with respect to functionality, performance, and energy efficiency. Besides that, the impressive progress in the development of semiconductors motivated numerous "Moore-than-Moore"-applications.

This special day will explore transformative concepts that will revolutionize future computing systems. It thereby reflects the broad variety of future and emerging technologies -- ranging from microfluidic devices over photonics and quantum computing to nanosystems. All talks are prepared in the spirit to first provide an overview of the respectively considered technology before open challenges and problems for which design automation methods may help are discussed. This way, the special day aims to trigger a more thorough exchange between the different communities.

5.1

Special Day Session on Future and Emerging Technologies: Challenges for the Design of Microfluidic Devices: EDA for your Lab-on-a-Chip

→ See Page 58

6.1

Special Day Session on Future and Emerging Technologies: Transistors for Digital NanoSystems: The Road Ahead

→ See Page 64

7.0

LUNCH TIME KEYNOTE SESSION: From Inverse Design to Implementation of Robust and Efficient Photonics for Computing

→ See Page 68

7.1

Special Day Session on Future and Emerging Technologies: Theoretical and practical aspects of verification of quantum computers

→ See Page 68

8.1

Special Day Session on Future and Emerging Technologies: NanoSystems: Connecting Devices, Architectures, and Applications

→ See Page 76

Designing Autonomous Systems

Co-Chairs:

Rolf Ernst, Institut für Datentechnik und Kommunikationsnetze, DE
Marco Platzner, University of Paderborn, DE

Autonomous vehicles and robots are prominent examples for a larger trend towards embedded and cyber-physical systems autonomy serving many purposes: function automation, function adaptation, platform adaptation, and handling the dynamics of function integration on large open networks. In autonomous systems, the current separation of design process and operation in the field will be replaced by a life-time process of in-field adaptation. Continuous change and evolution, application interference, environment dynamics and uncertainty have complex effects which must be controlled thereby adhering to safety, availability, and security guarantees where needed. This special day covers the latest trends in autonomous systems and the resulting challenges for design processes and EDA tools.

The first session addresses embedded machine learning, a core technology for autonomous systems, from its impact on safe automated driving to the design of scalable hardware accelerators. The second session outlines the impact of autonomous systems on the industrial design process, including services, vehicle functionality and its design, and the transition from mechanically dominated to software driven processes in industry 4.0. The lunch time keynote gives an insight in the resulting evolution of the automotive industry from a leading OEM perspective thereby emphasizing new safety and verification challenges. The first afternoon session focuses on another important and growing area of autonomous systems, smart vision systems. The last session is dedicated to the design of self-aware autonomous systems and their applications in avionics and automotive systems.

9.1

Special Day Session on Designing Autonomous Systems: Embedded Machine Learning

→ See Page 82

10.1

Special Day Session on Designing Autonomous Systems: Digitalization in automotive and industrial systems

→ See Page 88

11.0

LUNCH TIME KEYNOTE SESSION: Autonomous Driving: Ready to Market? Which are the Remaining Top Challenges?

→ See Page 92

11.1

Special Day Session on Designing Autonomous Systems: Smart Vision Systems

→ See Page 93

12.1

Special Day Session on Designing Autonomous Systems: Self-awareness for Autonomous Systems

→ See Page 100

Special Session Chairs:**Giovanni De Micheli**, EPFL, CH and Marco Casale-Rossi, Synopsys, IT**EU Sessions Chair: Paul Pop**, Technical University of Denmark, DK

The following Special Sessions have been organized, which should be of great general interest, and make a technical status about topics such as security for Internet-of-Things devices and applications, image recognition, machine learning processors, emerging devices, memories, and architectures:

2.7

Special Session: Spintronics based New Computing Paradigms and Applications**Chair: Weisheng Zhao**, Beihang University, PRC**Co-Chair: Mehdi Tahoori**, Karlsruhe Institute of Technology, DE

→ See Page 44

4.6

Special Session: Securing Power-constrained System-on-Chips: Challenges and Opportunities**Chair: Saibal Mukhopadhyay**, Georgia Institute of Technology, USA

→ See Page 55

5.4

Special Session: Lightweight Security for Resources-Constrained Internet-of-Things Applications**Chair: Basel Halak**, University of Southampton, UK**Co-Chair: Yier Jin Jin Yier**, University of Florida, USA

→ See Page 59

6.5

Special Session: Three Years of Low-Power Image Recognition Challenge**Chair: Yung-Hsiang Lu**, Purdue University, USA

→ See Page 66

7.6

Special Session: Next Generation Processors and Architectures for Deep Learning**Chair: Theocharis Theocharides**, University of Cyprus, CY**Co-Chair: Muhammad Shafique**, TU Wien, AT

→ See Page 72

8.2

EU Projects: Novel Technologies, Predictable Architectures and Worst-Case Execution Times

Chair: Paul Pop, Technical University of Denmark, DK
Co-Chair: Petru Eles, Linköping University, SE

→ See Page 76

9.4

EU Projects: Novel Platforms – from Self-Aware MPSoCs to Server Ecosystems

Chair: Martin Schoeberl, Technical University of Denmark, DK
Co-Chair: Flavius Gruian, Lund University, SE

→ See Page 84

10.6

Special Session: Computing with Ferroelectric FETs - Devices, Models, Systems, and Applications

Organizer: Michael Niemier, Notre Dame University, USA
Co-Chair: O'Connor, Ecole Centrale de Lyon, FR

→ See Page 91

12.6

Special Session: Computing with Emerging Memories: How Good can it be?

Organizer: Pierre-Emmanuel Gaillardon, University of Utah, USA
Co-Chair: O'Connor, Ecole Centrale de Lyon, FR

→ See Page 103

MON

TUE

WED

THU

FRI

EVENT OVERVIEW

MON

- 2nd IoT Student Challenge sponsored by IEEE CEDA and Texas Instruments
- Afternoon Tutorials
- EDA Forum: Advancing Diversity in EDA
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

TUE

- Opening Session: Plenary, Awards Ceremony & Keynote Addresses
- Executive Sessions
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Interactive Presentation IP1
- University Booth
- Fringe Meetings & Co-Located Workshops
- Exhibition Reception

WED

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on “Future and Emerging Technologies” and Keynote
- Interactive Presentations IP2 and IP3
- University Booth
- Fringe Meetings & Co-Located Workshops
- DATE Party | Networking Event

THU

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on “Designing Autonomous Systems” and Keynote
- Fringe Meetings & Co-Located Workshops
- Interactive Presentations IP4 and IP5
- University Booth

FRI

- Special Interest Workshops

CONTACTS

DATE 2018 Conference Organization

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Bautzner Str. 117 – 119
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Email: date@kitdresden.de

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Registration & Accommodation:

Elisa Antonucci
K.I.T. Group GmbH Dresden, DE
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date-registration@kitdresden.de

1330	Tutorial and Conference Registration	ICCD main entrance
1530–1600	Tutorial Coffee Break	

Registered participants can attend any tutorial and may move between tutorials during the session.

	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4
1400–1800	M01 Design: Emerging Technologies for Computing – From Devices to Systems	M02 Applications: Effective System Level Simulation Techniques and Cross-Layer Perspectives on Low Power Design	M03 Test: Reliability: From Physics to CAD	M04 Embedded: Industrial Internet-of-Things: Architectures, Designs and Challenges
	Konferenz 5	Seminar 3+4	Seminar 5+6	

1400–1800	M05 Industrial A: How to Implement Domain-Specific Modeling Languages: Hands-on Tutorial	M06 Industrial B: Building Arm Cortex-M Powered Internet of Things (IoT) Applications: From Design to Deployment	M07 Industrial C: Computer Vision for Automated Driving in MATLAB	
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1800–2100	Welcome Reception & PhD Forum, incl. Awards Presentation (PhD Forum Prize and 2nd IEEE CEDA IoT Student Challenge Prize) Saal 1			
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MONDAY EVENTS

March 19, 2018, 0900 – 1800, Konferenz 6

FM03

2nd IoT Student Challenge, sponsored by IEEE CEDA and Texas Instruments

Organiser: Akash Kumar, Technische Universitaet Dresden, DE

March 19, 2018, 1400 – 1800, Seminar 1 (Attendance free of charge)

FM04

Forum: Advancing Diversity in Electronic Design Automation (DivEDA)

Organisers: Ayse Coskun, Boston University, US
Eli Bozorgzadeh, University of California, Irvine, US

0730	Registration Speaker's Breakfast, Saal 1			
0830 – 1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses Großer Saal			
1030 – 1130	Exhibition and Coffee Break			
	Track 1	Track 2	Track 3	Track 4
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1130 – 1300	2.1 Executive Panel: How Electronics May Change Our Lives, and the World	2.2 Energy Efficient Neural Networks	2.3 High-Level Synthesis	2.4 Model Checking
1300 – 1430	Lunch Break, Großer Saal + Saal 1			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1430 – 1600	3.1 Executive Session: Design Automation for Quantum Computing	3.2 Approximate and Near-Threshold Computing	3.3 Optimization Techniques for MPSoCs	3.4 Optimizing Computing with Neuromorphic Architectures and Accelerators
1600 – 1700	Exhibition and Coffee Break 1600 – 1630 IP1 Interactive Presentations, Conference Level, Foyer			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1700 – 1830	4.1 Executive Session: Exact Synthesis and SAT	4.2 Domain Specific Design Methodologies	4.3 System Modelling for Simulation and Optimisation	4.4 Overcoming the Limitations of Worst-Case IC Design
1830 – 1930	EXHIBITION RECEPTION in the Exhibition Area			

Plenary OPENING

Executive Sessions

Special & EU Session

IP Session

Exhibition Theatre

Registration Speaker's Breakfast, Saal 1				0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses Großer Saal				0830 – 1030
Exhibition and Coffee Break				1030 – 1130
Track 5	Track 6	Track 7	TRACK 8	
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
2.5 GPU and GPU-based heterogeneous system management	2.6 Circuit Locking and Camouflaging	2.7 Special Session: Spintronics based New Computing Paradigms and Applications	2.8 Enabling ICT Innovations for European SMEs	1130 – 1300
Lunch Break, Großer Saal + Saal 1				1300 – 1430
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
3.5 Memory Reliability	3.6 Real-time Multiprocessing		3.8 Innovative Products for Autonomous Driving (part 1)	1430 – 1600
Exhibition and Coffee Break 1600 – 1630 IP1 Interactive Presentations, Conference Level, Foyer				1600 – 1700
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
4.5 Test: innovative infrastructures and ATPG techniques	4.6 Special Session: Securing Power-constrained System-on-Chips: Challenges and Opportunities	4.7 Adaptive Reliable Computing Using Memristive and Reconfigurable Hardware	4.8 Components for Secure IoT Systems	1700 – 1830
EXHIBITION RECEPTION in the Exhibition Area				1830 – 1930

D-Track

A-Track

T-Track

E-Track

WEDNESDAY 21 MARCH, 2018

0730 Registration Speaker's Breakfast, Saal 1				
	Track 1	Track 2	Track 3	Track 4
	Saal 2	Konf. 6	Konf. 1	Konf. 2
0830–1000	5.1 Special Day Session on Future and Emerging Technologies: Challenges for the Design of Microfluidic Devices: EDA for your Lab-on-a-Chip	5.2 Smart Energy and Automotive Systems	5.3 Heterogeneous multi-level caching	5.4 Special Session: Lightweight Security for Resources-Constrained Internet-of-Things Applications
1000–1100	Exhibition and Coffee Break 1000–1030 IP2 Interactive Presentations Conference Level, Foyer			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1100–1230	6.1 Special Day Session on Future and Emerging Technologies: Transistors for Digital Nano-Systems: The Road Ahead	6.2 Memory Security	6.3 Advances in AMS/RF Design & Test Automation and Beyond	6.4 Modeling, Control and Scheduling for Cyber-Physical Systems
1230–1430	Lunch Break, Großer Saal + Saal 1 1345–1350 Awards Presentation 1350–1420 7.0 LUNCH TIME KEYNOTE SESSION Saal 2			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1430–1600	7.1 Special Day Session on Future and Emerging Technologies: Theoretical and practical aspects of verification of quantum computers	7.2 Run-time power estimation and optimization	7.3 Advances in Logic Synthesis and Technology Mapping	7.4 DRAM and NVMs
1600–1700	Exhibition and Coffee Break 1600–1630 IP3 Interactive Presentations Conference Level, Foyer			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1700–1830	8.1 Special Day Session on Future and Emerging Technologies: NanoSystems: Connecting Devices, Architectures, and Applications	8.2 EU Projects: Novel Technologies, Predictable Architectures and Worst-Case Execution Times	8.3 Real time intelligent methods for energy-efficient approaches in CNN and biomedical applications	8.4 Efficient and reliable memory and computing architectures
1930–2300	DATE Party Networking Event		Deutsches Hygiene-Museum (incl. Best Paper Awards & Best IP Award)	

WED keynote

Special Day Session

Special & EU Session

IP Session

Exhibition Theatre

Registration Speaker's Breakfast, Saal 1				0730
Track 5	Track 6	Track 7	TRACK 8	
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
5.5 Emerging Technologies for Future Computing	5.6 Reliability improvement and evaluation techniques	5.7 Software-centric techniques for embedded systems	0830–1000	
Exhibition and Coffee Break 1000 – 1030 IP2 Interactive Presentations Conference Level, Foyer				1000 – 1100
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
6.5 Special Session: Three Years of Low-Power Image Recognition Challenge			6.8 Innovative Products for Autonomous Driving (part 2)	1100 – 1230
Lunch Break, Großer Saal + Saal 1 1345 – 1350 Awards Presentation 1350 – 1420 7.0 LUNCH TIME KEYNOTE SESSION Saal 2				1230 – 1430
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
7.5 Reliability Modeling and Mitigation	7.6 Special Session: Next Generation Processors and Architectures for Deep Learning	7.7 Rigorous design, analysis, and monitoring of dependable embedded systems	7.8 22FDX – the superior technology for IoT, RF, Automotive and Mobility: Advanced Design Methodologies for Ultra-low Power Solutions	1430 – 1600
Exhibition and Coffee Break 1600–1630 IP3 Interactive Presentations Conference Level, Foyer				1600 – 1700
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
8.5 From NBTI to IoT security: industrial experiences	8.6 Designing reliable embedded architectures under uncertainty		8.8 22FDX – the superior technology for IoT, RF, Automotive and Mobility: Best-in-Class RF, 5G and mmWave designs	1700 – 1830
DATE Party Networking Event		Deutsches Hygiene-Museum (incl. Best Paper Awards & Best IP Award)		1930 – 2300

D-Track A-Track T-Track E-Track

0730 Registration Speaker's Breakfast, Saal 1				
	Track 1	Track 2	Track 3	Track 4
	Saal 2	Konf. 6	Konf. 1	Konf. 2
0830 – 1000	9.1 Special Day Session on Designing Autonomous Systems: Embedded Machine Learning	9.2 Emerging architectures and technologies for ultra low power and efficient embedded systems	9.3 Advances in Reconfigurable Computing	9.4 EU Projects: Novel Platforms – from Self-Aware MPSoCs to Server Ecosystems
1000 – 1100	Exhibition and Coffee Break 1000 – 1030 IP4 Interactive Presentations Conference Level, Foyer			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1100 – 1230	10.1 Special Day Session on Designing Autonomous Systems: Digitalization in automotive and industrial systems	10.2 Neural Networks and Neurotechnology	10.3 From Non-Volatile Flip-Flops to Storage Systems	10.4 Cryptographic Hardware
1230 – 1400	Lunch Break, Großer Saal + Saal 1 1320 – 1350 11.0 LUNCH TIME KEYNOTE SESSION Saal 2			
	Saal 2	Konf. 6	Konf. 1	Konf. 2
1400 – 1530	11.1 Special Day Session on Designing Autonomous Systems: Smart Vision Systems	11.2 Timing and Power Driven Physical Design	11.3 More than Moore Interconnects	11.4 Evaluating and optimizing memory and timing across HW and SW boundaries
1530 – 1600	Exhibition and Coffee Break 1530–1600 IP5 Interactive Presentations Conference Level, Foyer			
	Saal 2	Room	Room	Room
1600 – 1730	12.1 Special Day Session on Designing Autonomous Systems: Self-awareness for Autonomous Systems	12.2 Searching for corner cases, bugs and security vulnerabilities	12.3 Verification and Formal Synthesis	12.4 Hardware-assisted Security

THU keynote

Special Day Session

Special & EU Session

IP Session

Exhibition Theatre

Registration Speaker's Breakfast, Saal 1				0730
Track 5	Track 6	Track 7	TRACK 8	
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
9.5 Physical Attacks				0830 – 1000
CExhibition and Coffee Break 1000 – 1030 IP4 Interactive Presentations Conference Level, Foyer				1000 – 1100
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
10.5 Mixed-Criticality and Fault-Tolerant Real-Time Embedded Systems	10.6 Special Session: Computing with Ferroelectric FETs - Devices, Models, Systems, and Applications		10.8 An Industry Approach to FPGA and SOC System Development and Verification	1100 – 1230
Lunch Break, Großer Saal + Saal 1 1320 – 1350 11.0 LUNCH TIME KEYNOTE SESSION Saal 2				1230 – 1400
Konf. 3	Konf. 4	Konf. 5	Exhibition Theatre	
11.5 Microfluidic Devices and Inexact Computing	11.6 Memory: new technologies and reliability-related issues	11.7 Building Resistant Systems: From Temperature Awareness to Attack Resistance	11.8 A Powerful Framework for Functional Safety	1400 – 1530
Exhibition and Coffee Break 1530 – 1600 IP5 Interactive Presentations Conference Level, Foyer				1530 – 1600
Room	Room	Room	Room	
12.5 Lifetime Improvement for Persistent Memory	12.6 Special Session: Computing with Emerging Memories: How Good can it be?			1600 – 1730

FRIDAY 23 MARCH, 2018

0730 – Workshop Registration and Welcome Refreshments
0830

Breaks Please see individual workshop programmes
for lunch and break times

0830–1730 0830–1700 0830–1730 0830–1700
Konferenz 1 Konferenz 2 Konferenz 3 Konferenz 4

W01
Optical/Photonic
Interconnects for
Computing Systems
(OPTICS)

W02
Emerging Memory
Solutions &
Applications –
Technology,
Manufacturing,
Architectures,
Design, Automation
and Test

W03
New Platforms for
Future Cars: Current
and Emerging Trends

W04
Design Automation
for Understanding
Hardware Designs
(DUHDE5)

0830–1700
Konferenz 5

0830–1700
Konferenz 6

W05
Trustworthy
Manufacturing and
Utilization of Secure
Devices (TRUDEVICE
2018)

W06
Embedded Software
for Industrial IoTs
(ESIIT 2018)

DATE¹⁹



CONFERENCE &
EXHIBITION

March 25 – 29, 2019

Firenze Fiera, Florence, Italy

DATE²⁰



CONFERENCE &
EXHIBITION

March 09 – 13, 2020

Alpexpo, Grenoble, France

1330 **Tutorial and Conference Registration**1400-1530 **Tutorials**1530-1600 **Coffee Break**1600-1800 **Tutorials**1800–2100 **Welcome Reception & PhD Forum****M01****Design: Emerging Technologies for Computing – From Devices to Systems**

Konferenz 1 1400 - 1800

M02**Applications: Effective System Level Simulation Techniques and Cross-Layer Perspectives on Low Power Design**

Konferenz 2 1400 - 1800

M03**Test: Reliability: From Physics to CAD**

Konferenz 3 1400 - 1800

M04**Embedded: Industrial Internet-of-Things: Architectures, Designs and Challenges**

Konferenz 4 1400 - 1800

M05**Industrial A: How to Implement Domain-Specific Modeling Languages: Hands-on Tutorial**

Konferenz 5 1400 - 1800

M06**Industrial B: Building Arm Cortex-M Powered Internet of Things (IoT) Applications: From Design to Deployment**

Seminar 3+4 1400 - 1800

M07**Industrial C: Computer Vision for Automated Driving in MATLAB**

Seminar 5+6 1400 - 1800

Design: Emerging Technologies for Computing – From Devices to Systems

Konferenz 1 1400 - 1800

Speakers:

Iuliana Radu, imec, BE

Pierre-Emmanuel Gaillardon, University of Utah, US

Michael Niemier, University Of Notre Dame, US

This tutorial will provide a global picture of 3 candidate technologies to sustain the need for a higher level of performance at the twilight of Moore's Law. A first contribution will discuss spintronic Majority gates, that could prove beneficial to complex circuits with a large number of inputs and few outputs. This contribution will introduce some of the fundamentals of spintronics, describe how majority gates can be implemented with spintronics phenomena and benchmark various device options in terms of performance at circuit level. A second contribution will deal with functionality-enhanced electronics where, by exploiting unconventional physical properties, several nanodevices show an alternative to Moore's Law by the increase of their functionality rather than the pure scaling. This presentation will introduce Three-Independent-Gate Field Effect Transistors (TIGFETs), that can, depending on the bias applied to its gate, achieve different modes of operations, such as the dynamic re-configuration of the device polarity. Such property is highly desirable for logic computation, as it allows the realization of compact logic gates and circuits beyond the capabilities of CMOS. A third contribution will cover steep-slope electronics based on integrated ferroelectrics. This presentation will showcase recent experimental FeFET results and modeling efforts, as well as circuit design efforts.

Speakers:

Iuliana Radu is Distinguished Member of Technical Staff at imec responsible for Beyond CMOS and Quantum Computing activities at IMEC. Beyond CMOS activities include work on novel device concepts including spintronics and wave computing and novel materials and their possible applications in the semiconductor industry. Quantum Computing activities includes work on qubit devices and the periphery circuits meant to control them.

Pierre-Emmanuel Gaillardon is assistant professor in the Electrical and Computer Engineering (ECE) department and adjunct assistant professor in the School of Computing at The University of Utah, Salt Lake City, UT, where he leads the Laboratory for NanoIntegrated Systems (LNIS). He holds an Electrical Engineer degree from CPE-Lyon, France (2008), a M.Sc. degree in Electrical Engineering from INSA Lyon, France (2008) and a Ph.D. degree in Electrical Engineering from CEA-LETI, Grenoble, France and the University of Lyon, France (2011).

Michael T. Niemier is currently an Associate Professor at the University of Notre Dame. His research interests include designing, facilitating, benchmarking, and evaluating circuits and architectures based on emerging technologies. Currently, Niemier's research efforts are based on new transistor technologies, as well as devices based on alternative state variables such as spin.

Applications: Effective System Level Simulation Techniques and Cross-Layer Perspectives on Low Power Design

Konferenz 2 1400 - 1800

Speakers:

Andreas Herkersdorf, Technische Universität München, DE
Frédéric Pétrot, TIMA Laboratory, FR

This tutorial focusing on virtual prototyping and low power design targets graduate students and industry participants who would like to familiarize themselves with these two central aspects of embedded systems engineering.

Virtual prototyping is a technology being used by computer and embedded system designers to take design decisions, as a replacement for excel sheets and magical dimensioning formulas. It is also used by software developers in early hardware design stages, to avoid costly hardware devices or for continuous integration to ensure software quality. The first part is an introduction to virtual prototyping. We first present the different abstraction levels at which virtual prototyping can be used, and the technologies on which it relies. Then, we will describe the various instruction set execution strategies, and compare their benefits and limitations. Finally, we will introduce the issue of evaluating non functional properties of software, such as timing and power, in these environments.

The second part of the tutorial conveys an overview on various low power design techniques applicable at different hardware abstraction levels of SoC platforms in embedded systems. Starting with an analytic review on static and dynamic power consumption basics, we then go into the details of specific low power techniques. The concepts range from system level down to transistor level considerations tackling aspects such as: DVFS (dynamic voltage frequency scaling), power gating, clock gating, algorithmic transformations, scheduling for low power, substrate biasing, Silicon on Insulator.

Speakers:

Andreas Herkersdorf is a Full Professor and head of the Chair for Integrated Systems at Technical University of Munich. He teaches graduate courses in digital integrated circuit design, the application of System on Chip technology in networking and communications, and Hardware/Software-Codesign.

He joined the IBM Zurich Research Laboratory as a PhD student in 1988. In 1991, he became a Research Staff Member in the Communications Systems department of the IBM Zurich and in 2000 manager of the network processor hardware group.

Andreas Herkersdorf was born in 1961 in Oberstdorf, Germany. He received the Dipl.-Ing. degree from Munich University of Technology in 1987 and the Dr. techn. degree from the ETH Zurich (Swiss Federal Institute of Technology), Switzerland, in 1991, both in electrical engineering.

Frédéric Pétrot received the PhD degree in Computer Science from Université Pierre et Marie Curie (Paris VI), Paris, France, in 1994, where has been Assistant Professor in Computer Science until September 2004. From 1996 to 2004, he led a team focusing on the specification, simulation and implementation of multiprocessor SoCs. He joined Grenoble Institute of Technology, Grenoble, France, as Professor in September 2004. Since 2006, he heads the System Level Synthesis group of the TIMA laboratory where he is currently deputy director. His research interests are in multiprocessor systems on chip architectures, including circuits and software aspects, and CAD tools for the design and evaluation of hardware/software systems.

**Test:
Reliability: From Physics to CAD**

Konferenz 3 1400 - 1800

Speakers:**Hussam Amrouch**, Karlsruhe Institute of Technology (KIT), DE**Norbert Wehn**, University of Kaiserslautern, DE**Montserrat Nafria Maqueda**, Universitat Autònoma de Barcelona (UAB), ES

The motivation of this tutorial is to understand the newest research results in reliability from ground up. The first talk introduces new physical effects, known as time-dependent variability, that jeopardize circuit reliability. The second talk discusses aging effects and bridges the gap between physics and CAD. The third talk finally applies the implication of the effects to the memory subsystem.

Speakers:

Hussam Amrouch is a Research Group Leader at the Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), Germany. He is leading of the Dependable Hardware research group. He received his Ph.D. degree from KIT in 2015 with distinction (Summa cum laude). His main research interests are design for reliability, thermal-aware VLSI design, modeling and mitigating aging effects at the device and circuit levels. He holds five HiPEAC Paper Awards. He has recently three best paper nominations at DAC'16, DAC'17 and DATE'17 for his work on reliability. He currently serves as Associate Editor at Integration, the VLSI Journal.

Jörg Henkel is the Chair Professor for Embedded Systems at Karlsruhe Institute of Technology. Before that he was a research staff member at NEC Laboratories in Princeton, NJ. He received his diploma and Ph.D. (Summa cum laude) from the Technical University of Braunschweig. His research work is focused on co-design for embedded hardware/software systems with respect to power, thermal and reliability aspects. He has received six best paper awards throughout his career from, among others, ICCAD, ESWeek and DATE. For two consecutive terms he served as the Editor-in-Chief for the ACM Transactions on Embedded Computing Systems.

Montserrat Nafria received the Ph.D. degree in Physics from the Universitat Autònoma de Barcelona, Spain, in 1993, where she is currently a Full Professor at the Department of Electronic Engineering. Her major research interests include CMOS device and circuit reliability. Currently, she is working on the characterization and modelling of the aging (BTI and channel hot carrier degradations) and variability of advanced MOS devices. This is done from the nanoscale level, by studying the phenomena using Atomic Force Microscope-related techniques, up to circuit level.

Norbert Wehn holds the chair for Microelectronic System Design in the department of Electrical Engineering and Information Technology at the University of Kaiserslautern. He has more than 300 publications in various fields of microelectronic system design and holds several patents. Two start-ups spinout of his research group. He is associate editor of various journals and member of several scientific advisory boards. In 2003 he served as program chair for DATE 2003 and as general chair for DATE 2005 respectively. In 2014 he was general Co-Chair of FPL 2015. He received several best paper awards.

1400

Talk 1: Characterization and Compact Modeling of Time-Dependent Variability Effects in Ultra-Scaled CMOS

Speaker: Montserrat Nafria, Universitat Autònoma de Barcelona, ES

Time Dependent Variability (TDV) in scaled CMOS technologies provokes uncertainty in the electrical characteristics of transistors, which will be transferred to the circuit performance. In the Design-for-Reliability context, understanding the phenomenology behind TDV is fundamental to explore new techniques for the design of reliable circuits. Several mechanisms are the main responsible of TDV in current and future CMOS technologies. In this tutorial, the physical origin and the characterization challenges of the main mechanisms (Random Telegraph Noise, Bias Temperature Instabilities and Channel Hot Carriers Injection) will be presented. The latest advances in the device TDV physics-based compact modeling will be also addressed.

1520

Talk 2: Aging Effects: From Physical to System Level

Speakers: Hussam Amrouch, Karlsruhe Institute of Technology, DE
Jörg Henkel, Karlsruhe Institute of Technology, DE

Due to aging, circuit reliability has become extraordinary challenging. Reliability-aware circuit design flows do virtually not exist and even research is in its infancy. In this presentation, first we will demonstrate how we can bring aging awareness to existing EDA tool flows based on so-called degradation-aware cell libraries. These libraries include detailed delay information of gates/cells under the impact that aging has on the key parameters of MOSFET transistors. We will also demonstrate that degradation-aware libraries and tool flows are indispensable for not only accurately estimating guardbands, but also efficiently containing them. Then, we will explain how to our degradation-aware cell libraries can be employed within the standard tool flows to quantify the impact of aging at the system level in the context of image processing. This goes far beyond investigating aging with respect to circuits' path delays solely as often done in state of the art. Afterwards, we will demonstrate how nondeterministic aging-induced timing errors can be converted into deterministic and controlled approximations instead. This enables designers for the first time to narrow or even remove guardbands through exploring application of approximate computing principles in the context of aging. Finally, we will demonstrate how the existing view of aging in the state of the art needs to be updated. In fact, aging has been, traditionally, assumed to be a long-term reliability degradation in which its effects are observed in the order of months and years. However, in the deep nano technology, aging has shifted from a sole long-term to a short- and long-term reliability challenge. We will explain why circuits designers need to take that into account when employing guardbands (i.e. safety margins) at the design time. Otherwise, reliability cannot be sustained at runtime. At the end of our presentation, we will distribute to the attendees USB drives, which

1640

Talk 3: Dependability Issues in Memories

Speaker: Norbert Wehn, University of Kaiserslautern, DE

All today's computing systems rely on an ever increasing amount of (external) memory. Dynamic Random Access Memories (DRAMs) play a central role in this memory hierarchy. DRAMs exhibit a large variation in their parameters and in the future memories such as DRAMs will become even more undependable due to further scaling. This has to be counterbalanced error detection and error correction codes and with higher refresh rates, which leads to a higher DRAM power consumption. Recent research activities resulted in the concept of "approximate DRAM" to save power and improve performance by lowering the refresh rate or disabling refresh completely. In this talk we will give an overview on the aforementioned DRAM challenges, present techniques to mitigate these problems and present a holistic simulation environment for investigations on approximate DRAM and the impact on error resilient applications.

Embedded: Industrial Internet-of-Things: Architectures, Designs and Challenges

Konferenz 4 1400 - 1800

Speakers:

Athanasios Kalogeras, ISI/ATHENA RC, GR

Christos Koulamas, ISI/ATHENA RC, GR

Dimitrios Serpanos, ISI/ATHENA RC, GR

The Industrial Internet-of-Things (IIoT) is one of the leading application domains of the Internet of Things (IoT) and a driving application area for semiconductors and computer systems. Its strong requirements for real-time and safety properties make IIoT system and network design key challenges for design automation and VLSI. IIoT has been leading IoT development and deployment for a long time. The recent efforts of Industrie 4.0 and the Industrial Internet Consortium (IIC) demonstrate the importance of IIoT, following the increasing adoption of IIoT technologies, methods and applications in domains such as critical infrastructure monitoring and control, manufacturing, avionics, etc. This tutorial will identify key aspects of IIoT systems, important design and CAD challenges, and discuss tools and methodologies.

Speakers:

Dr. Athanasios Kalogeras holds a Ph.D. in Electrical and Computer Engineering from the University of Patras, Greece. He has over 20 years of research experience. He is currently a Principal Researcher at the Industrial Systems Institute of the Athena Research and Innovation Center in Greece. He has over 80 publications in journals, conference proceedings and collective volumes. His research interests include smart manufacturing systems and processes, Cloud manufacturing, enterprise information systems, enterprise integration and interoperability, semantics for the manufacturing environment, industrial networking and informatics.

Dr. Christos Koulamas holds a PhD in Electrical & Computer Engineering and a Diploma in Computer Engineering and Informatics. He is Principal Researcher at the Industrial Systems Institute (ISI), ATHENA Research and Innovation Centre in Patras, Greece. He has more than 20 years of experience in R&D, in the areas of real-time distributed embedded systems, industrial communications, wireless sensor networks, and their applications in industrial & building automation and energy management systems, holding various positions in the industrial and academic sectors.

Prof. Dimitrios Serpanos is the Director of the Industrial Systems Institute/ATHENA RC, Vice Chairman of the Board of Directors of ATHENA RC and a Professor of Electrical and Computer Engineering, University of Patras, Greece. He holds a PhD in Computer Science from Princeton University (1990) and an Engineering Diploma in Computer Engineering and Informatics from the University of Patras (1985). Professor Serpanos has published widely in books, journals and conferences and holds two US patents. He was a founding member of the organizing committee of WESS (Workshop on Embedded Systems Security)/ESWEEK (2006-2015). He served as general or TPC chair at several IEEE conferences, and as TPC member at more than 100 events. He is associate editor of IEEE TII and served as associate editor of ACM TECS (2003-2016) and other journals.

M05

Industrial A: How to Implement Domain- Specific Modeling Languages: Hands-on Tutorial

Konferenz 5 1400 - 1800

Speaker: Juha-Pekka Tolvanen, MetaCase, FI

You've probably heard people say that defining a graphical modeling language is difficult and time-consuming. In this tutorial, we will lay bare this fallacy and demonstrate how simple and quick it is to create domain-specific languages and their generators. Using a hands-on approach you will define several modeling languages and generators within a few hours, learning principles and best practices proven in industrial experience. Even existing models update when the language is refined. The tutorial teaches practical, repeatable steps to invent and implement DSL. The language definition process reveals the characteristics of DSLs that enable generating working code from models:

- DSL is based on the concepts of problem domain rather than code
- Scope of the language narrowed down to a particular domain
- Language minimizes the effort needed to create, update and check the models
- Language supports communication with users and customers

Participants will learn how to define domain-specific modeling languages, including proven practices. During the tutorial we focus on medical devices and creating DSLs for their development. We also inspect modeling support and generators made in the industry for various embedded systems, like telecommunication, consumer electronics and industry automation systems.

This tutorial is an interactive tutorial where participants will define a modelling language for a narrow domain. Organizers will provide a sample case (from common and known application domains) and moderate the groups for making sure they make progress, without leading them in any particular direction. Language creation can be done in any technology or tool that is available for the participants. For the rest organizers will provide tools for language creation and participants should bring their own laptop for the class. No prior experience on language creation is required, but participants should have experience on using at least one modeling tool. Tutorial material includes slides and description of the domain to be tackled in the hands-on part.

Speaker:

Dr. Juha-Pekka Tolvanen works for MetaCase. He has been involved in domain-specific languages and tools since 1991 and acted as a consultant world-wide on their use. Juha-Pekka has co-authored a book (Domain-Specific Modeling, Wiley) and over 70 articles in software development magazines and conferences. Juha-Pekka holds a Ph.D. in computer science and he is an adjunct professor at the University of Jyväskylä.

Industrial B: Building Arm Cortex-M Powered Internet of Things (IoT) Applications: From Design to Deployment

Seminar 3+4 1400 - 1800

Speakers:

Xabier Iturbe, ARM Research, GB

Victor Nelson, Auburn University, US

An Internet of Things (IoT) system comprises a network of intelligent devices (Things) and a central server. The Things are low-cost, energy-efficient systems that comprise sensors, processor, memory, and communication capability. These Things periodically sample and transmit local data to the server, which analyzes the data and makes system-level decisions. In this workshop, attendees will be exposed to the design of a System-on-Chip (SoC) to power an IoT Thing, and the creation of a complete IoT system using these SoCs. The SoC will be designed around an Arm Cortex-M0 processor and will be using components provided by the Arm University Program.

Using hardware and software tools from Xilinx and Keil, and guided by the Workshop presenters, attendees will create, simulate and program their own Arm-powered SoC on a Numato Labs Mimas V2 FPGA board. The last step will consist on integrating all SoCs created by the attendees into an IoT network and communicating wirelessly with a server, thus demonstrating a complete IoT system.

Note that attendees to this Workshop will need to bring their own laptop. They will also have to download the Cortex-M0 files from the Arm DesignStart website and install the required software tools in their laptops in advance. The number of participants in this workshop will be limited to 40-50.

Speakers:

Xabier Iturbe is the Arm University Program EMEA Manager. He manages the Arm technology outreach to universities in the EMEA region to enable and promote Arm-based education and research. Xabier holds a PhD in Electronics Engineering from the University of Edinburgh.

Victor P. Nelson is Professor and Assistant Chair of Electrical and Computer Engineering at Auburn University. His primary teaching research interests include embedded systems, digital system design with FPGAs, and computer-aided design of application-specific integrated circuits (ASICs). He is co-author of the textbook Digital Logic Circuit Analysis and Design and IEEE tutorial book Fault-Tolerant Computing.

M07

Industrial C: Computer Vision for Automated Driving in MATLAB

Seminar 5+6 1400 - 1800

Speaker:**Alexander Schreiber**, The MathWorks, DE

Automated driving has revolutionized the automotive industry in the last few years because of the tremendous impact it can have on road safety, and computer vision has a crucial role to play in this space. This tutorial will cover both theoretical and practical aspects of developing, implementing and evaluating automated driving systems with real world examples of how companies are using our tools. This session will cover topics like camera calibration and co-ordinate transformation, object detection using deep learning, sensor fusion and tracking, and point cloud processing.

We will briefly introduce new functionality in MATLAB to support automated driving workflows, including camera calibration and co-ordinate system transforms, deep learning for object detection, sensor fusion and point cloud processing for LIDAR. We will demonstrate practical approaches to calibrating an in-vehicle camera and explain how to convert between image and vehicle co-ordinate systems. Deep learning is key to having a vehicle perceive its environment. This session will cover object detection in the context of an ADAS system using deep learning techniques such as Faster R-CNN and YOLO. We will demonstrate practical applications of speeding up training using multiple GPUs, and show how to leverage geometric constraints of an in-vehicle camera to accelerate processing and reduce false alarm rate. Additionally, we will show how to verify object detection results against ground truth data.

We will talk about practical aspects of designing a tracking and sensor fusion system. We will also show how to test and verify the reliability of the system by creating and using synthetic data.

We will show how to represent, display and process point clouds from LIDAR in MATLAB. You will learn practical techniques for efficient search, subsampling, as well as filtering from point cloud data in the context of common ADAS problems like ground plane estimation and obstacle detection.

Speaker:

Alexander Schreiber joined the Application Engineering department of MathWorks in 2008 and works as Principal Application Engineer and Technical Account Manager. He covers application areas of autonomous systems design, HW/SW co-design, automatic code generation and verification (HDL, C). Prior to joining MathWorks he worked as ASIC Designer and Project Manager for EDA and semiconductor companies. He holds an M.Sc. equivalent degree in Electrical Engineering from the University of Stuttgart.

DATE18

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20 – 22 MARCH, 2018

1.1

Opening Session: Plenary, Awards Ceremony & Keynote Addresses

Tuesday, March 20, 2018

0830 – 1030

International Congress Center Dresden, Germany

Großer Saal

Chair: Jan Madsen, Technical University of Denmark, DK

Co-Chair: Ayse K. Coskun, Boston University, US

0830

Welcome Addresses

Jan Madsen

DATE 2018 General Chair

Ayse K. Coskun

DATE 2018 Programme Chair

0845

Presentation of awards

2018 EDAA Achievement Award

(Mary Jane Irwin, Emerita Evan Pugh University Professor, US)

EDAA Outstanding Dissertations Award 2017

DATE Fellow Award

(David Atienza, EPFL, CH)

IEEE Fellow Award

(Tajana Simunic Rosing, University of California San Diego, US)

IEEE CEDA and CS TTTC Outstanding Service

Contribution Award 2017

(David Atienza, EPFL, CH)

0915

Keynote Addresses

0915

1.1.1 Keynote Address:

The Responsibility Sensitive Safety (RSS) Formal Model toward Safety Guarantees for Autonomous Vehicles

Amnon Shashua, CEO & CTO, Mobileye, an Intel company, and Senior Vice President, Intel Corporation, US

1000

1.1.2 Keynote Address:

Programming Living Cells: Design Automation to Map Circuits to DNA

Christopher Voigt, Professor of Biological Engineering at MIT, US

1030

Coffee Break in the Exhibition Area

2.1

Executive Panel: How Electronics May Change Our Lives, and the World

Saal 2 1130 - 1300

Chair: Antun Domic, Synopsys, US

Innovation runs strong in our industry. A 17 qubits Quantum Computer (QC) has been shipped to Delft University researchers; an initiative to make cloud QC commercially available for businesses and research has been announced; if, and once available QC may change the landscape of finance, imaging diagnostics, pharmacology, meteorology and, of course, security all the way. After decades of domination by general purpose CPU and GPU, innovation is disrupting computing architectures: Massively parallel Tensor Processing Units (TPU) have demonstrated that a computer can learn from past experience, and then beat a 9-dan human professional Go player, or classify zillions of images with unprecedented accuracy and speed. Autonomous "Things" in which a wide breadth of sensors feed a processor with huge amounts of data, that are analyzed in order to make decisions that are then sent to actuators with minimal if any human supervision are emerging; Advanced Driver-Assistance Systems (ADAS) are the top of the iceberg, exceeding SAE level 3 requirements, ADAS have been adopted by scores of automakers, and all the top 10 automakers have already announced plans toward SAE level 4, and 5 availability before the end of this decade. Finally, computers are digital, but the world is analog; scores of sensors and actuators are the eyes, the ears, the nose, and the arms of the most advanced processors, and the most advanced applications could not exist without them. Today, sensors are designed at the established technology nodes, and often manufactured using electro-mechanical processes which make their integration with their host processors challenging. Is this going to continue, or will they be submerged by digital, and eventually be designed, integrated, and manufactured using the very same emerging technology nodes? Electronics may truly change our lives, and the world, IF we will be able to expand the scope of QC beyond cryptography, and the scope of AI beyond image recognition, IF ADAS technology will not be overwhelmed by legal. IF "More than Moore" will join forces with "More of Moore". IF... This Executive Panel, moderated by Dr. Antun Domic, Synopsys CTO, gathers world experts to discuss the many opportunities that lie ahead, and the challenges to be overcome

Panelists:

Martin Roetteler, Microsoft, US

Horst Symanzik, Bosch Sensortec, DE

Olivier Temam, Google, US

Loic Lietar, Greenwaves Technologies, FR

Martin Duncan, STMicroelectronics, IT

1300

Lunch Break in Großer Saal and Saal 1

2.2

Energy Efficient Neural Networks

Konf. 6 1130 - 1300

Chair: Hai (Helen) Li, Duke University, US

Co-Chair: Muhammad Shafique, Vienna University of Technology (TU Wien), AT

This session focuses on energy efficient neural network architectures. The first paper proposes a methodology that enables aggressive voltage scaling of accelerator weight memories to improve the energy-efficiency of DNN accelerators. The second paper introduces methods to optimize the memory usage in DNN training. The third paper presents HyperPower, that enables efficient Bayesian optimization and random search in the context of power- and memory-constrained hyper- parameter optimization for NNs running on a given hardware platform. Finally, the last paper presents a new sparse matrix format to maximize the inference speed of the LSTM accelerator. The session also includes 2 IP papers ReCom and SparseNN, which both focus on energy efficiency of neural networks.

- 1130 **MATIC: Learning Around Errors for Efficient Low-Voltage Neural Network Accelerators**
Speaker: Sung Kim, University of Washington, US
Authors: Sung Kim, Patrick Howe, Thierry Moreau, Armin Alaghi, Luis Ceze and Visvesh Sathe, University of Washington, US
- 1200 **Maximizing System Performance by Balancing Computation Loads in LSTM Accelerators**
Speaker: Junki Park, POSTECH, KR
Authors: Junki Park¹, Jaeha Kung¹, Wooseok Yi² and Jae-Joon Kim¹
¹Pohang University of Science and Technology, KR; ²POSTECH CITE, KR
- 1230 **moDNN: Memory Optimal DNN Training on GPUs**
Speaker: Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, CN
Authors: Xiaoming Chen, Danny Z. Chen and Xiaobo Sharon Hu, University of Notre Dame, US
- 1245 **HyperPower: Power- and Memory-Constrained Hyper-Parameter Optimization for Neural Networks**
Speaker: Dimitrios Stamoulis, Carnegie Mellon University, US
Authors: Dimitrios Stamoulis¹, Ermao Cai¹, Da-Cheng Juan² and Diana Marculescu¹
¹Carnegie Mellon University, US; ²Google Research, US
- IPs **IP1-1, IP1-2**
- 1300 Lunch Break in Großer Saal and Saal 1

2.3 High-Level Synthesis

Konf. 1 1130 - 1300

Chair: Selma Saidi, Hamburg University of Technology, DE
Co-Chair: Daniel Ziener, Science University of Twente Zilverling, NL

This session addresses high-level synthesis for easing the development of application-specific designs. First, user-guided optimizations for high-level synthesis based on innovative resource prediction using CNNs will be discussed for an area-reduction advisor. The second paper proposes a look-ahead scheduling scheme to minimize the area for functional units. The final talk presents a direct HLS synthesis path of software-customizable floating-point cores that does not rely on external libraries or floating-point code generators.

- 1130 **Sensei: An Area-Reduction Advisor for FPGA High-Level Synthesis**
Speaker: Hsuan Hsiao, University of Toronto, CA
Authors: Hsuan Hsiao and Jason H. Anderson, University of Toronto, CA
- 1200 **A Fast and Effective Lookahead and Fractional Search Based Scheduling Algorithm For High-Level Synthesis**
Speaker: Shantanu Dutt, University of Illinois at Chicago, US
Authors: Shantanu Dutt and Ouwen Shi, University of Illinois at Chicago, US
- 1230 **High-Level Synthesis of Software-Customizable Floating-Point Cores**
Speaker: Hsuan Hsiao, University of Toronto, CA
Authors: Samridhi Bansal¹, Hsuan Hsiao¹, Tomasz Czajkowski² and Jason H. Anderson¹
¹University of Toronto, CA; ²Intel Corp., CA
- IPs **IP1-3**
- 1300 Lunch Break in Großer Saal and Saal 1

2.4

Model Checking

Konf. 2 1130 - 1300

Chair: Armin Biere, JKU Linz, AT**Co-Chair:** Daniel Große, University Bremen, DE

The session consists of four papers on model checking. It ranges from model checking of multiple properties, improving bit-level model checking, checking specific properties in processor design to software model checking of the Linux kernel.

1130

Efficient Verification Of Multi-Property Designs (The Benefit Of Wrong Assumptions)

Speaker: Eugene Goldberg, Diffblue, US

Authors: Eugene Goldberg¹, Matthias Gudemann², Daniel Kroening³ and Rajdeep Mukherjee⁴¹DiffBlue, US; ²DiffBlue, DE; ³DiffBlue, GB; ⁴Oxford University, GB

1200

Combining PDR and Reverse PDR for Hardware Model Checking

Speaker: Tobias Seufert, University of Freiburg, DE

Authors: Tobias Seufert and Christoph Scholl, University Freiburg, DE

1230

Symbolic Quick Error Detection Using Symbolic Initial State for Pre-Silicon Verification

Speaker: Mohammad Rahmani Fadiheh, University of Kaiserslautern, DE

Authors: Mohammad Rahmani Fadiheh¹, Joakim Urdahl¹, Srinivasa Shashank Nuthakki², Subhasish Mitra², Dominik Stoffel¹ and Wolfgang Kunz¹¹University of Kaiserslautern, DE; ²Stanford University, US

1245

Verification of Tree-Based Hierarchical Read-Copy Update in the Linux Kernel

Speaker: Paul McKenney, IBM Linux Technology Center, US

Authors: Lihao Liang¹, Paul McKenney², Daniel Kroening¹ and Tom Melham¹¹University of Oxford, GB; ²IBM Linux Technology Center, US

1300

Lunch Break in Großer Saal and Saal 1

2.5

GPU and GPU-based heterogeneous system management

Konf. 3 1130 - 1300

Chair: Andrea Marongiu, Università di Bologna, IT**Co-Chair:** Carles Hernandez, BSC, ES

GPUs are at the heart of several modern heterogeneous systems, where the common communication paradigm between the CPU and the GPU is shared memory. The papers in this session propose novel techniques to deal with i) efficient shared memory management and ii) GPU multiprocessor scheduling in presence of process variation. The first paper focuses on GPU-based heterogeneous systems with a shared last-level cache (SLLC) and proposes a novel metric that combines CPU/GPU miss count and "hit utility" to devise an effective cache-way partitioning. The second paper proposes a technique to mitigate the negative effects of cache and memory controller sharing in GPUs running multiple workloads. The third paper discusses a HW technique to mitigate the effects of hardware variability (e.g., process variations (PVs) and negative bias temperature instability (NBTI)) in GPU Streaming Processors (SPs).

1130

HVSM: Hardware-Variability Aware Streaming Processors' Management Policy in GPUs

Speaker: Kaige Yan, Jilin University, CN

Authors: Jingweijia Tan¹ and Kaige Yan²¹Jilin University, CN; ²College of Communication Engineering, Jilin University, CN

- 1200 **Throughput Optimization and Resource Allocation on GPUs under Multi-Application Execution**
Speaker: Iraklis Anagnostopoulos, Southern Illinois University Carbondale, US
Authors: Srinivasa Reddy Punyala, Theodoros Marinakis, Arash Komae and Iraklis Anagnostopoulos, Southern Illinois University Carbondale, US
- 1230 **Set Variation-aware Shared Last-level Cache Management for CPU-GPU Heterogeneous Architecture**
Speaker: Xin Li, Shandong University, CN
Authors: Zhaoying Li, Lei Ju, Hongjun Dai, Xin Li, Mengying Zhao and Zhiping Jia, Shandong University, CN
- IPs **IP1-4**
- 1300 Lunch Break in Großer Saal and Saal 1

2.6 Circuit Locking and Camouflaging

Konf. 4 1130 - 1300

Chair: Debdeep Mukhopadhyay, IIT Kharagpur, IN
Co-Chair: Yiorgos Makris, UT Dallas, US

Intellectual property piracy, counterfeiting and reverse-engineering are serious threats for the supply chain in advanced microelectronics. This session presents novel approaches to protect circuits against these threats. The techniques deploy nanotechnology and novel timing scheme to obtain efficient protections.

- 1130 **Cyclic Locking and Memristor-based Obfuscation Against CycSAT and Inside Foundry Attacks**
Speaker: Hai Zhou, Northwestern University, US
Authors: Amin Rezaei, Yuanqi Shen, Shuyu Kong, Jie Gu and Hai Zhou Northwestern University, CN
- 1200 **Timing Camouflage: Improving Circuit Security against Counterfeiting by Unconventional Timing**
Speaker: Li Zhang, Technical University of Munich, DE
Authors: Grace Li Zhang¹, Bing Li², Bei Yu³, David Z. Pan⁴ and Ulf Schlichtmann²
¹TU München (TUM), DE; ²TU München, DE; ³The Chinese University of Hong Kong, HK; ⁴University of Texas at Austin, US
- 1230 **Advancing Hardware Security Using Polymorphic and Stochastic Spin-Hall Effect Devices**
Speaker: Satwik Patnaik, New York University, AE
Authors: Satwik Patnaik¹, Nikhil Rangarajan¹, Johann Knechtel², Ozgur Sinanoglu² and Shaloo Rakheja¹
¹New York University, US; ²New York University Abu Dhabi (NYUAD), AE
- 1300 Lunch Break in Großer Saal and Saal 1

2.7 Special Session: Spintronics based New Computing Paradigms and Applications

Konf. 5 1130 - 1300

Chair: Zhao Weisheng, Beihang University, CN
Co-Chair: Tahoori Mehdi, Karlsruhe Institute of Technology, DE

In recent technology nodes, the well-known "moore's law" tends to slow down. Indeed, the continuously decreasing size of the CMOS transistors and operating frequencies result in serious power consumption, heat dissipation and reliability issues. Among the solutions investigated to overcome these limitations, the use of emerging nano-devices mixed (or

not) with CMOS circuits is often referred as the « More than Moore » concept. In particular, logic circuits based on non-volatile memories can be an efficient solution to reduce the power, to improve the reliability and can offer new paradigms for computing. We are convinced that this research field has become a hot topic for the DATE community. The aim of this session is to bring together the worldwide leading experts (from USA, Belgium, China, and Germany, respectively) related to this hot topic to share the most recent results and discuss the future challenges. Different computing paradigms will be involved in this special session benefiting from interesting nature of spintronics devices. The invited speakers will talk about devices, design and compact modeling aspects, and applications, permitting a full development platform from devices to circuit & systems based on spintronics.

- 1130 Main memory organization trade-offs with DRAM and STT-MRAM options based on extended GEM5/ NVMAIN simulation framework**
 Speaker: Manu Komalan, IMEC, BE
 Authors: Manu Komalan¹, Oh Hyung Rock¹, Matthias Hartmann¹, Sushil Sakhare¹, Christian Tenllado², Jose Ignacio Gomez², Gouri Sankar Kar¹, Arnaud Furnemont¹, Francky Catthoor¹, Sophie Senni³, David Novo⁴, Abdoulaye Gamatie⁵ and Lionel Torres⁶
¹IMEC, BE; ²Universidad Complutense de Madrid (UCM), ES; ³LIRMM, FR; ⁴French National Centre for Scientific Research (CNRS), FR; ⁵CNRS LIRMM / University of Montpellier, FR; ⁶University of Montpellier, FR
- 1145 Exploring the Opportunity of Implementing Neuromorphic Computing Systems with Spintronic Devices**
 Speaker: Hai Li, Duke University, US
 Authors: Bonan Yan¹, Fan Chen¹, Yaojun Zhang², Chang Song¹, Hai (Helen) Li³ and Yiran Chen¹
¹Duke University, US; ²University of Pittsburgh, US; ³Duke University/TUM-IAS, US
- 1200 Spintronic Normally-off Heterogeneous System-on-Chip Design**
 Speaker: Rajendra Bishnoi, Karlsruhe Institute of Technology, DE
 Authors: Anteneh Gebregiorgis, Rajendra Bishnoi and Mehdi Tahoori, Karlsruhe Institute of Technology, DE
- 1215 Magnetic Skyrmions for Future Potential Memory and Logic Applications: Alternative Information Carriers**
 Speaker and Author: Wang Kang, Beihang University, CN
- 1230 Novel application of spintronics in computing, sensing, storage and cybersecurity**
 Speaker: Anirudh Iyengar, Pennsylvania State University, US
 Author: Swaroop Ghosh, Pennsylvania State University, US
- 1245 Large scale, high density integration of All Spin Logic**
 Speaker and Author: Jacques-Olivier Klein, C2N, Univ. Paris-Sud, FR
- 1300 Lunch Break in Großer Saal and Saal 1**

2.8

Enabling ICT Innovations for European SMEs

Exhibition Theatre 1130 - 1300

Organisers: Rainer Leupers, RWTH Aachen, DE

Bernd Janson, ZENIT GmbH, DE

Moderator: Luca Fanucci, University of Pisa, IT

Technology-driven business in Europe fails more often compared to other regions such as the USA and China. Turning results into products is a challenge which starts at the very beginning of an idea for a new technology and obliges researchers to cooperate with business experts and investors. The European Commission started its Smart Anything Everywhere (SAE) Initiative to foster transfer from research to business in the areas of Cyber Physical Systems (CPS) and via the instrument of Digital

Innovation Hubs (DIH). Two SAE Initiative projects will be presented in the workshop session, supported by two speakers from industry presenting their products consisting of programming technology SLX (Silexica) and software for automated driving (BASELABS). The workshop session will introduce the SAE approach and their individual funding schemes for European university-industry cooperation. The technology transfer concept focuses on direct cooperation between universities and SMEs supported by open innovation networks and other stakeholders like investors. The session speakers will demonstrate in a pragmatic way and by use of concrete examples how technology transfer can be initiated and implemented in practice and to overcome the associated pitfalls and use the innovation opportunities. The mix of presentations ensures that both academic and industrial viewpoints and concerns are adequately addressed. The workshop session will hence be of interest to a large audience. Amongst others, the goal is to motivate more stakeholders to engage in international technology transfer. During the session, SAE representatives will share their experiences and insights as researcher, founder, entrepreneur, investor or consultant.

- 1130 **Presentation of TETRAMAX**
Speaker: Rainer Leupers, RWTH Aachen, DE
- 1145 **The FED4SAE project, accelerating European CPS solutions to market**
Speaker: Isabelle Dor, CEA, FR
- 1200 **Open innovation business based on efficient networking**
Speaker: Bernd Janson, ZENIT GmbH, DE
- 1215 **The Silexica multicore solution**
Speaker: Juan Eusse, Silexica GmbH, DE
- 1230 **Transferring Research Results to Safety-Relevant Products: Case Study on Automated Driving Software**
Speaker: Robert Schubert, BASELABS GmbH, DE
- 1245 **Intenta GmbH**
Speaker: Basel Fardi, Intenta GmbH, DE
- 1300 Lunch Break in Großer Saal and Saal 1

3.1

Executive Session: Design Automation for Quantum Computing

Saal 2 1430 - 1600

Chair: Charbon Edoardo, TU Delft / EPFL, NL

Co-Chair: Große Daniel, University of Bremen, DE

Recent developments in quantum hardware indicate that systems featuring more than 50 physical qubits are within reach. At this scale, classical simulation will no longer be feasible and there is a possibility that such quantum devices may outperform even classical supercomputers at certain tasks. With the rapid growth of qubit numbers and coherence times comes the increasingly difficult challenge of quantum program compilation. This entails the translation of a high-level description of a quantum algorithm to hardware-specific low-level operations which can be carried out by the quantum device. Some parts of the calculation may still be performed manually due to the lack of efficient methods. This, in turn, may lead to a design gap, which will prevent the programming of a quantum computer. In this session, we discuss the challenges in fully-automatic quantum compilation. We motivate directions for future research to tackle these challenges. Yet, with the algorithms and approaches that exist today, we demonstrate how to automatically perform the quantum programming flow from algorithm to a physical quantum computer for a simple algorithmic benchmark, namely the hidden shift problem. We present and use two tool flows which invoke RevKit. One which is based on ProjectQ and which targets the IBM Quantum Experience or a local simulator, and one which is based on Microsoft's quantum programming language Q#.

- 1430 **Quantum algorithms: the quest for scalable programming, synthesis, and test**
Author: Martin Roetteler, Microsoft, US
- 1500 **ProjectQ: A software framework for programming quantum computers**
Author: Thomas Haener, ETHZ, CH
- 1530 **RevKit: Automatic compilation and design space exploration for quantum programs**
Author: Mathias Soeken, EPFL, CH
- 1600 Coffee Break in Exhibition Area

3.2

Approximate and Near-Threshold Computing

Konf. 6 1430 - 1600

Chair: Semeen Rehman, Vienna University of Technology (TU Wien), AT
Co-Chair: Saibal Mukhopadhyay, Georgia Tech., US

This session focuses on approximate and near-threshold computing. The first paper proposes a novel dynamic virtual machine (VM) allocation method, while guaranteeing quality of service (QoS) requirements. The second paper introduces and presents an adaptive simulation methodology in which neurons in the region of interest (ROI) follow highly accurate biological models while the other neurons follow computation-friendly models. Finally the last paper shows an approximate computing technique to perform approximate computing with memory, avoiding redundant computation when encountering similar input patterns. The session also includes one IP paper on approximate big data computing.

- 1430 **Energy Proportionality in Near-Threshold Computing Servers and Cloud Data Centers: Consolidating or Not?**
Speaker: Ali Pahlevan, Embedded Systems Laboratory (ESL), EPFL, CH
Authors: Ali Pahlevan¹, Yasir Mahmood Qureshi¹, Marina Zapater¹, Andrea Bartolini², Davide Rossi³, Luca Benini⁴ and David Atienza¹
¹Embedded Systems Lab (ESL), EPFL, CH; ²ETH Zurich, CH; ³Energy Efficient Embedded Systems (EEES) Lab – DEI, University of Bologna, IT; ⁴Integrated System Laboratory ETH, Zurich, CH
- 1500 **Lookup Table Allocation for Approximate Computing with Memory under Quality Constraints**
Speaker: Ye Tian, The Chinese University of Hong Kong, HK
Authors: Ye Tian, Qian Zhang, Ting Wang and Qiang Xu, The Chinese University of Hong Kong, HK

1530 **Accelerating Biophysical Neural Network Simulation with Region of Interest based Approximation**

Speaker: Yun Long, Georgia Institute of Technology, US
 Authors: Yun Long, Xueyuan She and Saibal Mukhopadhyay, Georgia Institute of Technology, US

IPs **IP1-5**

1600 Coffee Break in Exhibition Area

3.3 Optimization Techniques for MPSoCs

Konf. 1 1430 - 1600

Chair: Stefan Wildermann, FAU Erlangen-Nuremberg, DE
Co-Chair: Michael Glass, Ulm University, DE

This session presents innovative techniques for optimizing several aspects in multi-processor/core system design. The first paper proposes an effective and efficient design space exploration technique for designing domain-specific platforms. The second paper proposes a novel task allocation and scheduling scheme to maximize soft-error reliability while satisfying lifetime reliability constraints for soft-real-time MPSoCs. Third paper proposes a virtual resource manager that monitors the access behavior and predicts the node-to-node interconnect performance.

1430 **DS-DSE: Domain-Specific Design Space Exploration for Streaming Applications**

Speaker: Jinghan Zhang, Northeastern University, US
 Authors: Jinghan Zhang, Hamed Tabkhi and Gunar Schirner, Northeastern University, US

1500 **Variation-Aware Task Allocation and Scheduling for Improving Reliability of Real-Time MPSoCs**

Speaker: Junlong Zhou, Nanjing University of Science and Technology, CN
 Authors: Junlong Zhou¹, Tongquan Wei², Mingsong Chen², Xiaobo Sharon Hu³, Yue Ma³, Gongxuan Zhang¹ and Jianming Yan⁴
¹Nanjing University of Science and Technology, CN; ²East China Normal University, CN; ³University of Notre Dame, US; ⁴Meituan.com Corporation, CN

1530 **Topology-aware Virtual Resource Management for Heterogeneous Multicore Systems**

Speaker: Jianmin Qian, Shanghai Jiaotong University, CN
 Authors: Jianmin Qian, Jian Li and Ruhui Ma, Shanghai Jiao Tong University, CN

IPs **IP1-6**

1600 Coffee Break in Exhibition Area

3.4 Optimizing Computing with Neuromorphic Architectures and Accelerators

Konf. 2 1430 - 1530

Chair: Dimitrios Soudris, NTUA, GR
Co-Chair: Ioana Vatajelu, University of Grenoble-Alpes, TIMA Laboratory, FR

Creating performance and power efficient acceleration techniques is a major challenge. In this session, various approaches are presented toward this direction for neural network applications and GPUs. A wide range of optimization techniques are discussed, including application-level optimizations, system-level solutions, matrix optimizations, and accuracy vs. computations trade-offs.

- 1430 **Structure Optimizations of Neuromorphic Computing Architectures for Deep Neural Networks**
 Speaker: Heechun Park, SNUCAD, KR
 Authors: Heechun Park and Taewhan Kim, Seoul National University, KR
- 1500 **CCR: A Concise Convolution Rule for Sparse Neural Network Accelerators**
 Speaker: Jiajun Li, Institute of Computing Technology, Chinese Academy of Sciences, CN
 Authors: Jiajun Li, Guihai Yan, Wenyan Lu, Shuhao Jiang, Shijun Gong, Jingya Wu and Xiaowei Li
 Institute of Computing Technology, Chinese Academy of Sciences, CN
- IPs **IP1-7**
- 1600 Coffee Break in Exhibition Area

3.5

Memory Reliability

Konf. 3 1430 - 1600

Chair: Jose Pineda, NXP, NL**Co-Chair:** Mehdi Tahoori, Karlsruhe Institute of Technology, DE

This session discusses reliability issues for different on-chip and off-chip memory technologies. The first paper uses important sampling to reduce the number of Monte Carlo simulations to obtain failure rates for advanced SRAM memories. The second paper performs degradation analysis for FinFET memories. The third paper discusses reliability issues for solid state memories.

- 1430 **Gradient Importance Sampling: an Efficient Statistical Extraction Methodology of High-Sigma SRAM Dynamic Characteristics**
 Speaker: Thomas Haine, Université catholique de Louvain, BE
 Authors: Thomas Haine¹, Johan Segers², Denis Flandre² and David Bol²
¹université catholique de louvain, BE; ²Université catholique de Louvain, BE
- 1500 **Degradation Analysis of High Performance 14nm FinFET SRAM**
 Speaker: Daniel Kraak, Delft University of Technology, NL
 Authors: Daniel Kraak¹, Innocent Agbo¹, Mottaqiallah Taouil¹, Said Hamdioui¹, Pieter Weckx², Stefan Cosemans² and Francky Catthoor²
¹Delft University of Technology, NL; ²imec vzw., BE
- 1530 **Investigating Power Outage Effects on Reliability of Solid-State Drives**
 Speaker: Hossein Asadi, Sharif University of Technology, IR
 Authors: Saba Ahmadian, Farhad Taheri, Mehrshad Lotfi, Maryam Karimi and Hossein Asadi, Sharif University of Technology, IR
- IPs **IP1-8**
- 1600 Coffee Break in Exhibition Area

3.6

Real-time Multiprocessing

Konf. 4 1430 - 1600

Chair: Jian-Jia Chen, TU Dortmund, DE**Co-Chair:** Rolf Ernst, TU Braunschweig, DE

The session details on various aspects of real-time multiprocessing, where special focus is put on workload-aware scheduling, network-on-chips, security and synchronization constraints. The first paper improves the overall schedulability by strategically arranging the workload among processors. The second paper reduces the pessimism in the analysis of NoC. The third paper considers security-related workloads whilst maintaining feasibility of schedules. The fourth paper presents an implemen-

tation of SDF graphs by means of OS-synchronization primitives.

1430 **Workload-Aware Harmonic Partitioned Scheduling for Probabilistic Real-Time Systems**

Speaker: Jiankang Ren, Dalian University of Technology, CN
 Authors: Jiankang Ren, Ran Bi, Xiaoyan Su, Qian Liu, Guowei Wu and Guozhen Tan, Dalian University of Technology, CN

1500 **Buffer-aware bounds to multi-point progressive blocking in priority-preemptive NoCs**

Speaker: Leandro Indrusiak, University of York, GB
 Authors: Leandro Indrusiak¹, Alan Burns¹ and Borislav Nikolic²
¹University of York, GB; ²CISTER/INESC-TEC, ISEP, IPP, PT

1530 **A Design-Space Exploration for Allocating Security Tasks in Multicore Real-Time Systems**

Speaker: Monowar Hasan, University of Illinois, BD
 Authors: Monowar Hasan¹, Sibin Mohan¹, Rodolfo Pellizzoni² and Rakesh Bobba³
¹University of Illinois at Urbana-Champaign, US; ²University of Waterloo, CA; ³Oregon State University, US

1545 **Design and Analysis of Semaphore Precedence Constraints: a Model-based Approach for Deterministic Communications**

Speaker: Yassine Ouhammou, LIAS / ENSMA & University of Poitiers, FR
 Authors: Thanh-Dat Nguyen¹, Yassine OUHAMMOU¹, Emmanuel GROLLEAU¹, Julien Forget², Claire Pagetti³ and Pascal RICHARD¹
¹LIAS/ENSMA, FR; ²LIFL/University of Lille1, FR; ³ONERA / DTIM, FR

IPs **IP1-9**

1600 Coffee Break in Exhibition Area

3.8 Innovative Products for Autonomous Driving (part 1)

Exhibition Theatre 1430 - 1600

Organiser: Hans-Jürgen Brand, IDT/ZMDI, DE

The workshop on Innovative Products for Autonomous Driving includes 2 sessions (part 2:session 6.8). This session will highlight how to design functional safety products, how 5G will enable connected cars and foundry solutions for manufacturing chips for autonomous driving.

1430 **Design of Functional Safety Products for Autonomous Driving**

Speaker: Christian Wolf, IDT Europe GmbH, DE

1500 **5G Connected Cars**

Speaker: Stanislav Mudriievskiy, Technical University Dresden, DE

1530 **Foundry Solutions for Autonomous Driving**

Speaker: Alexander Muffler, X-Fab Semiconductor Foundries AG, DE

1600 Coffee Break in Exhibition Area

1830 Exhibition Reception in Exhibition Area

IP1

Interactive Presentations

Conference Level, Foyer 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

- IP1-1 ReCom: An Efficient Resistive Accelerator for Compressed Deep Neural Networks**
 Speaker: Houxiang Ji, Shanghai Jiao Tong University, CN
 Authors: Houxiang Ji¹, Linghao Song², Li Jiang³, Hai (Helen) Li⁴ and Yiran Chen²
¹Shanghai Jiao Tong University, CN; ²Duke University, US; ³Department of Computer Science and Engineering, Shanghai Jiao Tong University, CN; ⁴Duke University/TUM-IAS, US
- IP1-2 SparseNN: An Energy-Efficient Neural Network Accelerator Exploiting Input and Output Sparsity**
 Speaker: Jingyang Zhu, Hong Kong University of Science and Technology, HK
 Authors: Jingyang Zhu, Jingbo Jiang, Xizi Chen and Chi-Ying Tsui, Hong Kong University of Science and Technology, HK
- IP1-3 ACCLIB: Accelerators as Libraries**
 Speaker: Jacob R. Stevens, Purdue University, US
 Authors: Jacob Stevens¹, Yue Du², Vivek Kozhikkottu³ and Anand Raghunathan¹
¹Purdue University, US; ²IBM, US; ³Intel Corporation, US
- IP1-4 HPXA: A Highly Parallel XML Parser**
 Speaker: Smruti Sarangi, IIT Delhi, IN
 Authors: Isaar Ahmad, Sanjog Patil and Smruti R. Sarangi, IIT Delhi, IN
- IP1-5 QoR-Aware Power Capping for Approximate Big Data Processing**
 Speaker: Sherief Reda, Brown University, US
 Authors: Seyed Morteza Nabavinejad¹, Xin Zhan², Reza Azimi², Maziar Goudarzi¹ and Sherief Reda²
¹Sharif University of Technology, IR; ²Brown University, US
- IP1-6 Exact Multi-Objective Design Space Exploration using ASPmT**
 Speaker: Kai Neubauer, University of Rostock, DE
 Authors: Kai Neubauer¹, Philipp Wanko², Torsten Schaub² and Christian Haubelt¹
¹University of Rostock, DE; ²University of Potsdam, DE
- IP1-7 HIPE: HMC Instruction Predication Extension Applied on Database Processing**
 Speaker: Diego Tomé, Centrum Wiskunde & Informatica (CWI), BR
 Authors: Diego Gomes Tomé¹, Paulo Cesar Santos², Luigi Carro², Eduardo Cunha de Almeida³ and Marco Antonio Zanata Alves³
¹Federal University of Paraná, BR; ²UFRGS - Universidade Federal do Rio Grande do Sul, BR; ³UFPR - Universidade Federal do Paraná, BRR
- IP1-8 Parametric Failure Modeling and Yield Analysis for STT-MRAM**
 Speaker: Sarath Mohanachandran Nair, Karlsruhe Institute of Technology, DE
 Authors: Sarath Mohanachandran Nair, Rajendra Bishnoi and Mehdi Tahoori, Karlsruhe Institute of Technology, DE
- IP1-9 One-Way Shared Memory**
 Speaker and Author: Martin Schoeberl, Technical University of Denmark, DK
- IP1-10 An Efficient Resource-Optimized Learning Prefetcher for Solid State Drives**
 Speaker: Rui Xu, University of Science and Technology of China, CN
 Authors: Rui Xu, Xi Jin, Linfeng Tao, Shuaizhi Guo, Zikun Xiang and Teng Tian,

Strongly-Coupled Quantum Matter Physics, Chinese Academy of Sciences, School of Physical Sciences, University of Science and Technology of China, Hefei, Anhui, China, CN

- IP1-11 **Bridging Discrete and Continuous Time Models with Atoms**
 Speaker: George Ungureanu, KTH Royal Institute of Technology, SE
 Authors: George Ungureanu¹, José E. G. de Medeiros² and Ingo Sander¹
¹KTH Royal Institute of Technology, SE; ²University of Brasília, BR
- IP1-12 **OHEX: OS-Aware Hybridization Techniques for Accelerating MPSoC Full-System Simulation**
 Speaker: Róbert Lajos Bücs, Institute for Communication Technologies and Embedded Systems, RWTH Aachen University, DE
 Authors: Róbert Lajos Bücs¹, Maximilian Fricke², Rainer Leupers¹, Gerd Ascheid¹, Stephan Tobies² and Andreas Hoffmann²
¹Institute for Communication Technologies and Embedded Systems, RWTH Aachen University, DE; ²Synopsys GmbH, DE
- IP1-13 **A Highly Efficient Full-System Virtual Prototype Based on Virtualization-Assisted Approach**
 Speaker: Hsin-I Wu, National Tsing Hua University, Department of Computer Science, Hsinchu, Taiwan, TW
 Authors: Hsin-I Wu, Chi-Kang Chen, Tsung-Ying Lu and Ren-Song Tsay, National Tsing Hua University, TW
- IP1-14 **Industrial Evaluation of Transition Fault Testing for Cost Effective Offline Adaptive Voltage Scaling**
 Speaker: Mahroo Zandrahimi, TU Delft, NL
 Authors: Mahroo Zandrahimi¹, Philippe Debaud², Armand Castillejo² and Zaid Al-Ars¹
¹Delft University of Technology, NL; ²STMicroelectronics, FR
- IP1-15 **An Analysis on Retention Error Behavior and Power Consumption of Recent DDR4 DRAMs**
 Speaker: Deepak M. Mathew, University of Kaiserslautern, DE
 Authors: Deepak M. Mathew¹, Martin Schultheis¹, Carl C. Rheinländer¹, Chirag Sudarshan¹, Matthias Jung², Christian Weis¹ and Norbert Wehn¹
¹University of Kaiserslautern, DE; ²Fraunhofer IESE, DE
- IP1-16 **A Boolean model for delay fault testing of emerging digital technologies based on ambipolar devices**
 Speaker: Davide Bertozzi, DE - University of Ferrara, IT
 Authors: Marcello Dalpasso¹, Davide Bertozzi² and Michele Favalli²
¹DEI - UNiv. of Padova, IT; ²DE - Univ. of Ferrara, IT
- IP1-17 **ATPG Power Guards: On Limiting the Test Power below Threshold**
 Speaker: Virendra Singh, Indian Institute of Technology Bombay, IN
 Authors: Rohini Gulve¹ and Virendra Singh²
¹Indian Institute of Technology Bombay, IN; ²IIT Bombay, IN
- 1830 Exhibition Reception in Exhibition Area

4.1

Executive Session: Exact Synthesis and SAT

Saal 2 1700 - 1830

Chair: Patrick Vuillod, Synopsys, FR
Co-Chair: Luca Amaru, Synopsys, US

Exact synthesis and SAT-based methods open new opportunities in design automation flows, where attaining the best possible logic implementation is key. This executive session covers recent advances on these two topics, which are tightly related, from both academic and industrial standpoints. The first paper shows how to find optimal circuit, on small number of variables, using SAT-solvers. The frontiers of circuits achievable by this method are discussed, together with known open problems. The second paper presents recent advancements on exact synthesis, with focus on implicit enumeration methods. Improvements on the

SAT-formulation are delineated, which enable complex constraints to be considered while solving exact synthesis. The third paper introduces a redundancy removal engine based on SAT. Its integration in a commercial EDA tool is described, detailing challenges and opportunities arising in an industrial synthesis environment.

- 1700 **Improving Circuit Size Upper Bounds Using SAT-Solvers**
Speaker and Author: Alexander Kulikov, Steklov Mathematical Institute at St. Petersburg, RU
- 1730 **Practical Exact Synthesis**
Speaker and Author: Winston Haaswijk, EPFL, CH
- 1800 **SAT-based Redundancy Removal**
Speaker and Author: Krishanu Debnath, Synopsys, IN
- 1830 Exhibition Reception in Exhibition Area

4.2

Domain Specific Design Methodologies

Konf. 6 1700 - 1830

Chair: Frédéric Pétrot, Grenoble Institute of Technology, FR
Co-Chair: Lars Bauer, Karlsruhe Institute of Technology, DE

In the quest for high efficiency, design methodologies specialize to particular domains. At first, a case study for approximate computing in the field of biometric security is presented. The second talk proposes a framework that uses a genetic algorithm to find an optimal mapping of artificial neural networks onto GPU + multi-core systems. Finally, a method is presented that controls by software the tolerance to disturbances provoked by neighboring readings of read-intensive applications in NAND flash.

- 1700 **Approximate Computing for Biometric Security Systems: A Case Study on Iris Scanning**
Speaker: Sherief Reda, Brown University, US
Authors: Soheil Hashemi, Hokchhay Tann, Francesco Buttafuoco and Sherief Reda, Brown University, US
- 1730 **Flash Read Disturb Management Using Adaptive Cell Bit-Density with In-Place Reprogramming**
Speaker: Sung-Ming Wu, National Chiao-Tung University, TW
Authors: Tai-Chou Wu, Yu-Ping Ma and Li-Pin Chang
National Chiao-Tung University, TW
- 1800 **HTF-MPR: A Heterogeneous TensorFlow Mapper Targeting Performance using Genetic Algorithms and Gradient Boosting Regressors**
Speaker: Nader Bagherzadeh, University of California, Irvine, US
Authors: Ahmad Albaqami, Maryam S. Hosseini and Nader Bagherzadeh
University of California, Irvine, US
- IPs **IP1-10**
- 1830 Exhibition Reception in Exhibition Area

4.3

System Modelling for Simulation and Optimisation

Konf. 1 1700 - 1830

Chair: Frederic Mallet, Universite Nice Cote d'Azur, FR
Co-Chair: Gianluca Palermo, Politecnico di Milano, IT

The session highlights the usefulness of modelling to improve the efficiency of system-level design and simulation. The first paper presents a framework to generate accurate representative workloads from big-data applications. The second paper minimises the energy consumption by reducing accesses to off-chip memory for convolutional neural networks (CNNs). The third paper introduces compile-time analysis to improve parallel SystemC simulation.

- 1700 **CAMP: Accurate Modeling of Core and Memory Locality for Proxy Generation of Big-data Applications**
Speaker: Andreas Gerstlauer, University of Texas at Austin, US
Authors: Reena Panda, Xinnian Zheng, Andreas Gerstlauer and Lizy John University of Texas at Austin, US
- 1730 **SmartShuttle: Optimizing Off-Chip Memory Accesses for Deep Learning Accelerators**
Speaker: Guihai Yan, Institute of Computing Technology, Chinese Academy of Sciences, CN
Authors: Jiajun Li, Guihai Yan, Wenyan Lu, Shuhao Jiang, Shijun Gong, Jingya Wu and Xiaowei Li
Institute of Computing Technology, Chinese Academy of Sciences, CN
- 1800 **Port Call Path Sensitive Conflict Analysis for Instance-Aware Parallel SystemC Simulation**
Speaker: Tim Schmidt, EECS, UC Irvine, US
Authors: Tim Schmidt, Zhongqi Cheng and Rainer Doemer EECS, UC Irvine, US
- IPs **IP1-11, IP1-12, IP1-13**
- 1830 Exhibition Reception in Exhibition Area

4.4

Overcoming the Limitations of Worst-Case IC Design

Konf. 2 1700 - 1830

Chair: Vasilis Pavlidis, University of Manchester, GB
Co-Chair: Giorgios Karakonstantis, Queen's University Belfast, GB

The session illustrates novel approaches to lower the high voltage and timing guard-bands affecting the performance of computing systems. The first talk introduces a methodology to increase the resiliency towards timing errors at ultra-low-voltages. Then, the placement of the timing monitor infrastructure is investigated in the second talk. The illustration of a mechanism to reliably tune the voltage supply concludes the session.

- 1700 **Trident: A Comprehensive Timing Error Resilient Technique against Choke Points at NTC**
Speaker: Aatreya Bal, Utah State University, US
Authors: Aatreya Bal, Sanghamitra Roy and Koushik Chakraborty, Utah State University, US
- 1730 **Bayesian Theory based Switching Probability Calculation Method of Critical Timing Path for On-Chip Timing Slack Monitoring**
Speaker: Byung Su Kim, Samsung Electronics, Foundry, KR
Authors: Byung Su Kim¹ and Joon-Sung Yang²
¹Samsung Electronics, KR; ²Sungkyunkwan University, KR

1800 **Performance Based Tuning of an Inductive Integrated Voltage Regulator Driving a Digital Core against Process and Passive Variations**

Speaker: Venkata Chaitanya Krishna Chekuri, Georgia Institute of Technology, US

Authors: Venkata Chaitanya Krishna Chekuri, Monodeep Kar, Arvind Singh and Saibal Mukhopadhyay, Georgia Institute of Technology, US

IPs **IP1-14, IP1-15**

1830 Exhibition Reception in Exhibition Area

4.5 **Test: innovative infrastructures and ATPG techniques**

Konf. 3 1700 - 1830

Chair: Danilo Pau, STMicroelectronics, IT

Co-Chair: Lukasz Rybak, Mentor Graphics Poland, PL

The session addresses hot challenges for 2.5D and 3D integration and asynchronous circuits, and introduces solutions for improving ATPG efficiency

1700 **Pre-Assembly Testing of Interconnects in Embedded Multi-Die Interconnect Bridge (EMIB) Dies**

Speaker: Krishnendu Chakrabarty, Duke University, US

Authors: Sudipta Mondal and Krishnendu Chakrabarty, Duke University, US

1730 **On the Reuse of Timing Resilient Architecture for Testing Path Delay Faults in Critical Paths**

Speaker: Luciano Ost, University of Leicester, UK

Authors: Felipe Kuentzer, Leonardo Juracy and Alexandre Amory, PUCRS University, BR

1745 **Characterization of Possibly Detected Faults by Accurately Computing their Detection Probability**

Speaker: Jan Burchard, Mentor, a Siemens Business, DE

Authors: Jan Burchard¹, Dominik Erb² and Bernd Becker¹

¹University of Freiburg, DE; ²Infinion Technologies, DE

IPs **IP1-16, IP1-17, IP2-1**

1830 Exhibition Reception in Exhibition Area

4.6 **Special Session: Securing Power-constrained System-on-Chips: Challenges and Opportunities**

Konf. 4 1700 - 1830

Chair: Mukhopadhyay Saibal, School of ECE, Georgia Institute of Technology, US

The power is the key constraint for modern System-on-Chip (SoC) design. After decade long research and development, the low-power circuit techniques and run-time power-management schemes are maturing at circuit, logic, and system levels. Now the SoCs face a new but critical design challenge: how to keep them secure - and techniques are being investigated in software and hardware to achieve this goal. This session is dedicated to study the critical, but often complex, interplay between power and security, in different aspects of design-for-security practices in SoCs.

- 1700 **Ultra-low Energy Circuit Building Blocks for Security Technologies**
Speaker: Sanu Mathew, Intel Corporation, US
Authors: Sanu Mathew¹, Sudhir Satpathy², Vikram Suresh² and Ram Krishnamurthy²
¹Intel Labs, US; ²Intel Corporation, Hillsboro, US
- 1715 **Embedded Randomness and Data Dependencies Design Paradigm: Advantages and Challenges**
Speaker: Itamar Levi, Université catholique de Louvain (UCL), Belgium, BE
Authors: Itamar Levi, Alexander Fish and Osnat Keren, Faculty of Engineering, Bar-Ilan University, IL
- 1740 **Exploiting On-chip Power Management for Side-Channel Security**
Speaker: Saibal Mukhopadhyay, Georgia Institute of Technology, US
Authors: Arvind Singh¹, Monodeep Kar¹, Sanu Mathew², Anand Rajan², Vivek De³ and Saibal Mukhopadhyay¹
¹Georgia Institute of Technology, US; ²Intel Labs, US; ³Intel Corporation, US
- 1805 **Energy-secure swarm power management**
Speaker: Pradip Bose, IBM Corporation, US
Authors: Augusto Vega, Alper Buyuktosunoglu and Pradip Bose
IBM T. J. Watson Research Center, US
- 1830 Exhibition Reception in Exhibition Area

4.7

Adaptive Reliable Computing Using Memristive and Reconfigurable Hardware

Konf. 5 1700 - 1830

Chair: Walter Weber, NAMLAB, DE**Co-Chair: Alessandro Cilardo**, University of Naples Federico II, IT

This session discusses reliability analysis and enhancement of memristive computing, addressing the non-linear behavior and the development of a logic synthesis flow for defect tolerance. The session also focuses on adapting the precision of the heterogeneous hardware to fit application requirements.

- 1700 **Rescuing Memristor-based Computing with Non-linear Resistance Levels**
Speaker: Jilan Lin, Tsinghua University, CN
Authors: Jilan Lin¹, Lixue Xia¹, Zhenhua Zhu¹, Hanbo Sun¹, Yi Cai¹, Hui Gao¹, Ming Cheng², Xiaoming Chen³, Yu Wang¹ and Huazhong Yang¹
¹Tsinghua University, CN; ²EE departement of Tsinghua University, CN; ³University of Notre Dame, US
- 1730 **PX-CGRA: Polymorphic Approximate Coarse-Grained Reconfigurable Architecture**
Speaker: Omid Akbari, University of Tehran, IR
Authors: Omid Akbari¹, Mehdi Kamal², Ali Afzali-Kusha², Massoud Pedram³ and Muhammad Shafique⁴
¹School of Electrical and Computer Engineering, University of Tehran,, IR; ²University of Tehran, IR; ³USC, US; ⁴Vienna University of Technology (TU Wien), AT
- 1800 **Multi-Precision Convolutional Neural Networks on Heterogeneous Hardware**
Speaker: Jose Nunez-Yanez, University of Bristol, GB
Authors: Moslem Amiri, Mohammad Hosseinabady, Simon McIntosh-Smith and Jose Nunez-Yanez, University of Bristol, GB
- 1815 **Logic Synthesis and Defect Tolerance for Memristive Crossbar Arrays**
Speaker: Onur Tunali, Istanbul Technical University, TR
Authors: Onur Tunali and Mustafa Altun, Istanbul Technical University, TR
- IPs **IP2-2, IP2-3, IP2-4**
- 1830 Exhibition Reception in Exhibition Area

4.8

Components for Secure IoT Systems

Exhibition Theatre 1700 - 1830

Organiser: Jürgen Haase, edacentrum, DE

In this Exhibition Workshop leading suppliers from the microelectronics industry present their newest technical solutions for designing and securing the IoT systems of the upcoming digital age. By elaborating on their technical approaches and the experience made during the design and in the field, they will provide attendees with valuable advice for the challenges in their own job.

- 1700 **Securing the Internet of Things with TI SimpleLink Platform**
Speaker: Roger Monk, Texas Instruments Europe, FR
- 1730 **Development of a near-threshold digital cell library and a design flow for IoT sensor systems**
Speaker: Jörg Doblaski, X-FAB, DE
- 1750 **Full Custom MEMS Design: new Methods for the Analysis of parasitic electrostatic effects**
Speaker: Axel Hald, Robert Bosch GmbH, DE
- 1810 **A Schmitt-Trigger Based Sub-Threshold Digital CMOS Circuit Design Technique for Ultra Low-Voltage and Ultra Low-Power Applications**
Speaker: Matthias Keller, University of Freiburg, DE
- 1830 Exhibition Reception in Exhibition Area

5.1

Special Day Session on Future and Emerging Technologies: Challenges for the Design of Microfluidic Devices: EDA for your Lab-on-a-Chip

Saal 2 0830 - 1000

Chair: Chakrabarty Krishnendu, Duke University, US

This session introduces experts from design automation to the field of microfluidic devices. Those devices, often also referred to as labs-on-chip, allow for conducting biological, chemical, and/or medical experiments with fluidics on a nano- or even picolitre scale automatically on miniaturized devices. By this, they revolutionized point-of-care diagnostics, chemo-fluidic logic, and more. The speakers in this session will introduce those areas and show how microfluidic devices help here. At the same time, they will cover how design automation can actually advance the further development of this emerging technology and how this can help to broaden the scope of applications for it.

0830 Point-of-care diagnostics 2.0: Standards, design automation, and consumer electronics for the next generation of diagnostic devices

Author: Emmanuel Delamarche, IBM Research, CH

0900 Design automation in microfluidics: An experimentalist's perspective

Author: William H. Grover, University of California, Riverside, US

0930 Chemofluidics: prospects and challenges

Author: Andreas Richter, Technische Universität Dresden, DE

1000 Coffee Break in Exhibition Area

5.2

Smart Energy and Automotive Systems

Konf. 6 0830 - 1000

Chair: Sebastian Steinhorst, Technical University of Munich, DE**Co-Chair:** Lulu Chan, NXP Semiconductors, NL

This session presents the latest advancements in battery and photovoltaic system management and optimization, as well as novel approaches towards efficient environmental mapping for autonomous driving and cloud-connected vehicles.

0830 SOH-Aware Active Cell Balancing Strategy For High Power Battery Packs

Speaker: Alma Proebstl, Technical University of Munich, DE

Authors: Sara Vinco, Lorenzo Bottaccioli, Edoardo Patti, Andrea Acquaviva, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT

¹Technical University of Munich, DE; ²TUM CREATE, SG

0900 GIS-Based Optimal Photovoltaic Panel Floorplanning for Residential Installations

Speaker: Massimo Poncino, Politecnico di Torino, IT

Authors: Sara Vinco, Lorenzo Bottaccioli, Edoardo Patti, Andrea Acquaviva, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT

0930 Cell-based Update Algorithm for Occupancy Grid Maps and Hybrid Map for ADAS on Embedded GPUs

Speaker: Jörg Fickenscher, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

Authors: Jörg Fickenscher¹, Jens Schlumberger¹, Frank Hannig¹, Mohamed Essayed Bouzouraa² and Jürgen Teich¹¹Friedrich-Alexander-Universität Erlangen-Nürnberg, DE; ²Concept Development Automated Driving, AUDI AG, DE

IPs IP2-5, IP2-6

1000 Coffee Break in Exhibition Area

5.3 **Heterogeneous multi-level caching**

Konf. 1 0830 - 1000

Chair: Jeronimo Castrillon, Technische Universität Dresden, DE**Co-Chair:** Lei Ju, Shandong University, CN

This session discusses different aspects and optimization for multi-level caching, involving various aspects of non-volatile memory technologies and embedded systems. The first paper proposes a novel management of last-level-cache for PCM-based main memory. The next paper presents a multi-level cache architecture with time-randomized behaviour, amenable for WCET analysis. The last paper explores the trade-off between retention time, performance, and energy for STT-RAM-based caches.

0830 **WALL: A Writeback-Aware LLC Management for PCM-based Main Memory Systems**

Speaker: Bahareh Pourshirazi, University of Illinois at Chicago, US

Authors: Bahareh Pourshirazi¹, Majed Valad Beigi², Zhichun Zhu¹ and Gokhan Memik²¹University of Illinois at Chicago, US; ²Northwestern University, US0900 **Design and Integration of Hierarchical-Placement Multi-level Caches for Real-Time Systems**

Speaker: Pedro Benedicte, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

Authors: Pedro Benedicte¹, Carles Hernandez², Jaume Abella³ and Francisco Cazorla⁴¹Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; ²Barcelona Supercomputing Center, ES; ³Barcelona Supercomputing Center (BSC-CNS), ES; ⁴Barcelona Supercomputing Center and IIIA-CSIC, ES0930 **LARS: Logically Adaptable Retention Time STT-RAM Cache for Embedded Systems**

Speaker: Tosiron Adegbija, University of Arizona, US

Authors: Kyle Kuan and Tosiron Adegbija, University of Arizona, US

IPs **IP2-7**

1000 Coffee Break in Exhibition Area

5.4 **Special Session: Lightweight Security for Resources-Constrained Internet-of-Things Applications**

Konf. 2 0830 - 1000

Chair: Halak Basel, Southampton University, GB**Co-Chair:** Jin Yier, University of Florida, US

This special sessions includes four papers: the first paper addresses the first question, it presents a lightweight cryptographic primitive based on physical unclonable functions, the second and third papers tackle the second and the third questions. They present two security protocols, for authentication and attestation respectively, which are specifically developed for resources-constrained IoT platforms. The fourth paper addresses the last challenge, it presents a solution which exploits existing on-chip hardware structure to detect abnormal and suspicious behaviours of an embedded system.

0830 **Cost Efficient Design of Modelling Attacks-Resistant Physical Unclonable Functions**

Speaker: Basel Halak, Southampton University, GB

Authors: Mohd Syafiq Mispan¹, Haibo Su¹, Mark Zwolinski² and Basel Halak³¹Electronics and Computer Science Department, Southampton University, GB; ²University of Southampton, GB; ³Southampton University, GB

- 0852 **Device Attestation: Past, Present, and Future**
 Speaker: Yier Jin, University of Florida, US
 Authors: Orlando Arias¹, Dean Sullivan¹, Fahim Rahman², Mark M. Teranipour² and Yier Jin²
¹University of Central Florida, US; ²University of Florida, US
- 0914 **A Reconfigurable Scan Network based IC Identification for Embedded Devices**
 Speaker: Omid Aramoon, University of Maryland, US
 Authors: Omid Aramoon¹, Xi Chen¹ and Gang Qu²
¹University of Maryland, US; ²Univ. of Maryland, College Park, US
- 0936 **Early Detection of System-Level Anomalous Behaviour using Hardware Performance Counters**
 Speaker: Mark Zwolinski, University of Southampton, GB
 Authors: Lai Leng Woo¹, Basel Halak² and Mark Zwolinski³
¹Electronics and Computer Science Department, Southampton University, GB; ²Southampton University, GB; ³University of Southampton, GB
- 1000 Coffee Break in Exhibition Area

5.5

Emerging Technologies for Future Computing

Konf. 3 0830 - 1000

Chair: Aida Todri-Sanial, CNRS, FR**Co-Chair: Mariagrazia Graziano**, Politecnico di Torino, IT

A wide overview of emerging technologies to enable novel computing paradigms. The session covers topics from carbon nanotube thin film transistors for flexible electronics, novel 3D interconnects using inductive coupling links, physical design of quantum cellular automata, and improving reliability of quantum logic cell implementation.

- 0830 **Compact Modeling of Carbon Nanotube Thin Film Transistors for Flexible Circuit Design**
 Speaker: Leilai Shao, University of California, Santa Barbara, US
 Authors: Leilai Shao¹, Tsung-Ching Huang², Ting Lei³, Zhenan Bao³, Raymond Beausoleil⁴ and Tim Cheng⁵
¹University of California Santa Barbara, US; ²Hewlett Packard Labs, US; ³Stanford University, US; ⁴HPE Labs, US; ⁵HKUST, HK
- 0900 **A High-Speed Design Methodology for Inductive Coupling Links in 3D-ICs**
 Speaker: Benjamin Fletcher, University of Southampton, GB
 Authors: Benjamin Fletcher¹, Shidhartha Das² and Terrence Mak¹
¹University of Southampton, GB; ²ARM Ltd., GB
- 0930 **An Exact Method for Design Exploration of Quantum-dot Cellular Automata**
 Speaker: Marcel Walter, University of Bremen, DE
 Authors: Marcel Walter¹, Robert Wille², Daniel Grosse³, Frank Sill Torres⁴ and Rolf Drechsler³
¹University of Bremen, DE; ²Johannes Kepler University Linz, AT; ³University of Bremen/DFKI GmbH, DE; ⁴Federal University of Minas Gerais, BR
- 0945 **Accurate Margin Calculation for Single Flux Quantum Logic Cells**
 Speaker: Massoud Pedram, University of Southern California, US
 Authors: Soheil Nazar Shahsavani, Bo Zhang and Massoud Pedram
 University of Southern California, US
- IPs **IP2-8, IP2-9, IP2-10**
- 1000 Coffee Break in Exhibition Area

5.6

Reliability improvement and evaluation techniques

Konf. 4 0830 - 1000

Chair: Stefano Di Carlo, Politecnico di Torino, IT**Co-Chair:** Vasileios Tenentes, University of Southampton, GB

This session introduces reliability improvement approaches using dynamic recovery, redundant multithreading, aging mitigation and optimization of metastability effects, spanning from the system to the circuit layer. Also, cross-layer resilience evaluation via fault injection for complex microprocessors is presented.

0830

Improving Reliability for Real-Time Systems through Dynamic Recovery

Speaker: Yue Ma, University of Notre Dame, US

Authors: Yue Ma¹, Tam Chantem², Robert P. Dick³ and X, Sharon Hu¹¹University of Notre Dame, US; ²Virginia Tech, US; ³University of Michigan, US

0900

Optimal Metastability-Containing Sorting Networks

Speaker: Johannes Bund, Saarland University, DE

Authors: Johannes Bund¹, Christoph Lenzen² and Moti Medina³¹Saarland University, Saarland Informatics Campus, DE; ²Max Planck Institute for Informatics, Saarland Informatics Campus, DE; ³From 1/10/2017 in The Department of Electrical and Computer Engineering Ben-Gurion University, IL

0930

MAUI: Making Aging Useful, Intentionally

Speaker: Shou-Chun Li, Department of Computer Science, National Chiao Tung University, TW

Authors: Kai-Chiang Wu¹, Tien-Hung Tseng² and Shou-Chun Li¹¹National Chiao Tung University, TW; ²National Chiao Tung University, Taiwan, TW

0945

EXPERT: Effective and Flexible Error Protection by Redundant Multithreading

Speaker: HwiSoo So, Yonsei University, US

Authors: HwiSoo So¹, Moslem Didehban², Yohan Ko¹, Aviral Shrivastava² and Kyoungwoo Lee¹¹Yonsei University, KR; ²Arizona State University, US

IPs

IP2-11, IP2-12

1000

Coffee Break in Exhibition Area

5.7

Software-centric techniques for embedded systems

Konf. 5 0830 - 1000

Chair: Marc Geilen, Eindhoven University of Technology, NL**Co-Chair:** Daniel Ziener, Science University of Twente Zilverling, NL

Modern heterogeneous architectures pose new challenges for energy-efficient embedded realizations. The talks in this session address these challenges using software techniques, such as approximate computing, task scheduling, and memory and power-management.

0830

HePREM: Enabling Predictable GPU Execution on Heterogeneous SoC

Speaker: Björn Forsberg, ETH Zürich, CH

Authors: Björn Forsberg¹, Luca Benini² and Andrea Marongiu³¹ETH Zürich, CH; ²Università di Bologna, IT; ³ETH Zurich, CH

0900

Circuit Carving: A Methodology for the Design of Approximate Hardware

Speaker: Ilaria Scarabottolo, USI Lugano, CH

Authors: Ilaria Scarabottolo, Giovanni Ansaloni and Laura Pozzi, USI Lugano, CH

- 0915 **ICNN: An Iterative Implementation of Convolutional Neural Networks to Enable Energy and Computational Complexity Aware Dynamic Approximation**
Speaker: Avesta Sasan, George Mason University, US
Authors: Katayoun Neshatpour, Farnaz Behnia, Houman Homayoun and Avesta Sasan
George Mason University, US
- 0930 **Task Scheduling for Many-Cores with S-NUCA Caches**
Speaker: Anuj Pathania, Karlsruhe Institute of Technology, IN
Authors: Anuj Pathania and Joerg Henkel, Karlsruhe Institute of Technology, DE
- 0945 **KVSSD: Close Integration of LSM Trees and Flash Translation Layer for Write-Efficient KV Store**
Speaker: Sung-Ming Wu, National Chiao-Tung University, TW
Authors: Sung-Ming Wu, Kai-Hsiang Lin and Li-Pin Chang
National Chiao-Tung University, TW
- IPs **IP2-13, IP2-14**
- 1000 Coffee Break in Exhibition Area

IP2 Interactive Presentations

Conference Level, Foyer 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

- IP2-1 **In-growth Test for Monolithic 3D Integrated SRAM**
Speaker: Yixun Zhang, Shanghai Jiao Tong University, CN
Authors: Pu Pang¹, Yixun Zhang¹, Tianjian Li¹, Sung Kyu Lim², Quan Chen¹, Xiaoyao Liang¹ and Li Jiang³
¹Shanghai Jiao Tong University, CN; ²Georgia Tech, US; ³Department of Computer Science and Engineering, Shanghai Jiao Tong University, CN
- IP2-2 **A Co-design Methodology for Scalable Quantum Processors and their Classical Electronic Interface**
Speaker: Jeroen van Dijk, Delft University of Technology, NL
Authors: Jeroen van Dijk¹, Andrei Vladimirescu², Masoud Babaie¹, Edoardo Charbon¹ and Fabio Sebastiano¹
¹Delft University of Technology, NL; ²University of California, Berkeley, US
- IP2-3 **Approximate Quaternary Addition with the Fast Carry Chains of FPGAs**
Speaker: Philip Brisk, University of California, Riverside, US
Authors: Sina Boroumand¹, Hadi P. Afshar² and Philip Brisk³
¹University of Tehran, IR; ²Qualcomm Research, US; ³University of California, Riverside, US
- IP2-4 **NN Compactor: Minimizing Memory and Logic Resources for Small Neural Networks**
Speaker: Seongmin Hong, Hongik University, KR
Authors: Seongmin Hong¹, Inho Lee² and Yongjun Park²
¹Hongik University, KR; ²Hanyang University, KR
- IP2-5 **Improving Fast Charging Efficiency of Reconfigurable Battery Packs**
Speaker: Alexander Lamprecht, TUM CREATE, SG
Authors: Alexander Lamprecht¹, Swaminathan Narayanaswamy¹ and Sebastian Steinhorst²
¹TUM CREATE, SG; ²Technical University of Munich, DE
- IP2-6 **Cloud-assisted Control of Ground Vehicles using Adaptive Computation Offloading Techniques**
Speaker: Soheil Samii, General Motors R&D, Warren, US
Authors: Arun Adiththan¹, Ramesh S² and Soheil Samii³
¹City University of New York, US; ²General Motors R&D, US; ³General Motors Research & Development, US

- IP2-7 FusionCache: using LLC Tags for DRAM Cache**
 Speaker: Evangelos Vasilakis, Chalmers University of Technology, SE
 Authors: Evangelos Vasilakis¹, Vassilis Papaefstathiou², Pedro Trancoso¹ and Ioannis Sourdis¹
¹Chalmers University of Technology, SE; ²FORTH-ICS, GR
- IP2-8 Improved Synthesis of Clifford+T Quantum Functionality**
 Speaker: Philipp Niemann, German Research Center for Artificial Intelligence (DFKI GmbH), DE
 Authors: Philipp Niemann¹, Robert Wille² and Rolf Drechsler³
¹Cyber-Physical Systems, DFKI GmbH, DE; ²Johannes Kepler University Linz, AT; ³University of Bremen/DFKI GmbH, DE
- IP2-9 Energy-Efficient Channel Alignment of DWDM Silicon Photonic Transceivers**
 Speaker: Yuyang Wang, University of California, Santa Barbara, US
 Authors: Yuyang Wang¹, M. Ashkan Seyedi², Rui Wu¹, Jared Hulme², Marco Fiorentino², Raymond G. Beausoleil² and Kwang-Ting Cheng³
¹University of California, Santa Barbara, US; ²Hewlett Packard Labs, US; ³Hong Kong University of Science and Technology, HK
- IP2-10 A Physical Synthesis Flow for Early Technology Evaluation of Silicon Nanowire based Reconfigurable FETs**
 Speaker: Shubham Rai, Chair For Processor Design, CFAED, Technische Universität Dresden, Dresden, DE
 Authors: Shubham Rai¹, Ansh Rupani², Dennis Walter¹, Michael Raitza³, André Heinzig⁴, Christian Mayr¹, Walter Weber⁵ and Akash Kumar⁶
¹Technische Universität Dresden, Dresden, DE; ²Birla Institute of Technology and Science Pilani, Hyderabad Campus, IN; ³Technische Universität Dresden and CfaED, DE; ⁴NaMLab GmbH, DE; ⁵NaMLab gGmbH and CfaED, DE; ⁶Technische Universität Dresden, DE
- IP2-11 ETISS-ML: A Multi-Level Instruction Set Simulator with RTL-level Fault Injection Support for the Evaluation of Cross-Layer Resiliency Techniques**
 Speaker: Martin Dittrich, Technical University of Munich, DE
 Authors: Daniel Mueller-Grietschneider¹, Martin Dittrich¹, Josef Weinzierl¹, Eric Cheng², Subhasish Mitra² and Ulf Schlichtmann¹
¹Technical University of Munich, DE; ²Stanford University, US
- IP2-12 Precise Evaluation of the Fault Sensitivity of OOO Superscalar Processors**
 Speaker: Antonio Carlos Schneider Beck, Federal University of Rio Grande do Sul, BR
 Authors: Rafael Tonetto¹, Gabriel Luca Nazar² and Antonio Carlos Schneider Beck²
¹Federal University of Rio Grande do Sul, BR; ²Universidade Federal do Rio Grande do Sul, BR
- IP2-13 StreamFTL: Stream-level Address Translation Scheme for Memory Constrained Flash Storage**
 Speaker: Dongkun Shin, Sungkyunkwan University, KR
 Authors: Hyukjoong Kim, Kyuhwa Han and Dongkun Shin, Sungkyunkwan University, KR
- IP2-14 Online Concurrent Workload Classification for Multi-core Energy Management**
 Speaker: Karunakar Reddy Basireddy, University of Southampton, GB
 Authors: Karunakar Reddy Basireddy¹, Amit Kumar Singh², Geoff V. Merrett¹ and Bashir M. Al-Hashimi¹
¹University of Southampton, GB; ²University of Essex, GB
- IP2-15 AIM: Fast and Energy-Efficient AES In-Memory Implementation for Emerging Non-volatile Main Memory**
 Speaker: Jingtong Hu, University of Pittsburgh, US
 Authors: Mimi Xie¹, Shuangchen Li², Alvin Glova², Jingtong Hu¹, Yuan-gang Wang³ and Yuan Xie²
¹University of Pittsburgh, US; ²University of California, Santa Barbara, US; ³Huawei Technologies, China, CN

- IP2-16 **SAT-based Bit-flipping Attack on Logic Encryptions**
 Speaker: Hai Zhou, Northwestern University, US
 Authors: Yuanqi Shen, Amin Rezaei and Hai Zhou, Northwestern University, US
- IP2-17 **AMS Verification Methodology regarding Supply Modulation in RF SoCs induced by Digital Standard Cells**
 Speaker: Fabian Speicher, RWTH Aachen University, DE
 Authors: Fabian Speicher, Jonas Meier, Soheil Aghaie, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, DE

6.1

Special Day Session on Future and Emerging Technologies: Transistors for Digital NanoSystems: The Road Ahead

Saal 2 1100 - 1230

Chair: Aitken Rob, ARM, US

This session presents energy-efficient digital design approaches using new transistor ideas and their experimental demonstrations. Examples include negative capacitance-based gate control, carbon nanotube-based channels, and polarity-control by design.

- 1100 **Negative Capacitance Transistors**
 Author: Sayeef Salahuddin, UC Berkeley, US
- 1130 **Carbon nanotube film-based CMOS and optoelectronic devices and integrated systems**
 Author: Lian-Mao Peng, Peking University, CN
- 1200 **Towards High-Performance Polarity-Controllable FETs with 2D Materials**
 Speaker: Pierre-Emmanuel Gaillardon, University of Utah, US
 Authors: Giovanni V. Resta¹, Jorge Romero Gonzalez², Yashwanth Balaji³, Tarun Kumar Agarwal³, Dennis Lin³, Francky Catthoor³, Iuliana P. Radu³, Giovanni De Micheli⁴ and Pierre-Emmanuel Gaillardon⁵
¹Integrated System Laboratory (LSI), School of Engineering, École Polytechnique Fédérale de Lausanne (EPFL), CH; ²Laboratory of NanoIntegrated Systems (LNIS), Department of Electrical and Computer Engineering, University of Utah, US; ³IMEC, BE; ⁴École Polytechnique Fédérale de Lausanne (EPFL), CH; ⁵University of Utah, US
- 1230 Lunch Break in Großer Saal and Saal 1

6.2

Memory Security

Konf. 6 1100 - 1230

Chair: Francesco Regazzoni, ALaRI USI, CH

Co-Chair: Todd Austin, University of Michigan, US

Papers in this session address the problem of dealing with secure memory architectures and cover the whole memory hierarchy from cache to storage. Different levels of the hierarchy need different protection mechanisms, such as: protecting information from attacks on untrusted clouds and ensuring integrity of the main memory used by the CPU. Finally, the last paper identifies cache attacks and vulnerabilities on MP-SoCs using Networks on Chips.

- 1100 **Dynamic Skewed Tree for Fast Memory Integrity Verification**
 Speaker: Saru Vig, Nanyang Technological University, SG
 Authors: Saru Vig, Jiang Guiyuan and Lam Siew Kei, Nanyang Technological University, SG

- 1130 **Earthquake - A NoC-based Optimized Differential Cache-Collision Attack for MPSoCs**
 Speaker: Cezar Rodolfo W. Reinbrecht, UFRGS, BR
 Authors: Cezar Rodolfo Wedig Reinbrecht¹, Bruno Endres Forlin¹, Andreas Zankl² and Johanna Sepulveda³
¹UFRGS, BR; ²Fraunhofer Institute for Applied and Integrated Security, DE; ³Technical University of Munich, DE
- 1200 **A Fast and Resource Efficient FPGA Implementation of Secret Sharing for Storage Applications**
 Speaker: Jakob Stangl, Austrian Institute of Technology (AIT), AT
 Authors: Jakob Stangl¹, Thomas Lorünser¹ and Sai Dinakar²
¹Austrian Institute of Technology (AIT), AT; ²TU Wien, AT
- IPs **IP2-15, IP2-16**
- 1230 Lunch Break in Großer Saal and Saal 1

6.3

Advances in AMS/RF Design & Test Automation and Beyond

Konf. 1 1100 - 1230

Chair: Marie-Minerve Louerat, LIP6, FR

This session brings together new design and test automation developments for AMS/RF systems and beyond. Papers in the session cover a wide range of exciting topics from circuit optimization to design tools and verification. The topics include innovative combination of principal component analysis and evolutionary computation applied to analog/RF IC optimization; hybrid automation approach for SAR ADC design aimed at IoT applications; and design space exploration for wireless systems. Interactive papers discuss AMS circuit testbenches, modeling and simulation of systems that combine continuous and discrete time components, and AMS verification.

- 1100 **Enhanced Analog and RF IC Sizing Methodology using PCA and NSGA-II Optimization Kernel**
 Speaker: Nuno Lourenco, Instituto de Telecomunicações, PT
 Authors: Tiago Pessoa¹, Nuno Lourenco², Ricardo Martins², Ricardo Povoas² and Nuno Horta²
¹Instituto Superior Técnico – TU Lisbon, PT; ²Instituto de Telecomunicações, Instituto Superior Técnico – TU Lisbon, PT
- 1130 **A SystemC-based Simulator for Design Space Exploration of Smart Wireless Systems**
 Speaker: Gabriele Miorandi, University of Verona, IT
 Authors: Gabriele Miorandi¹, Francesco Stefanni², Federico Fraccaroli³ and Davide Quaglia¹
¹University of Verona, IT; ²EDALab s.r.l., IT; ³Wagoo Italia s.r.l.s., IT
- 1200 **A Circuit-Design-Driven Tool with a Hybrid Automation Approach for SAR ADCs in IoT**
 Speaker: Ming Ding, IMEC/Holst Centre, NL
 Authors: Ming Ding¹, Guibin Chen², Pieter Harpe³, Benjamin Busze¹, Yao-Hong Liu¹, Christian Bachmann¹, Kathleen Philips¹ and Arthur van Roermund³
¹imec-Holst Centre, NL; ²imec-Holst Centre, Eindhoven University of Technology, NL; ³Eindhoven University of Technology, NL
- IPs **IP2-17, IP3-1, IP3-2**
- 1230 Lunch Break in Großer Saal and Saal 1

Modeling, Control and Scheduling for Cyber-Physical Systems

Konf. 2 1100 - 1230

Chair: Shiyun Hu, Michigan Tech., US**Co-Chair:** Franco Fummi, University of Verona, IT

The fast advancement of cyber-physical systems has been presenting significant design challenges. The papers in this session address these CPS design challenges across layers of control, communication, computation and embedded microarchitecture. They include methodologies for modeling and integrating heterogeneous models to build CPS virtual platforms, routing and scheduling messages with control stability consideration for networked CPS, designing feedback control of EtherCAT networks for reliability enhancement, and scheduling tasks with consideration of cache to maximize control performance.

1100 Automatic Integration of Cycle-accurate Descriptions with Continuous-time Models for Cyber-Physical Virtual Platforms

Speaker: Franco Fummi, University of Verona, IT

Authors: Michele Lora¹, Stefano Centomo¹, Davide Quaglia¹ and Franco Fummi²¹University of Verona, IT; ²Universita' di Verona, IT
1130 Stability-Aware Integrated Routing and Scheduling for Control Applications in Ethernet Networks

Speaker: Rouhollah Mahfouzi, Linköping University, SE

Authors: Rouhollah Mahfouzi¹, Amir Aminifar², Soheil Samii³, Ahmed Rezine¹, Petru Eles¹ and Zebo Peng¹¹Linköping University, SE; ²Swiss Federal Institute of Technology in Lausanne (EPFL), CH; ³General Motors Research & Development, US
1200 Feedback Control of Real-Time EtherCAT Networks for Reliability Enhancement in CPS

Speaker: Tongquan Wei, East China Normal University, CN

Authors: Liying Li¹, Peijin Cong¹, Kun Cao¹, Junlong Zhou², Tongquan Wei¹, Mingsong Chen¹ and X, Sharon Hu³¹East China Normal University, CN; ²Nanjing University of Science and Technology, CN; ³University of Notre Dame, US
1215 Cache-Aware Task Scheduling for Maximizing Control Performance

Speaker: Wanli Chang, Singapore Institute of Technology, SG

Authors: Wanli Chang¹, Debayan Roy², X, Sharon Hu³ and Samarjit Chakraborty²¹Singapore Institute of Technology, SG; ²Technical University of Munich, DE; ³University of Notre Dame, US
IPs IP3-3, IP3-4, IP3-5

1230 Lunch Break in Großer Saal and Saal 1

Special Session: Three Years of Low-Power Image Recognition Challenge

Konf. 3 1100 - 1230

Chair: Yung-Hsiang Lu, Purdue University, US

Reducing power consumption has been one of the most important goals since the creation of electronic systems. Energy efficiency is increasingly important as battery-powered systems equipped with cameras (such as drones and body cameras) are widely used. It is desirable using the on-board computers to recognize objects in the images captured by these cameras. The Low-Power Image Recognition Challenge (LPIRC) is an annual competition started in 2015. LPIRC considers both energy consumption and the accuracy in detecting and locating objects in images. The special session includes presentations given by the winners of the first three years of LPIRC explaining their winning solutions.

- 1100 **Three Years of Low-Power Image Recognition Challenge: Introduction to Special Session**
 Speaker: Yung-Hsiang Lu, Purdue University, US
 Authors: Kent Gauen¹, Ryan Dailey¹, Yung-Hsiang Lu¹, Eunbyung Park², Wei Liu², Alexander Berg² and Yiran Chen³
¹Purdue University, US; ²University of North Carolina at Chapel Hill, US; ³Duke University, US
- 1115 **Real-time object detection towards high power efficiency**
 Speaker: Jincheng Yu, Tsinghua University, CN
 Authors: Jincheng Yu¹, Kaiyuan Guo¹, Yiming Hu¹, Xuefei Ning¹, Jiantao Qiu¹, Huizi Mao¹, Song Yao², Tianqi Tang¹, Boxun Li¹, Yu Wang¹ and Huazhong Yang¹
¹Tsinghua University, CN; ²DeePhi Technology, Beijing, CN
- 1140 **A Retrospective Evaluation of Energy-Efficient Object Detection Solutions on embedded devices**
 Speaker: Ying Wang, Chinese Academy of Sciences, CN
 Authors: Ying Wang¹, Zhenyu Quan¹, Yinhe Han², Jiajun Li¹, Huawei Li² and Xiaowei Li¹
¹State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, CN;
²Institute of Computing Technology, Chinese Academy of Sciences, CN
- 1205 **Joint Optimization of Speed, Accuracy, and Energy for Embedded Image Recognition Systems**
 Speaker: Soonhoi Ha, Seoul National University, KR
 Authors: Duseok Kang, Jintaek Kang, Donghyun Kang, Sungjoo Yoo and Soonhoi Ha, Seoul National University, KR
- 1230 Lunch Break in Großer Saal and Saal 1

6.8

Innovative Products for Autonomous Driving (part 2)

Exhibition Theatre 1100 - 1230

Organiser: Hans-Jürgen Brand, IDT/ZMDI, DE

The workshop on Innovative Products for Autonomous Driving includes 2 sessions (part 1:session 3.8). This session will highlight how to do ultra-low-voltage design, how to accelerate physical signoff and a 22 nm FDSOI System-on-Chip development for Advanced Driver Assistance System.

- 1100 **22FDX Ultra-Low-Voltage Design based on Adaptive Body Bias**
 Speaker: Holger Eisenreich, Racyics GmbH, DE
- 1130 **A new ADAS Chip Design in 22 nm FDSOI Technology for Automotive Computer Vision Applications**
 Speaker: Jens Benndorf, Dream Chip Technologies, DE
- 1200 **Accelerating Physical Signoff for Leading edge chip designs**
 Speaker: David DeMarcos, Synopsys, DE
- 1230 Lunch Break in Großer Saal and Saal 1

7.0

LUNCH TIME KEYNOTE SESSION: From Inverse Design to Implementation of Robust and Efficient Photonics for Computing

Saal 2 1350 - 1420

Chair: Ayse Coskun, Boston University, US

It is estimated that nearly 10% of the world electricity is consumed in information processing and computing, including data centers [D.A.B. Miller, Journal of Lightwave Technology, 2017]. It is clear that the exponential growth in use of these technologies is not sustainable unless dramatic changes are made to computing hardware, in order to increase its speed and energy efficiency. Optical interconnects are considered a solution to these obstacles, with potential to reduce energy consumption in on-chip optical interconnects to atto-Joule per bit (aJ/bit), while increasing operating speed beyond 20GHz. However, the state of the art photonics is bulky, inefficient, sensitive to environment, lossy, and its performance is severely degraded in real-world environment as opposed to ideal laboratory conditions, which has prevented from using it in many practical applications, including interconnects. Therefore, it is clear that new approaches for implementing photonics are crucial. We have recently developed a computational approach to inverse-design photonics based on desired performance, with fabrication constraints and structure robustness incorporated in design process. Our approach performs physics guided search through the full parameter space until the optimal solution is reached. Resulting device designs are non-intuitive, but are fabricable using standard techniques, resistant to temperature variations of hundreds of degrees, typical fabrication errors, and they outperform state of the art counterparts by many orders of magnitude in footprint, efficiency and stability. This is completely different from conventional approach to design photonics, which is almost always performed by brute-force or intuition-guided tuning of a few parameters of known structures, until satisfactory performance is achieved, and which almost always leads to sub-optimal designs. Apart from integrated photonics, our approach is also applicable to any other optical and quantum optical devices and systems.

1345 **Presentation of the IEEE TCCPS Technical Achievement Award to Prof. Alberto Sangiovanni-Vincentelli**

Shiyun Hu, Chair of TCCPS, US

1350 **From inverse design to implementation of robust and efficient photonics for computing**

Author and Speaker: Jelena Vuckovic, Stanford University, US

7.1

Special Day Session on Future and Emerging Technologies: Theoretical and practical aspects of verification of quantum computers

Saal 2 1430 - 1600

Chair: Naveh Yehuda, IBM Research, IL

Quantum computing is emerging at a meteoric pace from a pure academic field to a fully industrial framework. Rapid advances are happening both in the physical realizations of quantum chips, and in their potential software applications. In contrast, we are not seeing that rapid growth in the design and verification methodologies for scaled-up quantum machines. In this session we describe the field of verification of quantum computers. We discuss the underlying concepts of this field, its theoretical and practical challenges, and state-of-the-art approaches to addressing those challenges. The goal of this session is to help facilitate early efforts to adapt and create verification methodologies for quantum computers and systems. Without such early efforts, a debilitating gap may form between the state-of-the-art of low level physical technologies for quantum computers, and our ability to build medium, large, and very large scale integrated quantum circuits (M/L/VLSIQ).

- 1430 **Verification of quantum computing**
Author: Petros Wallden, School of Informatics, University of Edinburgh, UK
- 1450 **Gaining insight into near-term quantum devices with tailor-made applications**
Author: James R. Wootton, University of Basel, CH
- 1515 **The engineering challenges in quantum computing**
Author: Koen Bertels, Delft University of Technology, NL
- 1540 **Quantum verification: What can we adopt and learn from classical verification**
Author: Yehuda Naveh, IBM Research - Haifa, IL
- 1600 Coffee Break in Exhibition Area

7.2

Run-time power estimation and optimization

Konf. 6 1430 - 1600

Chair: Pascal Vivet, CEA-Leti, FR

In this session, the first paper presents energy efficiency optimization for CPU-GPU heterogeneous architectures using machine-learning. The next two papers present run-time power modeling and estimation methods for embedded systems. Finally, the last paper presents an on-line reconfiguration method for photovoltaic power system.

- 1430 **Airavat: Improving Energy Efficiency of Heterogeneous Applications**
Speaker: Trinayan Baruah, Northeastern University, US
Authors: Trinayan Baruah¹, Yifan Sun¹, Shi Dong¹, David Kaeli² and Norm Rubin²
¹Northeastern University, Boston, US; ²NVIDIA, US
- 1500 **All-Digital Embedded Meters for On-line Power Estimation**
Speaker: Daniele Jahier Pagliari, Politecnico di Torino, IT
Authors: Daniele Jahier Pagliari, Valentino Peluso, Yukai Chen, Andrea Calimera, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT
- 1530 **PowerProbe: Run-time Power Modeling Through Automatic RTL Instrumentation**
Speaker: Davide Zoni, Politecnico di Milano, IT
Authors: Davide Zoni, Luca Cremona and William Fornaciari, Politecnico di Milano, IT
- 1545 **Design Optimization of Photovoltaic Array on a Curved Surface**
Speaker: Sangyoung Park, Technical University of Munich, DE
Authors: Sangyoung Park and Samarjit Chakraborty, Technical University of Munich, DE
- IPs **IP3-6, IP3-7, IP3-8**
- 1600 Coffee Break in Exhibition Area

7.3

Advances in Logic Synthesis and Technology Mapping

Konf. 1 1430 - 1600

Chair: Luciano Lavagno, Politecnico di Torino, IT**Co-Chair:** Mathias Soeken, EPFL, CH

This session presents recent progress in logic synthesis and technology mapping. The first paper discusses improvements to Boolean resynthesis using a theory on Boolean filtering and a more general notion of permissible functions. The second paper applies methods based on Boolean relations for the optimization of combinational logic networks. The third paper proposes a technology mapping approach for silicon nanowire reconfigurable FETs. The fourth paper presents for the first time an approximate synthesis methods for threshold logic circuits through an iterative approach that guarantees an error bound.

1430

Improvements to Boolean Resynthesis

Speaker: Mathias Soeken, EPFL, CH

Authors: Luca Amaru¹, Mathias Soeken², Patrick Vuillod³, Jiong Luo¹, Alan Mishchenko⁴, Janet Olson¹, Robert Brayton⁴ and Giovanni De Micheli²¹Synopsys Inc., US; ²EPFL, CH; ³Synopsys Inc., FR; ⁴UC Berkeley, US;

1500

Logic Optimization with Considering Boolean Relations

Speaker: Chia-Cheng Wu, National Tsing Hua University, TW

Authors: Tung-Yuan Lee¹, Chia-Cheng Wu¹, Chia-Chun Lin¹, Yung-Chih Chen² and Chun-Yao Wang³¹National Tsing Hua University, TW; ²Yuan Ze University, TW; ³Dept. CS, National Tsing Hua University, TW

1530

Technology Mapping Flow for Emerging Reconfigurable Silicon Nanowire Transistors

Speaker: Shubham Rai, Chair For Processor Design, CFAED, Technische Universität Dresden, Dresden, DE

Authors: Shubham Rai¹, Michael Raitza² and Akash Kumar¹¹Technische Universität Dresden, DE; ²Technische Universität Dresden and CFAED, DE

1545

Efficient Synthesis of Approximate Threshold Logic Circuits with an Error Rate Guarantee

Speaker: Chia-Chun Lin, National Tsing Hua University, TW

Authors: Yung-An Lai¹, Chia-Chun Lin¹, Chia-Cheng Wu¹, Yung-Chih Chen² and Chun-Yao Wang³¹National Tsing Hua University, TW; ²Yuan Ze University, TW; ³Dept. CS, National Tsing Hua University, TW

IPs

IP3-9, IP3-10

1600

Coffee Break in Exhibition Area

7.4

DRAM and NVMs

Konf. 2 1430 - 1600

Chair: Francisco Cazorla, BSC, ES**Co-Chair:** Olivier Sentieys, IRISA, FR

Memory is one of the major bottlenecks for performance and power. The first paper addresses this inefficiency by proposing a unified LLC+DRAM memory controller to harvest row buffer hits and to increase memory bandwidth. The next paper adopts approximate computing to increase the performance of STT and to reduce the number of writes to PCM. Finally, the third paper proposes an adaptive write current scaling approach that adjusts the write current at runtime while considering the write rates of the running application.

1430 **Row-Buffer Hit Harvesting in Orchestrated Last-Level Cache and DRAM Scheduling for Heterogeneous Multicore Systems**

Authors: Yang Song¹, Olivier Alavoine² and Bill Lin¹
¹University of California, San Diego, US; ²Qualcomm Inc., US

1500 **AdAM: Adaptive Approximation Management for the Non-Volatile Memory Hierarchies**

Speaker: Muhammad Abdullah Hanif, Vienna University of Technology, AT
 Authors: Mohammad Taghi Teimoori¹, Muhammad Abdullah Hanif², Alireza Ejlali¹ and Muhammad Shafique²
¹Sharif University of Technology, IR; ²Institute of Computer Engineering, Vienna University of Technology, AT

1530 **A Cross-layer Adaptive Approach for Performance and Power Optimization in STT-MRAM**

Speaker: Nour Sayed, KIT - Karlsruhe Institute of Technology, DE
 Authors: Nour Sayed, Rajendra Bishnoi, Fabian Oboril and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

IPs **IP3-11**

1600 Coffee Break in Exhibition Area

7.5

Reliability Modeling and Mitigation

Konf. 3 1430 - 1600

Chair: Said Hamdioui, TU Delft, NL
Co-Chair: Bram Kruseman, NXP, NL

This session covers various reliability modeling, characterization and mitigation approaches at different abstraction levels. The first paper uses deep learning for variability characterization. The second paper provides aging mitigation schemes for voltage regulators. The third paper addresses program vulnerability in GPU applications.

1430 **Low-Cost High-Accuracy Variation Characterization for Nanoscale IC Technologies via Novel Learning-based Techniques**

Speaker: Zhijian Pan, Tsinghua University, CN
 Authors: Zhijian Pan¹, Miao Li², Jian Yao², Hong Lu², Zuochang Ye¹, Yanfeng Li² and Yan Wang¹
¹Tsinghua University, CN; ²Platform Design Automation, Inc., CN

1500 **Mitigation of NBTI Induced Performance Degradation in On-Chip Digital LDOs**

Speaker: Longfei Wang, University of South Florida, US
 Authors: Longfei Wang¹, S. Karen Khatamifard², Ulya Karpuzcu² and Selcuk Kose¹
¹University of South Florida, US; ²University of Minnesota, US

1530 **Evaluating the Impact of Execution Parameters on Program Vulnerability in GPU Applications**

Speaker: Fritz Previlon, Northeastern University, US
 Authors: Fritz Previlon¹, Charu Kalra¹, Paolo Rech² and David Kaeli¹
¹Northeastern University, US; ²Universidade Federal do Rio Grande do Sul, BR

IPs **IP3-12, IP3-13**

1600 Coffee Break in Exhibition Area

Special Session: Next Generation Processors and Architectures for Deep Learning

Konf. 4 1430 - 1600

Chair: Theocharides Theocharis, University of Cyprus, CY
Co-Chair: Shafique Muhammad, TU Wien, AT

Machine Learning is nowadays embedded in several computing devices, consumer electronics and cyber-physical systems. Smart sensors are deployed everywhere, in applications such as wearables and perceptual computing devices, and intelligent algorithms power the so called "Internet of Things". Similarly, smart cyber-physical systems emerge as a vital computation paradigm in a vast application spectrum ranging from consumer electronics to large-scale complex critical infrastructures. The need for smartification of such systems, and intelligent data analytics (especially in the era of Big Data), emphasizes the need of revolutionizing the way we build processors and systems geared towards machine learning (and deep learning in particular). Issues related from memory, to interconnect, and spanning across the hardware and software spectrum, need to be addressed typically by advances in technology, design methodologies, and new programming paradigms among others. The emergence of powerful embedded devices and ultra-low-power hardware has enabled us to transfer the paradigm of deep learning architectures and systems, from high-end costly clusters/supercomputers, to affordable systems and even mobile devices. Such systems and devices have not received the required attention so far in research and development, until the last few years, when such systems were initially proposed to accelerate deep learning, providing previously unattainable levels of performance of such algorithms, whilst maintaining the power and reliability constraints imposed by the nature of these embedded applications. This special session aims to present a holistic overview of emerging works in such architecture and systems, using all available technology spectrums, and bring together views from academia and industry in order to exchange information and explain how we can take advantage of existing and emerging hardware technologies in addressing the associated challenges.

1430

ReRAM-based Accelerator for Deep Learning

Speaker: Hai Li, Duke university, US

Authors: Li Bing¹, Linghao Song², Fan Chen², Xuehai Qian³, Yiran Chen² and Hai (Helen) Li⁴¹Duke university, US; ²Duke University, US; ³University of South California, US; ⁴Duke University/TUM-IAS, US

1445

Exploiting Approximate Computing for Deep Learning Acceleration

Speaker: Jungook Choi, IBM Research, US

Authors: Chia-Yu Chen, Jungwook Choi, Kailash Gopalakrishnan, Viji Srinivasan and Swagath Venkataramani, IBM T. J. Watson Research Center, US

1510

An Overview of Next-Generation architectures for Machine Learning: Roadmap, Opportunities and Challenges in the IoT Era

Speaker: Muhammad Shafique, Vienna University of Technology (TU Wien), AT

Authors: Muhammad Shafique¹, Theocharis Theocharides², Christos Bouganis³, Muhammad Abdullah Haniff⁴, Faiq Khalid Lodhi⁵, Rehan Hafiz⁶ and Semeen Rehman¹¹Vienna University of Technology (TU Wien), AT; ²University of Cyprus, CY; ³Imperial College London, GB; ⁴Institute of Computer Engineering, Vienna University of Technology, AT; ⁵Department of Computer Engineering, Vienna University of Technology, AT; ⁶ITU, PK

1535

Inference of Quantized Neural Networks on Heterogeneous All-Programmable Devices

Speaker: Thomas Preusser, Xilinx Inc., IE

Authors: Thomas Preußner¹, Giulio Gambardella², Nicholas Fraser² and Michaela Blott³¹Technische Universität Dresden, DE; ²Xilinx Research Labs, IE; ³Xilinx, IE

1600

Coffee Break in Exhibition Area

7.7

Rigorous design, analysis, and monitoring of dependable embedded systems

Konf. 5 1430 - 1600

Chair: Petru Eles, Linköping University, SE**Co-Chair:** Akash Kumar, Technische Universität Dresden, DE

Dependability is a crucial aspect of embedded software systems. This session focuses on achieving dependability in different stages of the embedded software life cycle: requirements engineering, design, and maintenance. In particular, the papers presented in this session will address (1) contract based requirement engineering for cyber-physical systems, (2) formal analysis of code using SMT-based symbolic execution to deal with hardware faults, and (3) non-intrusive runtime trace analysis using FPGAs.

1430

CHASE: Contract-Based Requirement Engineering for Cyber-Physical System Design

Speaker: Pierluigi Nuzzo, University of Southern California, US

Authors: Pierluigi Nuzzo¹, Michele Lora², Yishai Feldman³ and Alberto Sangiovanni-Vincentelli⁴¹University of Southern California, US; ²University of Verona, IT; ³IBM Research, Haifa, IL; ⁴University of California at Berkeley, US

1500

Resilience Evaluation via Symbolic Fault Injection on Intermediate Code

Speaker: Hoang M. Le, University of Bremen, DE

Authors: Hoang M. Le¹, Vladimir Herdt¹, Daniel Grosse² and Rolf Drechsler²¹University of Bremen, DE; ²University of Bremen/DFKI GmbH, DE

1530

Online Analysis of Debug Trace Data for Embedded Systems

Speaker: Philip Gottschling, TU Darmstadt, DE

Authors: Normann Decker¹, Boris Dreyer², Philip Gottschling², Christian Hochberger², Alexander Lange³, Martin Leucker¹, Torben Scheffel¹, Simon Wegener⁴ and Alexander Weiss³¹Universität zu Lübeck, DE; ²TU Darmstadt, DE; ³Accemic Technologies GmbH, DE; ⁴AbsInt Angewandte Informatik GmbH, DE

1600

Coffee Break in Exhibition Area

7.8

22FDX - the superior technology for IoT, RF, Automotive and Mobility: Advanced Design Methodologies for Ultra-low Power Solutions

Exhibition Theatre 1430 - 1600

Organiser: Claudia Kretzschmar, GLOBALFOUNDRIES, DE

22FDX is the choice for applications in mobility, IoT, RF and mmWave as well as Automotive applications. It provides low active and standby power at a very small area. It is equally suited for digital as well as analog/RF/mmWave applications. The back gate bias capability provides an additional degree of freedom to the designer allowing the usage of near-threshold operation. Back gate biasing opens the possibility for many innovative design features like boosting the operation speed when needed as well as compensating for aging and process, temperature and voltage variations. Compared to other advanced node technologies 22FDX has a very low mask count which makes the technology a perfect fit for low-cost applications.

This session will give an introduction into the technology and provide an overview over design methodology. Adaptive body biasing is one of the innovative design methods that will be presented in the third talk applied to extreme low-voltage MPSoC. This session will be concluded with the design of a SoC base on the open-source PULPissimo architecture, built around a 32-bit RISC-V core.

- 1430 **22FDX: A Technology Alternative to the Mainstream optimized for IoT Applications**
Speaker: Jürgen Faul, GLOBALFOUNDRIES Fab1 LLC & Co. KG, DE
- 1450 **22FDX design methodology enabling optimized power performance and area for IoT and Mobile AP designs**
Speaker: Ulrich Hensel, GLOBALFOUNDRIES Fab1 LLC & Co. KG, DE
- 1510 **Adaptive Body bias for a 0.4V operable MPSoC in 22FDX as an example for Big data handling**
Speaker: Christian Mayr, Technische Universität Dresden, DE
- 1530 **Quentin: A Near-Threshold SoC for Energy-Efficient IoT End-Nodes in 22nm FDX Technology**
Speaker: Davide Rossi, Università di Bologna, IT
Co-authors: Pasquale Davide Schiavone¹, Davide Rossi², Antonio Pullini¹, Francesco Conti^{1,2}, Frank K. Gurkaynak¹, Luca Benini^{1,2}
¹Integrated System laboratory, ETH, Zurich, CH; ² Energy Efficient Embedded Systems Laboratory, University of Bologna, IT
- 1600 Coffee Break in Exhibition Area

IP3 Interactive Presentations

Conference Level, Foyer 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

- IP3-1 **Testbench Qualification for SystemC-AMS Timed Data Flow Models**
Speaker: Muhammad Hassan, DFKI GmbH, DE
Authors: Muhammad Hassan¹, Daniel Grosse², Hoang M. Le³, Thilo Voertler⁴, Karsten Einwich⁴ and Rolf Drechsler²
¹Cyber Physical Systems, DFKI, DE; ²University of Bremen/DFKI GmbH, DE; ³University of Bremen, DE; ⁴COSEDA Technologies GmbH, DE
- IP3-2 **An Algebra for Modeling Continuous Time Systems**
Speaker: José Medeiros, University of Brasilia, BR
Authors: José E. G. de Medeiros¹, George Ungureanu² and Ingo Sander²
¹University of Brasilia, BR; ²KTH Royal Institute of Technology, SE
- IP3-3 **TTW: A Time-Triggered Wireless Design for CPS**
Speaker: Romain Jacob, ETH Zurich, CH
Authors: Romain Jacob¹, Licong Zhang², Marco Zimmerling³, Jan Beutel¹, Samarjit Chakraborty² and Lothar Thiele¹
¹ETH Zurich, CH; ²Technical University of Munich, DE; ³Technische Universität Dresden, DE
- IP3-4 **PHYLAX: Snapshot-based Profiling of Real-Time Embedded Devices via JTAG Interface**
Speaker: Eduardo Chielle, New York University Abu Dhabi, BR
Authors: Charalambos Konstantinou¹, Eduardo Chielle² and Michail Maniatakos²
¹New York University, US; ²New York University Abu Dhabi, AE
- IP3-5 **Characterizing Display QoS Based on Frame Dropping for Power Management of Interactive Applications on Smartphones**
Speaker: Chung-Ta King, National Tsing Hua University, TW
Authors: Kuan-Ting Ho, Chung-Ta King, Bhaskar Das and Yung-Ju Chang
National Tsing Hua University, TW
- IP3-6 **Prediction-Based Fast Thermoelectric Generator Reconfiguration for Energy Harvesting from Vehicle Radiators**
Speaker: Xue Lin, Northeastern University, US

Authors: Hanchen Yang¹, Feiyang Kang², Caiwen Ding³, Ji Li⁴, Jaemin Kim⁵, Donkyu Baek⁶, Shahin Nazarian⁴, Xue Lin⁷, Paul Bogdan⁴ and Naehyuck Chang⁸

¹Beijing University of Posts and Telecommunications, CN; ²Zhejiang University, CN; ³Syracuse University, US; ⁴University of Southern California, US; ⁵Seoul National University, KR; ⁶Korea Advanced Institute of Science and Technology, KR; ⁷Northeastern University, US; ⁸KAIST, KR

- IP3-7 **A Parameterized Timing-aware Flip-flop Merging Algorithm for Clock Power Reduction**
 Speaker: Chaochao Feng, National University of Defense Technology, CN
 Authors: Chaochao Feng¹, Daheng Yue¹, Zhenyu Zhao¹ and Zhuofan Liao²
¹National University of Defense Technology, CN; ²Changsha University of Science and Technology, CN
- IP3-8 **Fast Chip-Package-PCB Coanalysis Methodology for Power Integrity of Multi-Domain High-Speed Memory: A Case Study**
 Speaker: Seungwon Kim, Ulsan National Institute of Science and Technology, KR
 Authors: Seungwon Kim¹, Ki Jin Han², Youngmin Kim³ and Seokhyeong Kang¹
¹Ulsan National Institute of Science and Technology (UNIST), KR; ²Dongguk University, KR; ³Kwangwoon University, KR
- IP3-9 **Approximate Hardware Generation using Symbolic Computer Algebra employing Gröbner Basis**
 Speaker: Saman Fröhlich, DFKI GmbH, DE
 Authors: Saman Fröhlich¹, Daniel Grosse² and Rolf Drechsler²
¹Cyber-Physical Systems, DFKI GmbH, DE; ²University of Bremen/DFKI GmbH, DE
- IP3-10 **Reconfigurable implementation of $GF(2^m)$ bit-parallel multipliers**
 Speaker and Author: José L. Imaña, Complutense University of Madrid, ES
- IP3-11 **Processing in 3D memories to speedup operations on complex data structures**
 Speaker: Luigi Carro, UFRGS, BR
 Authors: Paulo Cesar Santos, Geraldo Francisco de Oliveira Junior, Joao Paulo Lima, Marco Antonio Zanata Alves, Luigi Carro and Antonio Carlos Schneider Beck
 UFRGS - Universidade Federal do Rio Grande do Sul, BR
- IP3-12 **An Efficient NBTI-Aware Wake-Up Strategy for Power-Gated Designs**
 Speaker: Yu-Guang Chen, Yuan Ze University, TW
 Authors: Kun-Wei Chiu¹, Yu-Guang Chen² and Ing-Chao Lin¹
¹National Cheng Kung University, TW; ²Yuan Ze University, TW
- IP3-13 **Designing Reliable Processor Cores in Ultimate CMOS and Beyond: a Double Sampling Solution**
 Speaker: Nacer-Eddine Zergainoh, TIMA, FR
 Authors: Thierry Bonnoit, Fraidy Bouesse, Nacer-Eddine Zergainoh and Michael Nicolaidis, TIMA, FR
- IP3-14 **Design of a Time-predictable Multicore Processor: The T-CREST Project**
 Speaker and Author: Martin Schoeberl, Technical University of Denmark, DK
- IP3-15 **Error Resilience Analysis for Systematically Employing Approximate Computing in Convolutional Neural Networks**
 Speaker: Muhammad Abdullah Hanif, Vienna University of Technology, Vienna, AT
 Authors: Muhammad Abdullah Hanif¹, Rehan Hafiz² and Muhammad Shafique³
¹Institute of Computer Engineering, Vienna University of Technology, AT; ²TU, PK; ³Vienna University of Technology (TU Wien), AT

IP3-16 **DeMAS: An Efficient Design Methodology for Building Approximate Adders for FPGA-Based Systems**

Speaker: Semeen Rehman, Vienna University of Technology (TU Wien), AT
 Authors: Bharath Srinivas Prbakaran¹, Semeen Rehman², Muhammad Abdullah Hanif³, Salim Ullah², Ghazal Mazaheri⁴, Akash Kumar² and Muhammad Shafique¹

¹Vienna University of Technology (TU Wien), AT; ²Technische Universität Dresden, DE; ³Institute of Computer Engineering, Vienna University of Technology, AT; ⁴UC Riverside, US

IP3-17 **Gain Scheduled Control for Nonlinear Power Management in CMPs**

Speaker: Nikil Dutt, University of California at Irvine, US
 Authors: Bryan Donyanavard¹, Amir M. Rahmani², Tiago Muck¹, Kasra Moazzemi¹ and Nikil Dutt¹

¹University of California at Irvine, US
²University of California Irvine & TU Wien, US

8.1

Special Day Session on Future and Emerging Technologies: NanoSystems: Connecting Devices, Architectures, and Applications

Saal 2 1700 - 1830

Chair: Mohamed M. Sabry Aly, Nanyang Technological University, SG

This session presents end-to-end approaches for building nanosystems that enable new applications by connecting nanotechnologies for logic, memory and sensing with new architecture design. Projected energy efficiency benefits are significant. Hardware prototypes demonstrate the feasibility of such nanosystems.

1700 **3D NanoSystems: The Path to 1,000X Energy Efficiency**

Author: Max Shulaker, MIT, US

1730 **Resistive RAM for New Computing Systems: From Deep Learning to Biomimicry**

Author: Elisa Vianello, CEA LETI, FR

1800 **How Might New Technologies for Sensing Shape the Future of Computing**

Author: Naveen Verma, Princeton University, US

8.2

EU Projects: Novel Technologies, Predictable Architectures and Worst-Case Execution Times

Konf. 6 1700 - 1830

Chair: Paul Pop, Technical University of Denmark, DK

Co-Chair: Petru Eles, Linköping University, SE

This session presents the following EU projects: ARGO—developing a Worst-Case Execution Time (WCET)-aware parallelizing compilation toolchain, GREAT—aiming at using multifunctional standardized stack as a universal spintronic technology for IoT, CONNECT—highlighting the recent advancements of carbon nanotubes as interconnect material and T-CREST—which developed a real-time multicore processor to be time-predictable and an easy target for static worst-case execution time analysis.

1700 **Using Polyhedral Techniques to Tighten WCET Estimates of Optimized Code: A Case Study with Array Contraction**

Speaker: Steven Derrien, Université de Rennes 1 / IRISA, FR
 Authors: Thomas Lefeuve¹, Imen Fassi¹, Christoph Cullmann², Gernot Gebhard², Emin Koray Kasnakli³, Isabelle Puaut¹ and Steven Derrien¹
¹University of Rennes 1/IRISA, FR; ²Absint GmbH, DE; ³Fraunhofer IIS, DE

1730 **Using Multifunctional Standardized Stack as Universal Spintronic Technology for IoT**

Speaker: Mehdi Tahoori, Karlsruhe Institute of Technology, DE
 Authors: Mehdi Tahoori¹, Sarath Mohanachandran Nair¹, Rajendra Bishnoi¹, Sophiane SENNI², Jad Mohdad³, Frederick Maily³, Lionel Torres³, Pascal Benoit³, Abdoulaye Gamatie³, Pascal Nouet³, Kotb Jabeur⁴, Pierre Vanhauwaert⁴, Alexandru Atitoaie⁵, Iona Firastrau⁵, Gregory Di Pendina⁴ and Guillaume Prenat⁴
¹Karlsruhe Institute of Technology, DE; ²LIRMM, FR; ³LIRMM, Univ. of Montpellier, FR; ⁴CEA, Univ. Grenoble Alpes, FR; ⁵Transilvania University of Brasov, RO

1800 **Progress on Carbon Nanotube BEOL Interconnects**

Speaker: Benjamin Uhlig, Fraunhofer IPMS, Dresden, DE
 Authors: Benjamin Uhlig¹, Jie Liang², Jaehyun Lee³, Raphael Ramos⁴, Abitha Dhavamani¹, Nicole Nagy¹, Jean Dijon⁴, Hanako Okuno⁵, Dipankar Kalita⁵, Vihar Georgiev³, Asen Asenov³, Salvatore Amoroso⁶, Liping Wang⁶, Campbell Millar⁶, Fabian Koenemann⁷, Bernd Gotsmann⁷, Goncalo Goncalves⁸, Bingan Chen⁸, Reetu Raj Pandey², Rongmei Chen² and Aida Todri-Sanial²
¹Fraunhofer IPMS, DE; ²CNRS-LIRMM/University of Montpellier, FR; ³School of Engineering, University of Glasgow, GB; ⁴CEA-LITEN/University Grenoble Alpes, FR; ⁵CEA-INAC/University Grenoble Alpes, FR; ⁶Synopsys Inc., GB; ⁷IBM Research Zurich, CH; ⁸Aixtron Ltd., GB

1815 **A WCET-Aware Parallel Programming Model for Predictability Enhanced Multi-core Architectures**

Speaker: Simon Reder, Karlsruhe Institute of Technology (KIT), DE
 Authors: Simon Reder¹, Leonard Masing¹, Harald Bucher¹, Timon ter Braak², Timo Stripf³ and Jürgen Becker¹
¹Karlsruhe Institute of Technology (KIT), DE; ²Recore Systems B.V., NL; ³emmrix Technologies GmbH, DE

IPs **IP3-14**

8.3 **Real time intelligent methods for energy-efficient approaches in CNN and biomedical applications**

Konf. 1 1700 - 1830

Chair: Theocharis Theocharides, University of Cyprus, CY
Co-Chair: Jose L. Ayala, Dpto Arquitectura de Computadores – UCM, ES

Mobile devices and wearables require increased integration of technology for real-time applications, in particular in health and transport technology. This enables the possibility to implement machine-learning techniques directly on board. This session will firstly outline applications to detect and predict pathological health conditions, before examining real-time applications in UAVs.

1700 **Online Efficient Bio-Medical Video Transcoding on MPSoCs Through Content-Aware Workload Allocation**

Speaker: Arman Iranfar, Embedded Systems Lab (ESL), EPFL, CH
 Authors: Arman Iranfar¹, Ali Pahlevan¹, Marina Zapater¹, Martin Žagar², Mario Kovač² and David Atienza¹
¹Embedded Systems Lab (ESL), EPFL, CH; ²University of Zagreb, HR

- 1730 **Highly Efficient and Accurate Seizure Prediction on Constrained IoT Devices**
 Speaker: Farzad Samie, Karlsruhe Institute of Technology (KIT), DE
 Authors: Farzad Samie, Sebastian Paul, Lars Bauer and Joerg Henkel, Karlsruhe Institute of Technology (KIT), DE
- 1800 **A Wearable Long-Term Single-Lead ECG Processor for Early Detection of Cardiac Arrhythmia**
 Speaker: Muhammad Awais Bin Altaf, Lahore University of Management Sciences (LUMS), PK
 Authors: Syed Muhammad Abubakar, Wala Saadeh and Muhammad Awais Bin Altaf, Lahore University of Management Sciences (LUMS), PK
- 1815 **DroNet: Efficient Convolutional Neural Network Detector for Real-Time UAV Applications**
 Speaker: Christos Kyrkou, University of Cyprus, KIOS CoE, CY
 Authors: Christos Kyrkou¹, George Plastiras¹, Stylianos Venieris², Theodoris Theocharides¹ and Christos Bouganis²
¹University of Cyprus, CY; ²Imperial College London, GB
- IPs **IP3-15**

8.4 Efficient and reliable memory and computing architectures

Konf. 2 1700 - 1830

Chair: Göhringer Diana, Technische Universität Dresden, DE
Co-Chair: Jie Han, University of Alberta, CA

This session covers the exploitation of techniques to improve energy efficiency and resilience in memory and computing architectures. The first paper proposes a method using hybrid vertex-edge memory hierarchy to reduce the energy consumption of resistive random-access memory (ReRAM) systems. This method significantly improves the energy efficiency compared to conventional DRAM-based systems. The second paper examines the use of neural networks to improve resilience. The third paper addresses the performance bottleneck in von Neumann architectures by proposing an efficient algorithm for matrix multiplication in the memory of resistive associative processors (ReAPs). Finally, the last paper covers run-time application mapping on manycore systems for aging and process variations.

- 1700 **HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing**
 Speaker: Tianhao Huang, Tsinghua University, CN
 Authors: Tianhao Huang, Guohao Dai, Yu Wang and Huazhong Yang, Tsinghua University, CN
- 1730 **Accurate Neuron Resilience Prediction for a Flexible Reliability Management in Neural Network Accelerators**
 Speaker: Christoph Schorn, Robert Bosch GmbH, DE
 Authors: Christoph Schorn¹, Andre Guntoro¹ and Gerd Ascheid²
¹Robert Bosch GmbH, DE; ²RWTH Aachen University, DE
- 1800 **Rapid In-Memory Matrix Multiplication Using Associative Processor**
 Speaker: Hasan Erdem Yantir, University of California Irvine, US
 Authors: Neggaz Mohamed Ayoub¹, Hasan Erdem Yantir², Smail Niar³, Ahmed Eltawil² and Fadi Kurdahi²
¹University of Valenciennes, FR; ²University of California, Irvine, US; ³LAMIH-University of Valenciennes, FR

- 1815 **HiMap: A Hierarchical Mapping Approach for Enhancing Lifetime Reliability of Dark Silicon Manycore Systems**
 Speaker: Vivek Chaturvedi, Nanyang Technological University, SG
 Authors: Vijeta Rathore¹, Vivek Chaturvedi¹, Amit Kumar Singh², Thambipillai Srikanthan¹, Rohith R¹, Siew Kei Lam¹ and Muhammad Shafique³
¹Nanyang Technological University, SG; ²University of Essex, GB; ³Vienna University of Technology (TU Wien), AT

IPs **IP3-16, IP3-17, IP4-1**

8.5 From NBTI to IoT security: industrial experiences

Konf. 3 1700 - 1830

Chair: Doris Keitel-Schulz, Infineon Technologies, DE
Co-Chair: Norbert Wehn, University of Kaiserslautern, DE

This session covers industrial experiences from technologies such as NBTI mitigation and adaptive voltage scaling to system level aspects including safety-critical applications and IoT security.

- 1700 **NBTI Aged Cell Rejuvenation with Back Biasing and Resulting Critical Path Reordering for Digital Circuits in 28nm FDSOI**
 Speaker: Lorena Anghel, TIMA Labs, FR
 Authors: Ajith Sivasadan¹, Riddhi Jitendrakumar Shah², Vincent Huard³, Florian Cacho³ and Lorena Anghel⁴
¹TIMA Labs & ST Microelectronics, FR; ²TIMA Labs, FR; ³STMicroelectronics, FR; ⁴Grenoble-Alpes University, FR
- 1715 **An Industrial Case Study of Low Cost Adaptive Voltage Scaling Using Delay Test Patterns**
 Speaker: Mahroo Zandrahimi, TU Delft, NL
 Authors: Mahroo Zandrahimi¹, Philippe Debaud², Armand Castillejo² and Zaid Al-Ars¹
¹Delft University of Technology, NL; ²STMicroelectronics, FR
- 1730 **A Case Study for Using Dynamic Partitioning Based Solution in Volume Diagnosis**
 Speaker: Wu Yang, Mentor, A Siemens Business, US
 Authors: Tao Wang¹, Zhangchun Shi¹, Junlin Huang¹, Huaxing Tang², Wu Yang² and Junna Zhong³
¹Hisilicon Technologies Co., Ltd, CN; ²Mentor, A Siemens Business, US; ³Mentor, A Siemens Business, CN
- 1745 **On-line RF built-in self-test using noise injection and transmitter signal modulation by phase shifter**
 Speaker and Author: Jan Schat, NXP Semiconductors, DE
- 1800 **Neural Networks for Safety-Critical Applications - Challenges, Experiments and Perspectives**
 Speaker: Chih-Hong Cheng, fortiss, DE
 Authors: Chih-Hong Cheng¹, Frederik Diehl², Yassine Hamza², Gereon Hinz², Georg Nührenberg², Markus Rickert², Harald Ruess² and Michael Truong-Le²
¹fortiss - Landesforschungsinstitut des Freistaats Bayern, DE; ²fortiss GmbH, DE
- 1815 **IoT Security Assessment through the Interfaces P-SCAN Test Bench Platform**
 Speaker: Thomas Maurin, CEA, Leti, Univ. Grenoble Alpes, FR
 Authors: Thomas Maurin¹, Laurent-Frédéric Ducreux¹, George Caraiman² and Philippe Sissoko²
¹CEA Leti, Univ. Grenoble Alpes, FR; ²LCIE Bureau Veritas, FR

Designing reliable embedded architectures under uncertainty

Konf. 4 1700 - 1830

Chair: Oliver Bringmann, Universität Tübingen, DE**Co-Chair:** Amit Singh, University of Essex, GB

Reliability is a target which can be reached in some different ways, by using, for instance, fault-tolerant architectures or by exploiting adaptable architecture. The session presents original contributions in both directions. On the first paper, reconfigurable VLIW processors are targeted by means of dynamic binary translation to explore a performance-energy trade-off. The following two papers propose solutions for fault prevention, detection and isolation, without compromising performance. In the last paper, the potential use of approximate, low-power functional units is targeted while remaining within the overall error budget of an application.

1700 **Supporting Runtime Reconfigurable VLIWs Cores Through Dynamic Binary Translation**

Speaker: Simon Rokicki, Univ Rennes, INRIA, CNRS, IRISA, FR

Authors: Simon Rokicki¹, Erven Rohou² and Steven Derrien³¹Irisa, FR; ²Inria, FR; ³University of Rennes 1/IRISA, FR1730 **uSFI: Ultra-Lightweight Software Fault Isolation for IoT-Class Devices**

Speaker: Zelalem Aweke, University of Michigan, US

Authors: Zelalem Birhanu Aweke and Todd Austin, University of Michigan, US

1800 **Converging Safety and High-performance Domains: Integrating OpenMP into Ada**

Speaker: Sara Royuela, Barcelona Supercomputing Center, ES

Authors: Sara Royuela¹, Eduardo Quinones¹ and Luis Miguel Pinho²¹barcelona supercomputing center, ES; ²polytechnic institute of porto, PT1815 **Compiler-Driven Error Analysis for Designing Approximate Accelerators**

Speaker: Jorge Castro-Godínez, Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), DE

Authors: Jorge Castro-Godínez¹, Sven Esser¹, Muhammad Shafique², Santiago Pagani¹ and Joerg Henkel¹¹Karlsruhe Institute of Technology, DE; ²Vienna University of Technology (TU Wien), ATIPs **IP4-2, IP4-3, IP4-4****22FDX - the superior technology for IoT, RF, Automotive and Mobility: Best-in Class RF, 5G and mmWave designs**

Exhibition Theatre 1700 - 1830

Organiser: Claudia Kretzschmar, GLOBALFOUNDRIES, DE

This session focusses on the RF and mmWave capabilities of 22FDX where the technology has a great advantage over bulk or FinFET technologies: 22FDX is the best choice for any application where lowest analog and RF/mmWave circuit power consumption is desired. It offers a high peak frequency performance (Ft, Fmax), enables great integration of PA due to a high stacking efficiency and has one of the best CMOS switch behaviors due to low Ron and better Ron*Coff than FinFET or bulk technologies and a low-loss BEOL.

22FDX combines the best of RF performance of SiGe and PDSOI into one process technology, giving designers the opportunity to design best in class switches, LNA's and PA's onto a single die, integrated with transceiver and digital baseband

The first talk of this session will present RF integrated circuits for multi-

Gbps communication and provide two examples which are best in class regarding frequency of operation, broadest frequency band, energy efficiency and area.

The second presentation highlights the strengths of 22FDX regarding noise and linearity demonstrating smart mixed-signal calibration techniques in order to meet the performance targets at minimum power consumption and smallest silicon area.

Another outstanding application are N-Path Filters for "Software Defined Radios" which are being addressed in the third talk. N-path filters benefit from CMOS scaling as switch parasitics improve, and increasingly higher digital clock frequencies are feasible.

The fourth presentation concludes this session describing a mmWave circuit design example on how to utilize the 22FDX features.

1700 **Best-in Class RF integrated circuits for multi-Gbps communication in 22FDX**

Speaker: Corrado Carta, Technical University Dresden, DE

1720 **Smart Data Converters for Wireline and Wireless Systems using 22FDX**

Speaker: Friedel Gerfers, Technical University Berlin, DE

1740 **N-Path Filters and Mixers Controllable by a Digital Multi-Phase Clock**

Speaker: Eric Klumperink, University of Twente, NL

1800 **MM-wave circuit design using GLOBALFOUNDRIES 22FDX**

Speaker: Aarno Pärssinen, University of Oulu, FI

Co-authors: Janne P. Aikio¹, Mikko Hietanen², Henri Hurskainen², Timo Rahkonen¹, Aarno Pärssinen²

¹Circuits and systems Research unit, University of Oulu, FI; ²Center for Wireless Communication - Radio Technologies, University of Oulu, FI

Party

DATE Party | Networking Event

Deutsches Hygiene-Museum Dresden 1930 - 2300

The highlight of the DATE week will again be the DATE Party, which offers the perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. Thus, it states one of the main networking opportunities during the DATE week.

The party is scheduled on March 21, 2018, from 1930 to 2300, and will take place in the Deutsches Hygiene-Museum Dresden.

During the evening, all delegates will have the chance to visit the different expositions for free.

All delegates, exhibitors and their guests are invited to attend the party. Please be aware that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Price for extra ticket: EUR 70.00 per person.

A bus shuttle from the congress centre to the Hygiene-Museum Dresden will be organized, starting at 1900 from the main entrance of the ICC Dresden.

→ See Page 13

9.1

Special Day Session on Designing Autonomous Systems: Embedded Machine Learning

Saal 2 0830 - 1000

Chair: **Ahmed Jerraya**, CEA, FR

Autonomous systems will use machine learning techniques to deal with uncertainty and to accomplish intelligent tasks. In the case of cyberphysical systems, machine learning allow to solve complex tasks however it requires novel hardware and software solutions to achieve the required performances. This session introduces the knowledge chain for embedded machine learning. It includes talks on application needs, existing approaches and design tools.

0830 **Automotive Application Requirements for Embedded Machine Learning**

Speaker and Author: Dirk Ziegenbein, Robert Bosch GmbH, DE

0900 **Overview of the state of the art in embedded machine learning**

Speaker: Frédéric Pétrot, TIMA Lab, Univ. Grenoble Alpes, FR
 Authors: Liliana Andrade¹, Adrien Prost-Boucle¹ and Frédéric Pétrot²
¹Univ. Grenoble Alpes, CNRS, Grenoble INP, FR; ²TIMA Lab, Université Grenoble Alpes, FR

0930 **PNeuro: a scalable energy-efficient programmable hardware accelerator for neural networks**

Speaker: Nicolas VENTROUX, CEA LIST, FR
 Authors: Alexandre Carbon¹, Jean-Marc PHILIPPE¹, Olivier Bichler¹, Renaud Schmit¹, David Briand¹, Benoit Tain¹, Nicolas Ventroux¹, Michel Paindavoine² and Olivier Brousse²
¹CEA LIST, FR; ²GlobalSensing Technologies, FR

1000 Coffee Break in Exhibition Area

9.2

Emerging architectures and technologies for ultra low power and efficient embedded systems

Konf. 6 0830 - 1000

Chair: **Johanna Sepulveda**, Technical University of Munich, DE
 Co-Chair: **Amato Paolo**, Micron Technology, IT

New waves of architectures and technologies are emerging with the potential of bringing high efficiency and ultra low power in future embedded systems. This session on one hand focuses on the datapath with advances in neural networks, deep learning, and mix-precision accelerators. On the other hand it presents new technologies for non-volatile memories, and bus coding techniques for volatile memories

0830 **FFT-Based Deep Learning Deployment in Embedded Systems**

Speaker: Sheng Lin, Syracuse University, US
 Authors: Sheng Lin¹, Ning Liu¹, Mahdi Nazemi², Hongjia Li¹, Caiwen Ding¹, Yanzhi Wang³ and Massoud Pedram²
¹Syracuse University, US; ²USC, US; ³University of Southern California, US

0900 **A Transprecision Floating-Point Platform for Ultra-Low Power Computing**

Speaker: Giuseppe Tagliavini, Università di Bologna, IT
 Authors: Giuseppe Tagliavini¹, Stefan Mach², Davide Rossi¹, Andrea Marongiu² and Luca Benini¹
¹Università di Bologna, IT; ²ETH Zurich, CH

0930 **A Peripheral Circuit Reuse Structure Integrated with a Retimed Data Flow for Low Power RRAM Crossbar-based CNN**

Speaker: Keni Qiu, Capital Normal University, CN
 Authors: Keni Qiu¹, Weiwen Chen¹, Yuanchao Xu¹, Lixue Xia², Yu Wang² and Zili Shao³

¹Capital Normal University, CN; ²Tsinghua University, CN; ³The Hong Kong Polytechnic University, HK

0945 **Optimal DC/AC Data Bus Inversion Coding**

Speaker: Jan Lucas, TU Berlin, DE
 Authors: Jan Lucas, Sohan Lal and Ben Juurlink, TU Berlin, DE

IPs **IP4-5, IP4-6**

1000 Coffee Break in Exhibition Area

9.3

Advances in Reconfigurable Computing

Konf. 1 0830 - 1000

Chair: Jürgen Teich, Friedrich-Alexander Universität, DE
Co-Chair: Florent de Dinechin, INSA-Lyon, FR

This session presents four papers advancing the current state of the art in Coarse Grain Reconfigurable Architectures and two interactive presentations dealing with posit arithmetic and convolution neural networks.

0830 **LASER: A Hardware/Software Approach to Accelerate Complicated Loops on CGRAs**

Speaker: Shail Dave, Arizona State University, US
 Authors: Mahesh Balasubramanian¹, Shail Dave¹, Aviral Shrivastava¹ and Riley Jeyapaul²

¹Arizona State University, US; ²ARM Research, GB

0900 **A Time-Multiplexed FPGA Overlay with Linear Interconnect**

Speaker: Xiangwei Li, Nanyang Technological University, SG
 Authors: Xiangwei Li¹, Abhishek Kumar Jain², Douglas L. Maskell¹ and Suhaib A. Fahmy³

¹Nanyang Technological University, SG; ²Lawrence Livermore National Laboratory, US; ³University of Warwick, GB

0930 **URECA: A Compiler Solution to Manage Unified Register File for CGRAs**

Speaker: Shail Dave, Arizona State University, US
 Authors: Shail Dave, Mahesh Balasubramanian and Aviral Shrivastava, Arizona State University, US

0945 **Optimizing the data placement and transformation for multi-bank CGRA computing system.**

Speaker: Zhongyuan Zhao, Shanghai Jiao Tong University, CN
 Authors: Zhongyuan Zhao¹, Yantao Liu¹, Weiguang Sheng¹, Tushar Krishna², Qin Wang¹ and Zhigang Mao¹

¹Shanghai JiaoTong University, CN; ²Georgia Institute of Technology, US

IPs **IP4-7, IP4-8**

1000 Coffee Break in Exhibition Area

EU Projects: Novel Platforms – from Self-Aware MPSoCs to Server Ecosystems

Konf. 2 0830 - 1000

Chair: Martin Schoeberl, Technical University of Denmark, DK
Co-Chair: Flavius Gruian, Lund University, SE

This session presents three EU projects. The EU projects are: dReDBox—developing the next generation, low-power, across form-factor datacenters, enabling the creation of A338:AN521-as-a-unit, UniServer—developing a universal system architecture and software ecosystem for servers targeting cloud data-centers as well as upcoming edge-computing markets and OPRECOMP—developing concepts, methods, hardware and software building blocks for practical transprecision computing systems.

0830 dReDBox: Materializing a Full-stack Rack-scale System Prototype of a Next-Generation Disaggregated Datacenter

Speaker: Dimitris Syrivelis, IBM Research, Ireland, GR

Authors: Maciel Bielski¹, Ilias Syrigos², Kostas Katrinis³, Dimitris Syrivelis³, Andrea Reale³, Dimitris Theodoropoulos⁴, Nikolaos Alachiotis⁵, Dionisios Pnevmatikatos⁶, Evert Pap⁷, George Zervas⁸, Vaibhawa Mishra⁸, Arsalan Saljoghei⁸, Alvis Rigo⁹, Jose Fernando Zazo¹⁰, Sergio Lopez-Buedo¹⁰, Ferad Zyulkyarov¹¹, Michael Enrico¹² and Osar-Gonzalez de Dios¹³
¹Virtual Open Systems, FR; ²University of Thessaly, GR; ³IBM Research, Ireland, IE; ⁴Foundation for Research and Technology Hellas (FORTH), GR; ⁵Foundation for Research and Technology Hellas (FORTH), GR; ⁶ECE Department, Technical University of Crete & FORTH-ICS, GR; ⁷SINTECS, Netherlands, NL; ⁸University College London, GB; ⁹Virtual Open Systems, France, FR; ¹⁰NAUDIT HPCN, Spain, ES; ¹¹Barcelona Supercomputing Center, Spain, ES; ¹²POLATIS, UK, GB; ¹³TELEFONICA, Spain, ES

0900 An Energy-Efficient and Error-Resilient Server Ecosystem Exceeding Conservative Scaling Limits

Speaker: Georgios Karakonstantis, Queen's University Belfast, GB

Authors: Georgios Karakonstantis¹, Konstantinos Tovletoglou², Lev Mukhanov¹, Hans Vandierendonck¹, Dimitrios Nikolopoulos², Peter Lawthers³, Panos Koutsovasilis⁴, Manolis Maroudas⁵, Christos D. Antonopoulos⁴, Christos Kalogirou⁴, Nikolaos Bellas⁶, Spyros Lalis⁴, Srikumar Venugopal⁷, Arnau Prat-Perez⁸, Alejandro Lampropoulos⁹, Marios Kleantous¹⁰, Andreas Diavastos¹¹, Zacharias Hadjilambrou¹¹, Panagiota Nikolaou¹¹, Yanos Sazeides¹², Pedro Trancoso¹³, George Papadimitriou¹³, Manolis Kaliorakis¹³, Athanasios Chatzidimitriou¹³, Dimitris Gizopoulos¹³ and Shidhartha Das¹⁴
¹Queen's University Belfast, GB; ²Queen's University of Belfast, GB; ³A.M.C.C. Deutschland, DE; ⁴University of Thessaly, GR; ⁵University of Thessaly, GB; ⁶University of Thessaly & CERTH, GR; ⁷IBM Research - Ireland, IE; ⁸Sparsity, ES; ⁹Worldsensing, ES; ¹⁰Meritorious, CY; ¹¹University of Cyprus, CY; ¹²u cyprus, CY; ¹³University of Athens, GR; ¹⁴ARM Ltd., GB

0930 The Transprecision Computing Paradigm: Concept, Design, and Applications

Speaker: A. Cristiano I. Malossi, IBM Research - Zurich, CH

Authors: Cristiano I. Malossi¹, Michael Schaffner², Anca Molnos³, Luca Gammaitoni⁴, Giuseppe Tagliavini⁵, Andrew Emerson⁶, Andrés Tomás⁷, Dimitrios S. Nikolopoulos⁸, Eric Flamand⁹ and Norbert Wehn¹⁰
¹IBM Research - Zurich, CH; ²ETHZ, CH; ³CEA, FR; ⁴Università di Perugia, IT; ⁵Università di Bologna, IT; ⁶CINECA, IT; ⁷Universitat Jaume I, ES; ⁸Queen's University of Belfast, GB; ⁹GreenWaves Technologies, FR; ¹⁰University of Kaiserslautern, DE

1000 Coffee Break in Exhibition Area

9.5

Physical Attacks

Konf. 3 0830 - 1000

Chair: Bilge Kavun Elif, Infineon Technologies, DE**Co-Chair:** Batina Lejla, Radboud University, NL

Electronic circuits are increasingly processing sensitive confidential data, such as personal information. In this session, new types of attacks to extract such data out of circuits are discussed in-depth. They encompass passive side-channel attacks and active manipulations of circuits.

0830

An Inside Job: Remote Power Analysis Attacks on FPGAs

Speaker: Falk Schellenberg, Ruhr-Universität Bochum, DE

Authors: Falk Schellenberg¹, Dennis Gnad², Amir Moradi¹ and Mehdi Tahoori²¹Ruhr University Bochum, DE; ²Karlsruhe Institute of Technology, DE

0900

Confident Leakage Detection - A Side-Channel Evaluation Framework based on Confidence IntervalsAuthors: Florian Bache¹, Christina Plump¹ and Tim Güneysu²¹University of Bremen, DE; ²University of Bremen & DFKI, DE

0930

Øzone: Efficient Execution with Zero Timing Leakage for Modern Microarchitectures

Speaker: Zelalem Aweke, University of Michigan, US

Authors: Zelalem Birhanu Aweke and Todd Austin, University of Michigan, US

0945

SCADPA: Side-Channel Assisted Differential-Plaintext Attack on Bit Permutation Based Ciphers

Speaker: Jakub Breier, Nanyang Technological University, SG

Authors: Jakub Breier¹, Dirmanto Jap¹ and Shivam Bhasin²¹Nanyang Technological University, SG; ²Temasek Laboratories, Nanyang Technological University, SG

IPs

IP4-9, IP4-10

1000

Coffee Break in Exhibition Area

Conference Level, Foyer 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

- IP4-1 Efficient Mapping of Quantum Circuits to the IBM QX Architectures**
 Speaker: Alwin Zulehner, Johannes Kepler University Linz, AT
 Authors: Alwin Zulehner, Alexandru Paler and Robert Wille, Johannes Kepler University Linz, AT
- IP4-2 Parallel Code Generation of Synchronous Programs for a Many-core Architecture**
 Speaker: Amaury Graillat, Verimag - Univ. Grenoble Alpes, FR
 Authors: Amaury Graillat¹, Matthieu Moy², Pascal Raymond³ and Benoît Dupont de Dinechin⁴
¹Verimag - Univ. Grenoble Alpes, FR; ²Univ. Grenoble Alpes, Verimag, FR; ³VERIMAG/CNRS, FR; ⁴Kalray, FR
- IP4-3 SOCRATES - A Seamless Online Compiler and System Runtime AutoTuning Framework for Energy-Aware Applications**
 Speaker: Gianluca Palermo, Politecnico di Milano, IT
 Authors: Davide Gadioli¹, Ricardo Nobre², Pedro Pinto³, Emanuele Vitali¹, Amir H. Ashouri⁴, Gianluca Palermo¹, Cristina Silvano¹ and João M. P. Cardoso⁵
¹Politecnico di Milano, IT; ²University of Porto / INESC TEC, PT; ³Faculty of Engineering, University of Porto, PT; ⁴University of Toronto, Canada, CA; ⁵University of Porto, PT
- IP4-4 Non-Intrusive Program Tracing of Non-Preemptive Multitasking Systems Using Power Consumption**
 Speaker: Kamal Lamichhane, University of Waterloo, CA
 Authors: Kamal Lamichhane, Carlos Moreno and Sebastian Fischmeister, University of Waterloo, CA
- IP4-5 Energy-Performance Design Exploration of a Low-Power Microprogrammed Deep-Learning Accelerator**
 Speaker: Andrea Calimera, Politecnico di Torino, IT
 Authors: Andrea Calimera¹, Mario R. Casu², Giulia Santoro¹, Valentino Peluso¹ and Massimo Alioto³
¹Politecnico di Torino, IT; ²Politecnico di Torino, Department of Electronics and Telecommunications, IT; ³National University of Singapore, SG
- IP4-6 GenPIM: Generalized Processing In-Memory to Accelerate Data Intensive Applications**
 Speaker: Tajana Rosing, UC San Diego, US
 Authors: Mohsen Imani, Saransh Gupta and Tajana Rosing, University of California San Diego, US
- IP4-7 Universal Number Posit Arithmetic Generator on FPGA**
 Speaker: Hayden K.-H. So, The University of Hong Kong, HK
 Authors: Manish Kumar Jaiswal and Hayden So, The University of Hong Kong, HK
- IP4-8 Block Convolution: Towards Memory-Efficient Inference of Large-Scale CNNs on FPGA**
 Speaker: Gang Li, Institute of Automation, Chinese Academy of Sciences, CN
 Authors: Gang Li, Fanrong Li, Tianli Zhao and Jian Cheng, Institute of Automation, Chinese Academy of Sciences, CN
- IP4-9 Examining the Consequences of High-Level Synthesis Optimizations on the Power Side Channel**
 Speaker: Lu Zhang, Northwestern Polytechnical University, CN
 Authors: Lu Zhang¹, Wei Hu², Armaiti Ardeshiricham², Yu Tai¹, Jeremy Blackstone², Dejun Mu¹ and Ryan Kastner²
¹Northwestern Polytechnical University, CN; ²University of California, San Diego, US

- IP4-10** **DFARPA: Differential Fault Attack Resistant Physical Design Automation**
 Speaker: Jakob Breier, Nanyang Technological University, SG
 Authors: Mustafa Khairallah¹, Rajat Sadhukhan², Radhemanjari Samanta², Jakob Breier¹, Shivam Bhasin³, Rajat Subhra Chakraborty⁴, Anupam Chattopadhyay¹ and Debdeep Mukhopadhyay⁵
¹Nanyang Technological University, SG; ²Indian Institute of Technology Kharagpur, IN; ³Temasek Laboratories, Nanyang Technological University, SG; ⁴Assistant Professor, Computer Science and Engineering, IIT Kharagpur, IN; ⁵Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur, IN
- IP4-11** **An Energy-Efficient Stochastic Computational Deep Belief Network**
 Speaker: Jie Han, University of Alberta, CA
 Authors: Yidong Liu¹, Yanzhi Wang², Fabrizio Lombardi³ and Jie Han¹
¹University of Alberta, CA; ²Syracuse university, US; ³Northeastern University, US
- IP4-12** **Pushing the Number of Qubits Below the “Minimum”: Realizing Compact Boolean Components for Quantum Logic**
 Speaker: Alwin Zulehner, Johannes Kepler University Linz, AT
 Authors: Alwin Zulehner and Robert Wille, Johannes Kepler University Linz, AT
- IP4-13** **Power Optimization Through Peripheral Circuit Reusing Integrated with Loop Tiling for RRAM Crossbar-based CNN**
 Authors: Yuanhui Ni, Weiwen Chen and Keni Qiu, Capital Normal University, CN
- IP4-14** **ORIENT: Organized Interleaved ECCs for New STT-RAM Caches**
 Speaker: Hamed Farbeh, School of Computer Science, Institute for Research in Fundamental Sciences (IPM), IR
 Authors: Zahra Azad¹, Hamed Farbeh² and Amir Mahdi Hosseini Monazzah³
¹Sharif University of Technology, IR; ²School of Computer Science, Institute for Research in Fundamental Sciences (IPM), IR; ³Department of Computer Engineering, Sharif University of Technology, Tehran, Iran, IR
- IP4-15** **ERASMUS: Efficient Remote Attestation via Self-Measurement for Unattended Settings**
 Speaker: Norrathep Rattanavipanon, University of California, Irvine, US
 Authors: Xavier Carpent, Norrathep Rattanavipanon and Gene Tsudik UC Irvine, US
- IP4-16** **End-to-end Latency Analysis of Cause-effect Chains in an Engine Management System**
 Speaker: Junchul Choi, Seoul National University, KR
 Authors: Junchul Choi, Donghyun Kang and Soonhoi Ha, Seoul National University, KR
- IP4-17** **General Floorplanning Methodology for 3D ICs with An Arbitrary Bonding Style**
 Speaker: Chien-Yu Huang, Department of Electrical Engineering, National Cheng Kung University, TW
 Authors: Jai-Ming Lin and Chien-Yu Huang, Department of Electrical Engineering, National Cheng Kung University, TW

10.1

Special Day Session on Designing Autonomous Systems: Digitalization in automotive and industrial systems

Saal 2 1100 - 1230

Chair: Matthias Traub, BMW, DE

Autonomous systems are an important part of today's and future solutions for the automotive and industrial sector. The research and development activities to enable high/full automated driving and industry 4.0 have to deal with a lot of new requirements (e.g. fail operational, cyber security), technologies (connectivity over 5G, neuronal networks, future computing platforms) and topics (data analytics, artificial intelligence). Furthermore, processes, methods and tools lag behind and need to speed up to cope with all the consequences in validation and verification. The short paper will give an overview over these challenges and the actual state of research and the development in the field of digital autonomous systems.

1100 **Auto in Motion - Trends in Automotive Engineering**

Author: Eric Sax, Karlsruhe Institute of Technology, DE

1115 **Driving and being driven: future mobility and technological enablers**

Author: Hans-Jörg Vögel, BMW Group, DE

1140 **Digitalization in the Industry Automation - From the Component to the Cloud**

Author: Thilo Streichert, Festo AG & Co. KG, DE

1205 **5G Challenges for Connected, Cooperative and Automated Transport Systems**

Author: Jérôme Härri, Eurecom - Communication systems, FR

1230 Lunch Break in Großer Saal and Saal 1

10.2

Neural Networks and Neurotechnology

Konf. 6 1100 - 1230

Chair: Jim Harkin, University of Ulster, GB**Co-Chair: Robert Wille**, University of Linz, AT

New approaches to energy efficiency in neural networks using approximate computing and non-volatile FeFET memory are presented. A novel inductive coupling interconnect approach for neurotechnology applications and an optimisation strategy for efficiently mapping spiking neural networks to neuromorphic hardware are also presented.

1100 **Design and Optimization of FeFET-based Crossbars for Binary Convolution Neural Networks**

Speaker: Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, CN

Authors: Xiaoming Chen, Xunzhao Yin, Michael Niemier and Xiaobo Sharon Hu, University of Notre Dame, US

1130 **Low-Power 3D Integration using Inductive Coupling Links for Neurotechnology Applications**

Speaker: Benjamin Fletcher, University of Southampton, GB

Authors: Benjamin Fletcher¹, Shidhartha Das², Chi-Sang Poon³ and Terrence Mak¹¹University of Southampton, GB; ²ARM Ltd., GB;³Massachusetts Institute of Technology, US1200 **Mapping of Local and Global Synapses on Spiking Neuromorphic Hardware**

Speaker: Francky Catthoor, IMEC Fellow, BE

Authors: Anup Das¹, Yuefeng Wu¹, Khanh Huynh¹, Francesco Dell'Anna², Francky Catthoor² and Siebren Schaafsma¹¹IMEC, NL; ²IMEC, BE

- 1215 **Energy-Efficient Neural Networks using Approximate Computation Reuse**
 Speaker: Xun Jiao, University of California San Diego, US
 Authors: Xun Jiao¹, Vahideh Akhlaghi¹, Yu Jiang² and Rajesh Gupta¹
¹University of California, San Diego, US; ²Tsinghua University, CN

IPs **IP4-11, IP4-12**

1230 Lunch Break in Großer Saal and Saal 1

10.3

From Non-Volatile Flip-Flops to Storage Systems

Konf. 1 1100 - 1230

Chair: Alexandre Levisse, EPFL, CH

Co-Chair: Weisheng Zhao, Beihang University, CN

This session combines research from circuit to system level on non-volatile memories. The first paper proposes an STT-MRAM-based multi-bit non-volatile flip-flop. The other papers address system-level challenges, such as write disturbance mitigation, wear levelling scheme and latency reduction, for various technologies (PCM, SSD-flash).

- 1100 **Multi-Bit Non-Volatile Spintronic Flip-Flop**
 Speaker: Rajendra Bishnoi, Karlsruhe Institute of Technology, DE
 Authors: Christopher Münch, Rajendra Bishnoi and Mehdi Tahoori, Karlsruhe Institute of Technology, DE
- 1130 **ADAM: Architecture for Write Disturbance Mitigation in Scaled Phase Change Memory**
 Speaker: Shivam Swami, University of Pittsburgh, US
 Authors: Shivam Swami and Kartik Mohanram, University of Pittsburgh, US
- 1200 **Program Error Rate-based Wear Leveling for NAND Flash Memory**
 Speaker: Fei Wu, Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, CN
 Authors: Xin Shi¹, Fei Wu¹, Shunzhuo Wang¹, Changsheng Xie¹ and Zhonghai Lu²
¹Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, CN; ²KTH Royal Institute of Technology, SE
- 1215 **ShadowGC: Cooperative Garbage Collection with Multi-level Buffer for Performance Improvement in NAND flash-based SSDs**
 Speaker: Jinhua Cui, Xi'an Jiaotong University, CN
 Authors: Jinhua Cui¹, Youtao Zhang², Jianhang Huang¹, Weiguo Wu¹ and Jun Yang²
¹Xi'an Jiaotong University, CN; ²University of Pittsburgh, US
- IPs **IP4-13, IP4-14, IP5-16**
- 1230 Lunch Break in Großer Saal and Saal 1

10.4 Cryptographic Hardware

Konf. 2 1100 - 1230

Chair: Nele Mentens, Katholieke Universiteit Leuven, BE**Co-Chair:** Tim Güneysu, Ruhr-Universität Bochum, DE

This session presents novel ideas realized in hardware for cryptographic systems. The contributions range from implementations of leakage resilient cryptography in ASICs, to FPGA realizations of novel public-key primitives as well as optimization of FPGA resources used by random number generation schemes.

1100 **Binary Ring-LWE Hardware with Power Side-Channel Countermeasures**

Speaker: Aydin Aysu, The University of Texas at Austin, US

Authors: Aydin Aysu, Mohit Tiwari and Michael Orshansky, University of Texas at Austin, US

1130 **High Speed ASIC Implementations of Leakage-Resilient Cryptography**

Speaker: Thomas Unterluggauer, Graz University of Technology, AT

Authors: Robert Schilling¹, Thomas Unterluggauer², Stefan Mangard², Frank Gurkaynak³, Michael Muehlberghuber⁴ and Luca Benini⁵¹Graz University of Technology / Know Center GmbH, AT; ²Graz University of Technology, AT; ³ETH Zurich, CH; ⁴Integrated Systems Laboratory (ETH Zurich), CH; ⁵Università di Bologna, IT1200 **Optimization of the PLL Configuration in a PLL-based TRNG Design**

Speaker: Elie Noumon Allini, Laboratoire Hubert Curien, University of Saint-Etienne, FR

Authors: Elie Noumon Allini, Oto Petura, Viktor Fischer and Florent Bernard, Hubert Curien Laboratory, Jean Monnet University, FR

IPs **IP4-15, IP5-14**

1230 Lunch Break in Großer Saal and Saal 1

10.5 **Mixed-Criticality and Fault-Tolerant Real-Time Embedded Systems**

Konf. 3 1100 - 1230

Chair: Leandro Indrusiak, Univ. of York, GB**Co-Chair:** Andy Pimentel, University of Amsterdam, DE

The session presents advances in mixed criticality systems related to Availability, Memory Bandwidth and Fault-Tolerance. The first paper details on service degradation in mixed criticality systems. The second paper handles mixed-critical workloads in the presences of memory contention. The third paper considers fault-tolerance to be incorporated into control algorithms.

1100 **Availability Enhancement and Analysis for Mixed-Criticality Systems on Multi-core**

Speaker: Roberto Medina, Télécom ParisTech, FR

Authors: Roberto Medina, Etienne Borde and Laurent Pautet, Télécom ParisTech, FR

1130 **Mixed-criticality Scheduling with Memory Bandwidth Regulation**

Speaker: Muhammad Ali Awan, CISTER/INESC-TEC and ISEP/IPP, Porto, Portugal, PT

Authors: Muhammad Ali Awan¹, Pedro Souto², Konstantinos Bletsas³, Benny Akesson³ and Eduardo Tovar⁴¹CISTER Research Centre, PT; ²Faculty of Engineering of the University of Porto, PT; ³CISTER/INESC-TEC, ISEP, PT; ⁴CISTER/INESC-TEC, PT

- 1200 **Design and Validation of Fault-tolerant Embedded Controllers**
 Speaker: Soumyajit Dey, IIT Kharagpur, IN
 Authors: Saurav Kumar Ghosh¹, Soumyajit Dey², Dip Goswami³, Daniel Mueller-Gritschneider⁴ and Samarjit Chakraborty⁴
¹Dept. of CSE, IIT Kharagpur, IN; ²Indian Institute of Technology Kharagpur, IN; ³Eindhoven University of Technology, NL; ⁴Technical University of Munich, DE

IPs **IP4-16, IP5-12**

1230 Lunch Break in Großer Saal and Saal 1

10.6

Special Session: Computing with Ferroelectric FETs - Devices, Models, Systems, and Applications

Konf. 4 1100 - 1230

Chair: Michael Niemier, University of Notre Dame, US

Co-Chair: Ian O'Connor, Ecole Centrale de Lyon, FR

In this session, we consider devices, circuits, and systems comprised of transistors with integrated ferroelectrics. Said structures are actively being considered by various semiconductor manufacturers as they can address a large and unique design space. Transistors with integrated ferroelectrics could (i) enable a better switch (i.e., offer steeper subthreshold swings), (ii) are CMOS compatible, (iii) have multiple operating modes (i.e., I-V characteristics can also enable compact, 1-transistor, non-volatile storage elements, as well as analog synaptic behavior), and (iv) have been experimentally demonstrated (i.e., with respect to all of the aforementioned operating modes). These device-level characteristics offer unique opportunities at the circuit, architectural, and system-level, and are considered from device, circuit/architecture, and foundry-level perspectives.

- 1100 **Outlook for low-power beyond-CMOS devices**
 Author: An Chen, Semiconductor Research Corporation, US
- 1130 **Exploiting Ferroelectric FETs: From Logic-in-Memory to Neural Networks and Beyond**
 Author: Xiaobo Sharon Hu, University of Notre Dame, US
- 1200 **FeFETs: from non-volatile memory to non-volatile computing**
 Author: Stefan Slesazeck, NaMLab gGmbH, DE
- 1230 Lunch Break in Großer Saal and Saal 1

An Industry Approach to FPGA and SOC System Development and Verification

Exhibition Theatre 1100 - 1230

Organiser: Alexander Schreiber, The MathWorks, DE**Speaker:** John Zhao, MathWorks, US

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

In this exhibition theater session, you will learn

Automatically generate synthesizable RTL code from you MATLAB and Simulink algorithms targeting FPGA, ASIC or Programmable SoC

A HW/SW co-design workflow that combines system level design and simulation with automatic code generation

Functional verification using MATLAB and Simulink in a SystemVerilog workflow illustrated by a detailed example

1230

Lunch Break in Großer Saal and Saal 1

**LUNCH TIME KEYNOTE SESSION:
Autonomous Driving: Ready to Market?
Which are the Remaining Top Challenges?**

Saal 2 1320 - 1350

Chair: Ayse Coskun, Boston University, US

During the last years a lot of prototypes for automated/autonomous driving vehicles have been presented to the public. Depending on the use case car manufacturers or tech companies have used an evolutionary or a revolutionary approach. While the evolutionary way should be more reasonable applied for owned cars due to cost restraints and the need for the functionality to work more or less by "something everywhere", the revolutionary approach following the strategy "everything somewhere" seems to be the better solution for fleets of autonomous cabs or shuttles. Although we have seen a lot of functional concepts for both approaches to automation, there are still some big challenges to be solved. On one hand the whole automation function has to be designed redundantly to ensure a sufficient functional safety level. In this context the use of Artificial Intelligence based networks could be a solution in particular neuronal networks based on deep learning. On the other hand there is still the question "how good is good enough" having in mind that perfectly working systems cannot be realized and how can the necessary verification/validation process be implemented. The public funded project PEGASUS is working to provide first answers. However: do we have considered all impacts of automated mobility?

1320

Autonomous driving: Ready to market? Which are the remaining top challenges?

Author and Speaker: Thomas Form, Head of Electronics and Vehicle Research, Volkswagen AG, and co-ordinator of the Pegasus research project on safety of automated driving, DE

11.1

Special Day Session on Designing Autonomous Systems: Smart Vision Systems

Saal 2 1400 - 1530

Chair: Bernhard Rinner, Alpen-Adria-Universität Klagenfurt, AT

Smart vision systems that capture data in both private and public environments are now ubiquitous and have applications in security, disaster response, robotics, and smart environments, among others. Processing this data manually is an immensely tedious – and for some applications – an infeasible task, and an enhanced level of automation and self-awareness in the overall system is a key to overcome the design challenges. This special session addresses design aspects of smart vision systems realized at different levels: the image sensor, the camera node and the system level.

1400

The CAMEL Approach to Stacked Sensor Smart Cameras

Speaker: Marilyn Wolf, Georgia Institute of Technology, US

Authors: Saibal Mukhopadhyay¹, Marilyn Wolf¹ and Evan Gebhardt²

¹Georgia Institute of Technology, US; ²School of ECE, Georgia Institute of Technology, US

1418

A Design Tool for High Performance Image Processing on Multicore Platforms

Speaker: Shuvra Bhattacharyya, University of Maryland, College Park, MD, USA and Tampere University of Technology, Finland, US

Authors: Jiahao Wu¹, Timothy Blattner², Walid Keyrouz² and Shuvra S. Bhattacharyya¹

¹University of Maryland, US; ²National Institute of Standards and Technology, US

1436

Quasar, a High-level Programming Language and Development Environment for Designing Smart Vision Systems on Embedded Platforms

Speaker: Bart Goossens, Ghent University - imec, BE

Authors: Bart Goossens, Hiệp Luong, Jan Aelterman and Wilfried Philips, Ghent University, Dept. of Telecommunications and Information Processing, BE

1454

Concurrent focal-plane generation of compressed samples from time-encoded pixel values

Speaker: Ricardo Carmona-Galan, Instituto de Microelectronica de Sevilla (CSIC-Univ. de Sevilla), ES

Authors: Marco Trevisi¹, Héctor C Bandala², Jorge Fernández-Berni¹, Ricardo Carmona-Galán¹ and Ángel Rodríguez-Vázquez¹

¹Instituto de Microelectrónica de Sevilla (IMSE-CNM), CSIC-Universidad de Sevilla, ES; ²Dept. Electronics, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), MX

1512

Contactless Finger and Face Capturing on a Secure Handheld Embedded Device

Speaker: Axel Weissenfeld, AIT Austrian Institute of Technology GmbH, AT

Authors: Axel Weissenfeld and Bernhard Strobl

AIT Austrian Institute of Technology GmbH, AT

1530

Coffee Break in Exhibition Area

11.2

Timing and Power Driven Physical Design

Konf. 6 1400 - 1530

Chair: Miguel Silveira, INESC-ID/IST, PT**Co-Chair:** Patrick Groeneveld, Cadence Design Systems, US

The first two papers in this session present timing analysis algorithms to handle non-ideal physical conditions. In particular the first paper extends the involution model adding non-deterministic delay variations. The second paper presents a method for estimating the worst case delay based on the extreme value theory. The remaining two papers in this session deal with floorplanning and placement. One paper addresses 3D ICs for multiple supply voltages. The other shows a way to accelerate the analytical placement employing GPU cores.

1400

A Faithful Binary Circuit Model with Adversarial Noise

Speaker: Jürgen Maier, TU Wien, AT

Authors: Matthias Fuegger¹, Jürgen Maier², Robert Najvirt², Thomas Nowak³ and Ulrich Schmid²¹LSV, CNRS & ENS Paris-Saclay, FR; ²TU Wien, AT; ³Universite Paris Sud, FR

1430

EVT-based Worst Case Delay Estimation Under Process Variation

Speaker: Charalampos Antoniadis, University of Thessaly, GR

Authors: Charalampos Antoniadis, Dimitrios Garyfallou, Nestor Evmoropoulos and Georgios Stamoulis, University of Thessaly, GR

1500

Co-Synthesis of Floorplanning and Powerplanning in 3D ICs for Multiple Supply Voltage Designs

Speaker: Jih-Ying Yang, Department of Electrical Engineering, National Cheng Kung University, TW

Authors: Jai-Ming Lin, Chien-Yu Huang and Jih-Ying Yang, Department of Electrical Engineering, National Cheng Kung University, TW

1515

Accelerate Analytical Placement with GPU: A Generic Approach

Speaker: Martin D. F. Wong, University of Illinois Urbana-Champaign, US

Authors: Chun-Xun Lin and Martin Wong

University of Illinois at Urbana-Champaign, US

IPs

IP4-17, IP5-1, IP5-2, IP5-3

1530

Coffee Break in Exhibition Area

11.3

More than Moore Interconnects

Konf. 1 1400 - 1530

Chair: Sébastien Le Beux, Ecole Centrale de Lyon – University of Lyon, FR**Co-Chair:** Davide Zoni, Politecnico di Milano, IT

In this session, the application of emerging technologies such as 3D Integration and Silicon Photonics broadens the capabilities of chip-scale interconnects and on-chip resource allocation mechanisms. The first two papers apply 3D integration to the design of networks-on-chip by providing enhanced collective communication mechanisms and resiliency to soft errors, respectively. The third paper shows how to leverage the NoC to manage resource allocations in chip multiprocessors. The final paper applies silicon photonics to the design of chip-scale interconnection networks for high-performance computing systems.

1400

High Performance Collective Communication-Aware 3D Network-on-Chip Architectures

Speaker: Biresch Joardar, Washington State University, US

Authors: Biresch Joardar, Karthi Duraisamy and Partha Pande, Washington State University, US

- 1430 **A Soft-Error Resilient Route Computation Unit for 3D Networks-on-Chips**
Speaker: Alexandre Coelho, TIMA Laboratory, FR
Authors: Alexandre Coelho¹, Amir Charif², Nacer-Eddine Zergainoh¹, Juan Fraire¹ and Raoul Velazco¹
¹TIMA Laboratory, FR; ²TIMA, FR
- 1500 **SPA: Simple Pool Architecture for application resource allocation in many-core systems**
Speaker: Iraklis Anagnostopoulos, Southern Illinois University Carbondale, US
Authors: Jayasimha Sai Koduri and Iraklis Anagnostopoulos, Southern Illinois University Carbondale, US
- 1515 **RSON: an Inter/Intra-Chip Silicon Photonic Network for Rack-Scale Computing Systems**
Speaker: Peng Yang, Hong Kong University of Science and Technology, CN
Authors: Peng Yang¹, Zhengbin Pang², Zhifei Wang¹, Zhehui Wang¹, Min Xie², Xuanqi Chen¹, Luan H.K. Duong¹ and Jiang Xu¹
¹Hong Kong University of Science and Technology, HK
²National University of Defense Technology, CN
- IPs **IP5-4, IP5-5**
- 1530 Coffee Break in Exhibition Area

11.4

Evaluating and optimizing memory and timing across HW and SW boundaries

Konf. 2 1400 - 1530

Chair: Sara Vinco, Politecnico di Torino, IT
Co-Chair: Todd Austin, University of Michigan, US

The session presents new solutions to evaluate and optimize data location and application timing. The first paper presents a hybrid memory emulator to analyze the performance characteristics of non-volatile memories. The second paper proposes a tool and a library to synthesize distributed protocols on concurrent systems. The third paper presents an optimization framework to find the best data partitioning schemes for processing-in-memory architectures. Finally, the last paper uses loop acceleration to advance source level timing simulation.

- 1400 **HME: A Lightweight Emulator for Hybrid Memory**
Speaker: Zhuohui Duan, Huazhong University of Science and Technology, CN
Authors: Zhuohui Duan, Haikun Liu, Xiaofei Liao and Hai Jin, Huazhong University of Science and Technology, CN
- 1430 **VerC3: A Library for Explicit State Synthesis of Concurrent Systems**
Speaker: Marco Elver, University of Edinburgh, GB
Authors: Marco Elver, Christopher J. Banks, Paul Jackson and Vijay Nagarajan, University of Edinburgh, GB
- 1500 **Prometheus: Processing-in-memory Heterogeneous Architecture Design From a Multi-layer Network Theoretic Strategy**
Speaker: Yao Xiao, USC, US
Authors: Yao Xiao, Shahin Nazarian and Paul Bogdan, University of Southern California, US
- 1515 **Advancing Source-Level Timing Simulation using Loop Acceleration**
Speaker: Joscha Benz, University of Tuebingen, DE
Authors: Joscha Benz¹, Christoph Gerum¹ and Oliver Bringmann²
¹University of Tuebingen, DE; ²University of Tuebingen / FZI, DE
- IPs **IP5-13**
- 1530 Coffee Break in Exhibition Area

11.5

Microfluidic Devices and Inexact Computing

Konf. 3 1400 - 1530

Chair: Martin Trefzer, University of York, GB**Co-Chair:** Lukas Sekanina, University of Brno, CZ

The first two presentations cover applications for microfluidic devices. The first one considers sample preparation, i.e. how to efficiently prepare certain dilutions and mixtures of fluids with a given amount of storages. The second one considers programmable versions of these devices that allow for the realization of general purpose applications. The last two presentations introduce new circuit structures for computing technologies that rely on approximation and probabilities. More precisely, an adaptive approximated divider design and manipulating circuits for stochastic computing are presented.

1400 **Storage-Aware Sample Preparation Using Flow-Based Microfluidic Lab-on-Chip**

Speaker: Robert Wille, Institute for Integrated Circuits, Johannes Kepler University Linz, 4040 Linz, Austria, AT

Authors: Sukanta Bhattacharjee¹, Robert Wille², Juinn-Dar Huang³ and Bhargab Bhattacharya¹¹Indian Statistical Institute, IN; ²Johannes Kepler University Linz, AT; ³National Chiao Tung University, Hsinchu, TW1430 **Pump-Aware Flow Routing Algorithm for Programmable Microfluidic Devices**

Speaker: Tsung-Yi Ho, National Tsing Hua University, TW

Authors: Guan-Ru Lai¹, Chun-Yu Lin² and Tsung-Yi Ho²¹TSMC, TW; ²National Tsing Hua University, TW1500 **Adaptive Approximation in Arithmetic Circuits: A Low-Power Unsigned Divider Design**

Speaker: Honglan Jiang, University of Alberta, CA

Authors: Honglan Jiang¹, Leibo Liu², Fabrizio Lombardi³ and Jie Han¹¹University of Alberta, CA; ²Tsinghua University, CN; ³Northeastern University, US1515 **Correlation Manipulating Circuits for Stochastic Computing**

Speaker: Vincent Lee, University of Washington, US

Authors: Vincent T. Lee, Armin Alaghi and Luis Ceze, University of Washington, US

IPs **IP5-6, IP5-7**

1530 Coffee Break in Exhibition Area

11.6

Memory: new technologies and reliability-related issues

Konf. 4 1400 - 1530

Chair: Carles Hernandez, Barcelona Supercomputing Center (BSC), ES**Co-Chair:** Shahar Kvatinsky, Technion, IL

The session covers computation using emerging memory technologies, investigating techniques to protect against process variation and soft errors

1400 **XNOR-RRAM: A Scalable and Parallel Resistive Synaptic Architecture for Binary Neural Networks**

Speaker: Shimeng Yu, Arizona State University, CN

Authors: Xiaoyu Sun, Shihui Yin, Xiaochen Peng, Rui Liu, Jae-sun Seo and Shimeng Yu, Arizona State University, US

- 1430 **A Novel Fault Tolerant Cache Architecture Based on Orthogonal Latin Squares Theory**
 Speaker: Georgios Kerasidas, Think Silicon S.A., GR
 Authors: Filippos Filippou¹, Georgios Kerasidas², Michail Mavropoulos¹ and Dimitris Nikolos¹
¹University of Patras, GR; ²Think Silicon S.A./Technological Educational Institute of Western Greece, GR
- 1500 **Technology-Aware Logic Synthesis for ReRAM based In-Memory Computing**
 Speaker: Debjyoti Bhattacharjee, Nanyang Technological University, SG
 Authors: Debjyoti Bhattacharjee¹, Luca Amaru² and Anupam Chattopadhyay¹
¹Nanyang Technological University, SG; ²Synopsys, US
- 1515 **SMARTag: Error Correction in Cache Tag Array by Exploiting Address Locality**
 Speaker: Hamed Farbeh, School of Computer Science, Institute for Research in Fundamental Sciences (IPM), IR
 Authors: Seyedeh Golsana Ghaemi¹, Iman Ahmadpour¹, Mehdi Ardebili² and Hamed Farbeh³
¹Sharif University of Technology, IR; ²Tehran University, IR; ³School of Computer Science, Institute for Research in Fundamental Sciences (IPM), IR
- IPs **IP5-8, IP5-9, IP5-17**
- 1530 Coffee Break in Exhibition Area

11.7

Building Resistant Systems: From Temperature Awareness to Attack Resistance

Konf. 5 1400 - 1530

Chair: Marina Zapater, EPFL, CH**Co-Chair:** Georg Becker, ESMT Berlin, DE

This session explores new methods in building reliable and secure systems, especially in larger SoCs. Temperature-induced stress can impact the reliability of digital systems. Temperature fluctuations can also be exploited as side channels. This session first explores the two side of this coin by discussing a novel temperature-aware chiplet placing algorithm in 2.5D systems and by showing how transmission bandwidth encoded as a temperature signal can be maximized. Then, the rest of the session highlights advances in PUFs that are resistant against latest-generation attacks, and particularly integration of PUFs in larger systems.

- 1400 **Leveraging Thermally-Aware Chiplet Organization in 2.5D Systems to Reclaim Dark Silicon**
 Speaker: Yenai Ma, Boston University, US
 Authors: Furkan Eris¹, Ajay Joshi¹, Andrew B. Kahng², Yenai Ma¹, Saiful Mojumder¹ and Tiansheng Zhang¹
¹Boston University, US; ²UCSD, US
- 1430 **Ising-PUF: A Machine Learning Attack Resistant PUF Featuring Lattice Like Arrangement of Arbiter-PUFs**
 Speaker: Hiromitsu Awano, The University of Tokyo, JP
 Authors: Hiromitsu Awano¹ and Takashi Sato²
¹The University of Tokyo, JP; ²Kyoto University, JP
- 1500 **Efficient Helper Data Reduction in SRAM PUFs via Lossy Compression**
 Speaker: Ye Wang, University of Texas at Austin, US
 Authors: Ye Wang and Michael Orshansky, University of Texas at Austin, US
- 1515 **Improving the Efficiency of Thermal Covert Channels in Multi-/Many-core Systems**
 Speaker: Zijun Long, South China University of Technology, CN
 Authors: Zijun Long¹, Xiaohang Wang¹, Yingtao Jiang², Guofeng Cui¹, Yiming Zhao¹, Li Zhang¹ and Terrence Mark³

¹South China University of Technology, CN; ²University of Nevada, US;
³University of Southampton, UK, GB

IPs **IP5-10, IP5-11, IP5-15**
 1530 Coffee Break in Exhibition Area

11.8 A Powerful Framework for Functional Safety

Exhibition Theatre 1400 - 1530

Organiser: Astrid Ernst, Mentor, DE

In the program of the technical conference, on Thursday is the Special Day for "Autonomous Driving". In the Exhibition Theatre this will be complemented by a workshop on how to design chips and electronic systems fulfilling the functional safety requirements of devices used in the car. This a challenge which is absolutely key for the automotive industry - no autonomous driving without functional safety, no matter how cool the driving algorithms might be.

1400 **Introduction**
 Speaker: Dirk Hansen, Mentor, DE

As semiconductor value in a modern car expands, reliability and safety of electronics must improve dramatically. This will increase the test cycles, visibility and coverage to improve the safety and reliability. In this session, we will present technologies and methodologies allowing us to handle an explosion of test scenarios to verify electronics and algorithms of driverless cars. We will explain a mature Development Process and show how Requirement driven development provides proof that design was built and tested as intended.

1410 **IC Verification: Shift-Left the Path to ISO 26262 Compliance for Digital IC Development**
 Speaker: Dirk Hansen, Mentor, DE

1450 **DFT part: Test Solutions for the Automotive Market**
 Speaker: Ralph Sommer, Mentor, DE

1530 Coffee Break in Exhibition Area

IP5 Interactive Presentations

Conference Level, Foyer 1530 - 1600

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

IP5-1 **A Placement Algorithm for Superconducting Logic Circuits Based on Cell Grouping and Super-Cell Placement**

Speaker: Massoud Pedram, University of Southern California, US
 Authors: Soheil Nazar Shahsavani, Alireza Shafaei Bejestan and Massoud Pedram
 University of Southern California, US

IP5-2 **Abax: 2D/3D Legaliser Supporting Look-Ahead Legalisation and Blockage Strategies**

Speaker: Christos Sotiriou, University of Thessaly, GR
 Authors: Nikolaos Sketopoulos, Christos Sotiriou and Stavros Simoglou, Department of Electrical and Computer Engineering, University of Thessaly, GR

- IP5-3 LESAR: A Dynamic Line-End Spacing Aware Detailed Router**
 Speaker: Yih-Lang Li, Computer Science Department, NCTU, TH
 Authors: Ying-Chi Wei¹, Radhamañjari Samanta¹ and Yih-Lang Li²
¹NCTU CS department, TW; ²National Chiao-Tung University, TW
- IP5-4 Understanding Turn Models for Adaptive Routing: the Modular Approach**
 Speaker: Edoardo Fusella, Department of Electrical Engineering and Information Technologies, University of Naples Federico II, IT
 Authors: Edoardo Fusella and Alessandro Cilardo, University of Naples Federico II, IT
- IP5-5 Quater-Imaginary Base for Complex Number Arithmetic Circuits**
 Speaker: Souradip Sarkar, Nokia Bell Labs, BE
 Authors: Souradip Sarkar and Manil Dev Gomony
 Nokia Bell Labs, BE
- IP5-6 Fault-Tolerant Valve-Based Microfluidic Routing Fabric for Droplet Barcoding in Single-Cell Analysis**
 Speaker: Yasamin Moradi, Technical University of Munich (TUM), DE
 Authors: Yasamin Moradi¹, Mohamed Ibrahim², Krishnendu Chakraborty² and Ulf Schlichtmann¹
¹Technical University of Munich, DE; ²Duke University, US
- IP5-7 Optimizing Power-Accuracy trade-off in Approximate Adders**
 Speaker: Celia Dharmaraj, Indian Institute of Technology Madras, IN
 Authors: Celia Dharmaraj, Vinita Vasudevan and Nitin Chandrachoodan, Indian Institute of Technology Madras, IN
- IP5-8 Improving the Error Behavior of DRAM by Exploiting its Z-Channel Property**
 Speaker: Kira Kraft, University of Kaiserslautern, DE
 Authors: Kira Kraft¹, Matthias Jung², Chirag Sudarshan¹, Deepak M. Mathew¹, Christian Weis¹ and Norbert Wehn¹
¹University of Kaiserslautern, DE; ²Fraunhofer IESE, DE
- IP5-9 Architecture and Optimization of Associative Memories used for the Implementation of Logic Functions based on Nanoelectronic 1S1R Cells**
 Speaker: Arne Heittmann, RWTH-Aachen University, DE
 Authors: Arne Heittman and Tobias G. Noll, RWTH Aachen University, DE
- IP5-10 Accurate Prediction of Smartphones' Skin Temperature by Considering Exothermic Components**
 Speaker: Jihoon Park, Yonsei University, KR
 Authors: Jihoon Park and Hojung Cha, Dept. of Computer Science, Yonsei University, KR
- IP5-11 Trustworthy Proofs for Sensor Data using FPGA based Physically Unclonable Functions**
 Speaker: Urbi Chatterjee, Indian Institute of Technology Kharagpur, IN
 Authors: Urbi Chatterjee¹, Durga Prasad Sahoo², Debdeep Mukhopadhyay³ and Rajat Subhra Chakraborty⁴
¹Indian Institute of Technology Kharagpur, IN; ²Bosch India (RBEI/ETI), IN; ³Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur, IN; ⁴Assistant Professor, Computer Science and Engineering, IIT Kharagpur, IN
- IP5-12 Towards Fully Automated TLM-to-RTL Property Refinement**
 Speaker: Vladimir Herdt, University of Bremen, DE
 Authors: Vladimir Herdt¹, Hoang M. Le¹, Daniel Grosse² and Rolf Drechsler²
¹University of Bremen, DE; ²University of Bremen/DFKI GmbH, DE
- IP5-13 In-Memory Computing Using Paths-Based Logic and Heterogeneous Components**
 Speaker: Alvaro Velasquez, University of Central Florida, US
 Authors: Alvaro Velasquez and Sumit Kumar Jha, University of Central Florida, US

- IP5-14 **Non-Intrusive Testing Technique for Detection of Trojans in Asynchronous Circuits**
 Speaker: Rodrigo Possamai Bastos, TIMA Laboratory, CNRS/Grenoble INP/UJF, FR
 Authors: Leonel Acunha Guimarães, Thiago Ferreira de Paiva Leite, Rodrigo Possamai Bastos and Laurent Fesquet, TIMA - Grenoble Institute of Technology, FR
- IP5-15 **Towards Inter-Vendor Compatibility of True Random Number Generators for FPGAs**
 Speaker: Miloš Grujić, imec-COSIC, KU Leuven, BE
 Authors: Miloš Grujić, Bohan Yang, Vladimir Rozic and Ingrid Verbauwhede, imec-COSIC, KU Leuven, BE
- IP5-16 **Efficient Wear Leveling for Inodes of File Systems on Persistent Memories**
 Speaker: Xianzhang Chen, Chongqing University, CN
 Authors: Xianzhang Chen¹, Edwin Sha¹, Yuansong Zeng¹, Chaoshu Yang¹, Weiwen Jiang¹ and Qingfeng Zhuge²
¹Chongqing University, CN; ²East China Normal University, CN
- IP5-17 **Exploring Non-Volatile Main Memory Architectures for Handheld Devices**
 Speaker: Virendra Singh, Indian Institute of Technology Bombay, IN
 Authors: Sneha Ved and Manu Awasthi, Indian Institute of Technology Gandhinagar, IN

12.1

Special Day Session on Designing Autonomous Systems: Self-awareness for Autonomous Systems

Saal 2 1600 - 1730

Chair: Nikil Dutt, University of California at Irving, US

With increasing interest in the deployment of autonomous vehicles and robots, a critical open challenge is to empower these systems with self-awareness for achieving truly autonomous operation. Self-awareness principles hold the promise to manage effectively continuous change and evolution, application interference, environment dynamics and system uncertainty, thereby adhering to safety, availability, and security guarantees as needed. The goal of this special session is to make the audience appreciate the benefits of self-awareness for systems autonomy, highlight challenges for self-awareness using two application contexts (unmanned aerial systems and autonomous vehicles), and outline EDA and HW/SW challenges to support self-awareness for systems autonomy.

- 1600 **Self-Awareness and Behavior Assurance for Unmanned Aerial Vehicle (UAV) Systems**
 Speaker: Prakash Sarathy, Northrop Grumman, US
 Authors: Peter Lee¹ and Prakash Sarathy²
¹Corenova Technologies Inc., US; ²Northrop Grumman Corporation, US
- 1630 **Promises and Challenges in deploying Self-Awareness in Autonomous Vehicles**
 Author: Christoph Stiller, Karlsruhe Institute of Technology (KIT), DE
- 1700 **Design Methodologies for Enabling Self-awareness in Autonomous Systems**
 Speaker: Andreas Herkersdorf, Technical University Munich (TUM), DE
 Authors: Armin Sadighi¹, Bryan Donyanavard², Thawra Kadeed³, Kasra Moazzemi², Tiago Muck², Ahmed Nassar², Amir Rahmani², Thomas Wild¹, Nikil Dutt², Rolf Ernst³, Andreas Herkersdorf¹ and Fadi Kurdahi²
¹Technical University of Munich (TUM), DE; ²University of California at Irvine (UCI), US; ³TU Braunschweig, DE

12.2

Searching for corner cases, bugs and security vulnerabilities

Konf. 6 1600 - 1730

Chair: Daniel Grosse, University of Bremen / DFKI, DE
Co-Chair: Jaan Raik, Tallinn University of Technology, EE

This session presents innovative solutions to identify challenging situations in RTL designs. The first work presents a fully automated and scalable approach for concolic generation of direct test on RTL models. The second work uses historical debugging data to predict future bug locations. The last presentation automatically mines formal assertions to highlight security vulnerabilities on IP firmware.

1600 **Directed Test Generation using Concolic Testing on RTL models**

Speaker: Jonathan Cruz, University of Florida, US
Authors: Alif Ahmed, Farimah Farahmandi and Prabhat Mishra, University of Florida, US

1630 **Suspect Set Prediction in RTL Bug Hunting**

Speaker: Neil Veira, University of Toronto, CA
Authors: Neil Veira, Zissis Poulos and Andreas Veneris, University of Toronto, CA

1700 **Symbolic assertion mining for security validation**

Speaker: Alessandro Danese, University of Verona, IT
Authors: Alessandro Danese¹, Valeria Bertacco² and Graziano Pravadelli¹
¹University of Verona, IT; ²University of Michigan, US

12.3

Verification and Formal Synthesis

Konf. 1 1600 - 1730

Chair: Christoph Scholl, Albert-Ludwigs-Universität Freiburg, DE
Co-Chair: Gianpiero Cabodi, Politecnico di Torino, IT

This session explores formal design methodology for asynchronous pipelines, reasons about decomposing assume/guarantee contracts, links high-level models and RTL designs, and also improves arithmetic circuit verification.

1600 **Improving and Extending the Algebraic Approach for Verifying Gate-Level Multipliers**

Speaker: Armin Biere, Johannes Kepler Universität Linz, AT
Authors: Daniela Ritirc, Armin Biere and Manuel Kauers, Johannes Kepler University Linz, AT

1630 **Reconfigurable Asynchronous Pipelines: from Formal Models to Silicon**

Speaker: Danil Sokolov, Newcastle University, GB
Authors: Danil Sokolov, Alessandro de Gennaro and Andrey Mokhov, Newcastle University, GB

1700 **Automatic generation of hardware checkers from formal micro-architectural specifications**

Speaker: Alexander Fedotov, Eindhoven University of Technology, NL
Authors: Alexander Fedotov and Julien Schmaltz, Eindhoven University of Technology, NL

1715 **Specification Decomposition for Synthesis from Libraries of LTL Assume/Guarantee Contracts**

Speaker: Antonio Iannopollo, UC Berkeley, IT
Authors: Antonio Iannopollo, Stavros Tripakis and Alberto Sangiovanni Vincentelli
University of California, Berkeley, US

12.4 **Hardware-assisted Security**

Konf. 2 1600 - 1730

Chair: Ilia Polian, University of Stuttgart, DE**Co-Chair:** Nele Mentens, Katholieke Universiteit Leuven, BE

Security of today's system cannot be achieved by software techniques alone. This session presents hardware anchors which provide security at circuit and system level and allow its efficient verification.

1600 **Hardware-Assisted Rootkit Detection via On-line Statistical Fingerprinting of Process Execution**

Speaker: Yiorgos Makris, University of Texas at Dallas, US

Authors: Liwei Zhou and Yiorgos Makris
The University of Texas at Dallas, US1630 **Securing Conditional Branches in the Presence of Fault Attacks**

Speaker: Robert Schilling, Graz University of Technology, AT

Authors: Robert Schilling¹, Mario Werner² and Stefan Mangard²¹Graz University of Technology / Know Center GmbH, AT; ²Graz University of Technology, AT1700 **Towards Provably-Secure Performance Locking**

Speaker: Jeyavijayan Rajendran, Co-author, US

Authors: Monir Zaman¹, Abhrajit Sengupta², Danqing Liu³, Ozgur Sinanoglu⁴, Yiorgos Makris¹ and Jeyavijayan Rajendran³¹The University of Texas and Dallas, US; ²New York University, US³Texas A&M University, US; ⁴New York University Abu Dhabi, AE1715 **An Automated Configurable Trojan Insertion Framework for Dynamic Trust Benchmarks**

Speaker: Jonathan Cruz, University of Florida, US

Authors: Jonathan Cruz, Yuanwen Huang, Prabhat Mishra and Swarup Bhunia, University of Florida, US

12.5 **Lifetime Improvement for Persistent Memory**

Konf. 3 1600 - 1730

Chair: Arne Heittman, RWTH, DE**Co-Chair:** Chengmo Yang, University of Delaware, US

This session concentrates on methods for prolonging the lifetime of persistent main memory. Based on reference frequencies, papers in this session promote novel approaches to mitigate the adverse impact of writes from perspectives of cache replacement policy, frequent pattern compression, SLC/MLC hybrid organization, inode virtualization, as well as Android application specific address mapping.

1600 **Extending the Lifetime of NVMs with Compression**Speaker: Dan Feng, Huazhong University of Science and Technology, CN
Authors: Jie Xu¹, Dan Feng², Yu Hua², Wei Tong², Jingning Liu² and Chunyan Li²¹Wuhan National Lab for Optoelectronics, School of Computer Science and Technology Huazhong University of Science and Technology, Wuhan, China, CN; ²WNLO, CN1630 **Heterogeneous PCM array architecture for reliability, performance and lifetime enhancement**

Speaker: Taehyun Kwon, Sungkyunkwan University, KR

Authors: Taehyun Kwon, Muhammad Imran, Jung Min You and Joon-Sung Yang

Sungkyunkwan University, KR

- 1700 **An Efficient PCM-based Main Memory System via Exploiting Fine-grained Dirtiness of Cachelines**
 Speaker: Jie Xu, Huazhong University of Science and Technology, CN
 Authors: Jie Xu¹, Dan Feng², Yu Hua², Wei Tong², Jingning Liu², Chunyan Li² and Zheng Li²
¹Wuhan National Lab for Optoelectronics, School of Computer Science and Technology, Huazhong University of Science and Technology, Wuhan, China, CN; ²Wuhan National Lab for Optoelectronics, CN

- 1715 **DFPC: A Dynamic Frequent Pattern Compression Scheme in NVM-based Main Memory**
 Speaker: Yuncheng Guo, Huazhong University of Science and Technology, CN
 Authors: Yuncheng Guo, Yu Hua and Pengfei Zuo, Huazhong University of Science and Technology, CN

12.6

Special Session: Computing with Emerging Memories: How Good can it be?

Konf. 4 1600 - 1730

Chair: Pierre-Emmanuel Gaillardon, University of Utah, US
Co-Chair: Ian O'Connor, Ecole Centrale de Lyon, FR

With the recent evolutions of nanometer transistor technologies, power consumption emerged as the most critical limitation. Within advanced processors and computing architectures, the processor-memory communication accounts for a significant part of the energy requirement. While alternative design approaches, such as the use of optimized accelerators or advanced power management techniques are successfully employed in contemporary designs, the trend keeps worsening due to the ever-increasing gap between on-chip and off-chip memory data rates. This trend, known as Von Neumann bottleneck, not only limits the system performance, but also acts nowadays as a limiter of the energy scaling. The quest towards more energy-efficiency requires solutions that solve the Von Neumann bottleneck by tightly intertwining computing with memories. In this hot topic session, we intend to elaborate on in-memory computing by identifying and compare the latest computing models in light of conventional, e.g., SRAMs, and emerging memory technologies, e.g., RRAMs, STT-MRAMs. In-memory computing is considered here in the general sense of computing information locally within large data storage.

- 1600 **Practical Challenges in Delivering the Promises of Real Processing-in-Memory Machines**

Speaker: Nishil Talati, Technion - Israel Institute of Technology, IL
 Authors: Nishil Talati¹, Ameer Haj Ali², Rotem Ben Hur², Nimrod Wald², Ronny Ronen², Pierre-Emmanuel Gaillardon³ and Shahar Kvatinsky¹
¹Technion, IL; ²Technion - Israel Institute of Technology, IL; ³University of Utah, US

- 1630 **Smart Instruction Codes for In-Memory Computing Architectures Compatible with Standard SRAM Interfaces**

Speaker: Maha Kooli, CEA-Leti, FR
 Authors: Maha Kooli¹, Henri-Pierre CHARLES², Bastien Giraud¹ and Jean-Philippe Noel²
¹CEA/LETI, FR; ²CEA, FR

- 1700 **Memristive devices for Computation-in-Memory**

Speaker: Said Hamdioui, Delft University of Technology, NL
 Authors: Jintao Yu, HoangAnh DuNguyen, Mottaqiallah Taouil and Said Hamdioui
 Delft University of Technology, NL

- 1715 **Computing-in-memory with Spintronics**

Speaker: Shubham Jain, Purdue University, US
 Authors: Shubham Jain¹, Sachin Sapatnekar², Jian-Ping Wang², Kaushik Roy¹ and Anand Raghunathan¹
¹Purdue University, US; ²Department of Electrical and Computer Engineering, University of Minnesota, US

Optical/Photonic Interconnects for Computing Systems (OPTICS)

Konferenz 1 0830 - 1730

General Co-Chairs:

Jiang Xu, Hong Kong University of Science and Technology, HK
Sébastien Le Beux, Lyon Institute of Nanotechnology, FR
Gabriela Nicolescu, Ecole Polytechnique de Montréal, CA

Programme Committee Chair:

Mahdi Nikdast, Colorado State University, US

Invited Speakers:

Alan Mickelson, University of Colorado Boulder, US
Abderazek Ben Abdallah, The University of Aizu, JP
Bert Jan Offrein, IBM Zurich Research Lab., CH
Cédric Killian, IRISA, FR
Christophe Kopp, CEA, FR
Davide Bertozzi, University of Ferrara, IT
Jean-Francois Carpentier, STMicroelectronics, FR
José Abellán, Universidad Católica de Murcia (UCAM), ES
Jun Shiomi, Kyoto University, JP
Laurent Vivien, CNRS, FR
Nikos Pleros, Aristotle University of Thessaloniki, GR
Pieter Dumon, Luceda Photonics, US
Siming Chen, University College London, GB
Smruti R. Sarangi, Indian Institute of Technology Delhi, IN
Ulf Schlichtmann, Technische Universität München, DE
Yvain Thonnart, CEA, LETI, MINATEC, FR

The 4th International Workshop on Optical/Photonic Interconnects for Computing Systems(OPTICS Workshop)

Final Program: www.ece.ust.hk/~eexu/OPTICS.html

Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering alternative emerging technologies to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to solve the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices, which are compatible with CMOS fabrication process, are necessary to construct photonic interconnection networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects.

OPTICS workshop aims at discussing the most recent advances in photonic interconnects, covering topics from the device fabrication all the way up to the system-level design. The workshop is of interest to researchers working on silicon photonics and high-performance computing systems. It is comprised of invited talks of the highest caliber in addition to refereed poster presentations. Industry's and academia's views on the feasibility and recent progress of optical interconnects will be discussed during the workshop.

Topics to be discussed in the workshop include (but are not limited to) the following:

- Design Methodology, Modeling and Tools
- Architectures/Micro-Architectures
- Applications
- Silicon Photonic Devices
- Silicon Photonic Circuit

- 0830 Introduction to OPTICS Workshop**
Chair: **Jiang Xu**, Hong Kong University of Science and Technology, CN
- 0840 Morning Session I: Technological Advances**
Chair: **Sébastien Le Beux**, Lyon Institute of Nanotechnology, FR
- 0840 Keynote: Silicon photonics technology for advanced computing applications**
Speaker: Bert Jan Offrein, IBM Zurich Research Lab., CH
- 0910 Silicon photonics : towards heterogeneous and multi-layer integration for very high density circuits**
Speaker: Christophe Kopp, CEA, FR
- 0930 Monolithic III-V quantum-dot lasers for silicon photonics**
Speaker: Siming Chen, University College London, GB
- 0950 Towards low power electro-optics modulators**
Speaker: Laurent Vivien, CNRS, FR
- 1015 Coffee Break and Poster Presentations
- 1100 Morning Session II: Silicon Photonics in High Performance Computing**
Chair: **Sébastien Le Beux**, Lyon Institute of Nanotechnology, FR
Co-Chair: **Mahdi Nikdast**, Colorado State University, US
- 1100 The IIT Delhi photonics stack**
Speaker: Smruti R. Sarangi, Indian Institute of Technology Delhi, IN
- 1120 Electro-photonic NoC designs for kilocore systems**
Speaker: José Abellán, Universidad Católica de Murcia (UCAM), ES
- 1140 Fault-resilient photonic on-chip network for reliable high-throughput manycore systems**
Speaker: Ben Abdallah Abderazek, University of AIZU, JP
- 1200 Lunch Break and Poster Presentations
- 1300 Afternoon Session I: Silicon Photonics Design Automation**
Chair: **Jiang Xu**, Hong Kong University of Science and Technology, CN
- 1300 Keynote: Enabling photonic IC design**
Speaker: Pieter Dumon, Luceda Photonics, US
- 1330 EDA for ONOCs: Achievements, challenges, and opportunities**
Speaker: Ulf Schlichtmann, Technical University of Munich, DE
- 1350 Interfacing 3D-stacked electronic and optical NoCs with mixed CMOS-ECL bridges: a realistic preliminary assessment**
Speaker: Davide Bertozzi, University of Ferrara, IT
- 1410 Offline optimization of wavelength allocation and laser to deal with Energy-Performance tradeoffs in nanophotonic interconnects**
Speaker: Cédric Killian, IRISA, FR
- 1430 Coffee Break and Poster Presentation

- 1500** **Afternoon Session II: Design requirements, Challenges, and Applications**
Chair: Jiang Xu, Hong Kong University of Science and Technology, CN
- 1500** **Optical test chip and characterization challenges to address reliability and PAM4 topics**
 Speaker: Jean-Francois Carpentier, STMicroelectronics, FR
- 1520** **Thermally-tuned photonic links towards full electro-optical computing**
 Speaker: Yvain Thonnart, CEA, LETI, MINATEC, FR
- 1540** **Crosstalk in petabyte/s interconnection**
 Speaker: Alan Mickelson, University of Colorado Boulder, US
- 1600** **Photonics in computing: use “more than a link” for getting “more than Moore”**
 Speaker: Nikos Pleros, Aristotle University of Thessaloniki, GR
- 1620** **A light speed integrated optical parallel multiplier exploiting approximate binary logarithms with deterministic errors**
 Speaker: Jun Shiomi, Kyoto University, JP
- 1645** **Panel Discussion**
- 1725** **Concluding Remarks and Closing Session**
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR
Co-Chairs: Jiang Xu, Hong Kong University of Science and Technology, CN
Mahdi Nikdast, Colorado State University, US

Emerging Memory Solutions & Applications – Technology, Manufacturing, Architectures, Design, Automation and Test

Konferenz 2 0830 - 1700

General Chair: Said Hamdioui, Delft University of Technology, NL

Programme Co-Chairs:

Christian Weis, University of Kaiserslautern, DE

Bastien Giraud, CEA LETI, FR

Panel Chair: Ian O'Connor, Lyon Institute of Nanotechnology, FR

Publicity Chair: Matthias Jung, Fraunhofer IESE, DE

Publication Chair: Jean-Philippe Noel, CEA-Leti, FR

Steering Committee Member: Erik Jan Marinissen, IMEC, BE

Evolving memory technologies are triggering intense interdisciplinary activities; they have the potential to provide many benefits, such as energy efficiency, density, re-configurability, non-volatility, novel computational structures and approaches, massive parallelism, etc. And therefore overcome both technology and design limitations (e.g., leakage and memory wall) to answer the requirements of today's and future applications such as IoT, big-data, healthcare, etc. These characteristics may force to deeply revisit existing computing and storage paradigms.

This workshop (third edition) aims at providing a forum to discuss challenges, trends, solutions and applications of these rapidly evolving memory technologies by gathering researchers and engineers from academia and industry; it also aims at creating a unique network of competence and experts in all aspects of emerging memory solutions and technologies including manufacturing, architectures, design, automation and test.

Subjects of Interest

You are invited to participate and submit your contributions to the DATE 2018 Friday Workshop on Emerging Memory Solutions. The areas of interest include (but are not limited to) the following topics:

- Volatile embedded memories (DRAM, SRAM, CAM etc.),
- Advanced non-volatile memories (3D Flash, ReRAM, PCM, MRAM, STT-MRAM etc.),
- Memories based on emerging devices/technologies (TFET, nanowires, CNTs, etc.), 3D stacking of memories,
- Logic and arithmetic designs based on emerging memristive devices,
- Application-specific memory solutions such as near memory computing,
- Computing paradigms based on emerging memristive devices such as neuromorphic computing, computing-in-memory,
- Automation, compilers, programming models, etc. for the above designs and architectures.

Program and Panel

This one-day event will consist of two plenary keynotes, regular and poster presentations, and a panel session. The panel of the workshop will be about the topic "Deep Learning: what is the best memory to choose?". We are looking forward to a very lively discussion.

0840 **Opening**
Chair: Said Hamdioui, Delft University of Technology, NL

0840 **Welcome Address**
Speaker: Christian Weis, University of Kaiserslautern, DE

0845 **Keynote**
Chair: Christian Weis, University of Kaiserslautern, DE

0845 **Processing Data Where It Makes Sense in Modern Computing Systems: Enabling In-Memory Computation**
Speaker: Onur Mutlu, ETHZ, CH

0930 **Invited Talk about Emerging Neuromorphic Applications**
Chair: Pascal Vivet, CEA-Leti, FR

0930 **SpiNNaker2: Energy Efficient Neuromorphic Computing in 22nm FDSOI CMOS**
Speaker: Sebastian Höppner, Technische Universität Dresden, DE

1000 Coffee Break and Poster Session

Poster Session

Chair: Bastien Giraud, CEA-Leti, FR

1030 **Industry Talk**
Chair: Ian O'Connor, Ecole Centrale de Lyon, FR

1030 **Applications of phase-change memory in non-von Neumann computing**
Speaker: Manuel Le Gallo, IBM, CH

1100 **Panel about "Deep Learning: what is the best Memory to choose?"**
Moderator: Ian O'Connor, Ecole Centrale de Lyon, FR

Panelists: Elisa Vianello, CEA-Leti, FR
Andrew J. Walker, Schiltron Corp., US
Manuel Le Gallo, IBM, CH

The bridge between technology and applications is challenging. But that is exactly what this topic is about. Our discussion will take into consideration Deep Learning and AI (different flavors of neural networks) as used in current available Smartphones and HPC systems.

- How commodity technologies such as Flash, DRAM, 3D NAND are still suitable to support this demanding applications?
- How this fits together in the future?
- Can the technology and the design of memories help to improve?
- What about Emerging Memories, do they fit? What are the best candidates?

1200 Lunch Break

- 1300** **Keynote**
Chair: Said Hamdioui, Delft University of Technology, NL
- 1300** **Memory-Centric Architectures for Artificial Intelligence**
Speaker: Paul Franzon, NC State University, US
- 1330** **Special Session I on "In-Memory Computing"**
Chair: Said Hamdioui, Delft University of Technology, NL
- 1330** **Memristive Memory Processing Unit (mMPU) for Real Processing in Memory**
Speaker: Nishil Talati, TECHNION, IL
- 1350** **The Processing In Memory Revolution**
Speaker: Fabrice Devaux, UPMEM SAS, FR
- 1410** **Conceptual design of a RISC-V compatible processor core using ternary arithmetic unit with memristive MLC storage**
Speaker: Dietmar Fey, FAU, DE
- 1430** **Coffee Break and Poster Session**
Chair: Bastien Giraud, CEA-Leti, FR
- 1500** **Special Session II on "Emerging RRAMs and Alternatives"**
Chair: Bastien Giraud, CEA-Leti, FR
- 1500** **Challenges for Memristive Circuit Design**
Speaker: Anne Siemon, RWTH, DE
- 1520** **Reliability Modeling Framework for Emerging STT-MRAM**
Speaker: Rajendra Bishnoi, Karlsruhe Institute of Technology, DE
- 1540** **Compact modeling of resistive switching memories**
Speaker: Marc Bocquet, IM2NP, FR
- 1600** **Open Call Paper Session**
Chair: Matthias Jung, Fraunhofer IESE, DE
- 1600** **Quantifying the Performance Overhead of NVML**
Speaker: William Wang, ARM, GB
- 1615** **RRAM-based Automata Processor**
Speaker: Jintao Yu, Delft University of Technology, NL
- 1627** **Energy Efficient DRAM Cache with Unconventional Row Buffer Size**
Speaker: Nyunyi M. Tshibangu, NCSU, US
- 1639** **A 3-D Priority Address Encoder for 3-D Content Addressable Memories**
Speaker: Jin-Fu Li, NCU, TW
- 1651** **Asynchronous Ultra Wide Voltage Range Two-Port SRAM Circuit for Fast Wake-up IoT Platform**
Speaker: Réda Boumchedda, STMicroelectronics, FR

New Platforms for Future Cars: Current and Emerging Trends

Konferenz 3 0830 - 1730

Organisers:**Selma Saidi**, Hamburg University of Technology, DE**Muhammad Shafique**, Vienna University of Technology (TU Wien), AT

The automotive industry is rapidly moving towards the adoption of new hardware solutions, such as multi- and many-core processors, FPGAs and neural networks in order to comply with the increasingly number of ECUs and the high computational power required by future autonomous cars and advanced vision processing. Moreover, with the emerging trends in autonomous driving such as V2X communication and Internet of Cars, security is also arising as a serious concern for many automotive players. Therefore, new architecture solutions pose numerous challenges such as migrating legacy code, data fusion and processing of a multitude of sensors piling into autonomous cars, mapping affecting processing power demands in new systems architectures, employment of deep learning and other advanced AI techniques, the verification and validation of timing safety and providing secure interfaces to connect the cars to each other and to the outside world.

The goal of this workshop is to bring together researchers as well as practitioners from academia and industry to discuss and investigate cutting-edge methods and tools that will be driving technology innovation in the field of autonomous systems in order to devise highly efficient systems and systems-of-systems for future self-driving cars.

The program of the workshop includes invited talks from industry and academia experts. The workshop also involves short presentations based on selected submitted contributions in addition to a poster and demos session.

Invited Speakers:**Michael Kiehn**, Ibeo Automotive Systems GmbH, DE**Jens Benndorf**, Dream Chip Technologies, DE**Radu Grosu**, Vienna University of Technology, AT**Dirk Ziegenbein**, Robert Bosch GmbH, DE**Juergen Becker**, KIT - Karlsruher Institut für Technologie, DE**Wilfried Steiner**, TTEch Computertechnik AG, AT**Rolf Ernst**, Technische Universität Braunschweig, DE**Bernd Elend**, NXP Semiconductors, DE**Albrecht Mayer**, Infineon Technologies, DE**0815 Welcome and Opening****Organisers: Selma Saidi**, Hamburg University of Technology, DE**Muhammad Shafique**, Vienna University of Technology (TU Wien), AT**0830 Session 1 : From Advanced Data Sensing to Smart Processing in Autonomous Cars****0830 Processing needs for next generation 3D LIDAR****Speaker: Michael Kiehn**, Ibeo Automotive Systems GmbH, DE**0900 Automotive Multiprocessor ADAS Chip Design in 22nm FDSOI Technology****Speaker: Jens Benndorf**, Dream Chip Technologies, DE**0930 Parking with a Worms Brain****Speaker: Radu Grosu**, Vienna University of Technology, AT**1000 Coffee Break**

1030 Session 2 : Current Practices in Hardware and Software Automotive Design

1030 APP4MC: An Open Source Platform for Automotive Multi-Core Systems

Speaker: Dirk Ziegenbein, Robert Bosch GmbH, DE

1100 Reliable Heterogenous Multi-Core Platforms – Cyber-Physical Systems in Embed- ded: Automotive, Industry 4.x, Avionics –

Speaker: Juergen Becker, KIT – Karlsruher Institut für Technologie, DE

1130 Short Presentations

1130 Driving Against the Memory Wall: The Role of Memory for Autonomous Driving
Matthias Jung and Norbert Wehn, TU Kaiserslautern, DE

1140 Towards a Predictable Execution Model for Heterogeneous Systems-on-a-Chip
Andrea Marongiu, University of Bologna, IT

1150 Architecture Exploration for Safety-Critical Systems
Alexander Diewald, Simon Barner and Sebastian Voss, fortiss GmbH, DE

1200 Lunch Break

1300 Session 3 : Communication and Software Integration in Automotive Systems

1300 Highly-Integrated E/E Architectures by means of Vehicle-Wide Virtualization

Speaker: Wilfried Steiner, TTTech Computertechnik AG, AT

1330 System Level Logical Execution Time (LET)

Speaker: Rolf Ernst, TU Braunschweig, IDA, DE

1400 Short Presentations

1400 An Efficient and Streamlined Open Source Implementation of the LET Paradigm

Matthias Beckert and Rolf Ernst, TU Braunschweig, DE

1410 Big Data Analytics for Smart Cities: The H2o2o CLASS Project

Eduardo Quinones¹, Marko Bertogna², Erez Hadad³, Ana Juan Ferrer⁴, Luca Chiantore⁵ and Alfredo Reboa⁶

¹Barcelona Supercomputing Center, ES, ²Univ. of Modena, IT, ³IBM, IL,

⁴ATOS, ES, ⁵City of Modena, IT ⁶Maserati, IT

1420 WCET Analysis of Automotive Buses using WCC

Dominic Oehlert and Heiko Falk, TU Hamburg, DE

1430 Coffee Break

- 1500** **Session 4: Security as a Pillar for Automotive Functional Safety**
- 1500** **Secure CAN Communication for Increased Functional Safety - A New Approach Without the Challenges of Using Cryptography**
Speaker: Bernd Elend, NXP Semiconductors, DE
- 1530** **Cyber Security Paranoia: A Threat for Functional Safety?**
Speaker: Albrecht Mayer, Infineon Technologies, DE
- 1600** **Short Presentations**
- 1600** **Embedded GPUs in Future Automated Cars**
Joerg Fickenscher¹, Frank Hannig¹, Mohamed Essayed Bouzouraa² and Jürgen Teich¹
¹Friedrich-Alexander-Universität Erlangen-Nürnberg, DE ²AUDI AG, DE
- 1610** **Convolutional Neural Networks on Embedded Automotive Platforms: a Qualitative Comparison**
Paolo Burgio, Gianluca Brilli, Antonio Marra and Marko Bertogna, University of Modena, IT
- 1620** **Road Extraction and Object Recognition for Autonomous Cars**
Smail Niar¹, Mohamed Yazid Laachachi¹, Mohamed Ayoub Neggaz¹, Ihsen Alouani¹, Hasan Yantir², Abdelmalik Taleb-Ahmed¹, Fadi Kurdahi² and Ahmed Eltawil²
¹University of Valenciennes, FR, ²University of California, Irvine, US
- 1630** **Interactive Discussion: Posters and Demos**
- 1730** **Closing Session**

W04

Design Automation for Understanding Hardware Designs (DUHDE5)

Konferenz 4 0830 - 1700

Organiser: Jannis Stoppe, German Aerospace Center (DLR), DE

Understanding a hardware design is tough. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, lacks in understanding the details of a design are major obstacles for productivity. In software engineering topics like software maintenance, software understanding, reverse engineering are well established in the research community and partially tackled by tools. In the hardware area the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems, which mostly have yet to be solved by the hardware community.

The core audience are practitioners working in circuit design and to researchers interested in design automation as well as researchers and/or industry representatives from the fields of visualization and natural language processing.

It is not limited to the following topics in design understanding but includes:

- Design descriptions from the ESL down to RTL
- Extraction of high-level properties
- Localization of code implementing particular functionality
- Hardware design evolution : feature integration, feature interactions
- Innovative GUIs for designs
- Visualization of large scale designs
- Managing documentation of hardware designs
- Analysis of natural language documents and their connections to hardware implementations
- Scalable approaches to design understanding

Programme Committee:

Eli Arbel, IBM Haifa Research Lab, ISR

Lyes Benalycherif, ST Microelectronics, FR

Rüdiger Ehlers, University of Bremen, DE

Görschwin Fey, Hamburg University of Technology, DE

Christopher B. Harris, Auburn University, US

Ian Harris, UC Irvine, US

Oliver Keszöcze, University of Bremen, DE

Christian Krieg, Vienna University of Technology, AT

Tun Li, National University of Defense Technology, Changsha, CN

Matthieu Moy, Université Claude Bernard Lyon 1, FR

Christos Papachristou, Case Western Reserve University, US

Mathias Soeken, EPFL, CH

Georg Weissenbacher, Vienna University of Technology, AT

Francis Wolff, Case Western Reserve University, US

0830 Design Understanding for Risk Reduction

0830 Design Risk Analysis Based on Version Control Data

Author: Raviv Gal, IBM Haifa, IL

0930 A Test Register Assignment Method to Reduce the Number of Test Patterns Using Controller Augmentation

Authors: Syun Takeda¹, Toshinori Hosokawa², Hiroshi Yamazaki² and Masayoshi Yoshimura³

¹Graduate School of Industrial Technology, Nihon University, JP; ²College of Industrial Technology, Nihon University, JP; ³Faculty of Computer Science and Engineering, Kyoto Sangyo University, JP

0945 A Secure Design Method to Detect for Trojan Circuit inserted in Manufacturing Process

Authors: Yoshinobu Okuda¹ and Masayoshi Yoshimura²

¹Division of Frontier Infomatics, Kyoto Sangyo University, JP; ²Faculty of Computer Science and Engineering, Kyoto Sangyo University, JP

- 1030** **Turning Data into Knowledge: Tools and Applications I**
- 1030 **SymbiYosys: Investigating and Verifying Hardware Designs with Formal Open Source Tools**
Speaker: Clifford Wolf, TU Wien, AT
- 1130 **Modeling Heterogeneous Embedded Systems with TTool**
Author: Daniela Genius, Sorbonne Universités, UPMC Paris 06, LIP6, CNRS UMR 7606, FR
- 1300** **Turning Data into Knowledge: Tools and Applications II**
- 1300 **UMLAUT: Synthesis of Natural Language from Constrained UML Models**
Authors: Martin Ring¹, Jannis Stoppe² and Rolf Drechsler³
¹Cyber-Physical Systems, DFKI GmbH, DE; ²German Aerospace Center (DLR), Institute for the Protection of Maritime Infrastructures, DE; ³University of Bremen/DFKI GmbH, DE
- 1330 **Subtree Identification for Generating Assertions from Natural Language Descriptions**
Author: Ian Harris, University of California Irvine, US
- 1400 **Time-stamps for Hardware Simulation Models Accurate Time-back Annotation**
Authors: Rehab Massoud¹, Jannis Stoppe² and Rolf Drechsler³
¹Group of Computer Architecture, University of Bremen, DE; ²German Aerospace Center (DLR), Institute for the Protection of Maritime Infrastructures, DE; ³University of Bremen/DFKI GmbH, DE
- 1500** **Current and Future Techniques**
- 1500 **Unconventional Computing - What, Why and How**
Speaker: Jan Madsen, Technical University of Denmark, DK
- 1600 **PGSL: Identifying Functional Primitives in Hardware Description Language (HDL) Specifications**
Authors: Christian Krieg¹, Martin Mosbeck², Clifford Wolf² and Axel Jantsch²
¹Institute of Computer Technology, Vienna University of Technology, AT; ²Technische Universität Wien, AT
- 1630 **Execution Environment for Dynamic Software Runtime Examination**
Authors: Kenneth Schmitz¹, Oliver Keszöcze¹, Jannis Stoppe² and Rolf Drechsler³
¹University of Bremen, DE; ²German Aerospace Center (DLR), Institute for the Protection of Maritime Infrastructures, DE; ³University of Bremen/DFKI GmbH, DE

W05

Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE 2018)

Konferenz 5 0830 - 1700

Organisers:

Giorgio Di Natale, LIRMM, FR
Francesco Regazzoni, AlaRI, CH

Programme Committee Chairs:

Nele Mentens, KU Leuven, BE
Lejla Batina, Radboud University Nijmegen, NL

Programme Committee Members:

Bernd Becker, University of Freiburg, DE
Bossuet Lilian, University of St. Etienne, FR
Ricardo Chaves, Instituto de Engenharia de Sistemas e Computadores, PT
Viktor Fischer, Hubert Curien Laboratory, FR
Marie-Lise Flottes, LIRMM, FR
Said Hamdioui, Delft University of Technology, NL
Paris Kitsos, Hellenic Open University, GR
Martin Novotny, CVUT, CZ
Iliia Polian, University of Passau, DE
Bruno Rouzeyre, University Montpellier, FR
Johanna Sepulveda, TU Munich, DE
Nicolas Sklavos, University of Patras, GR

Hardware security is becoming increasingly important for many embedded systems applications, ranging from small RFID tags to satellites orbiting the earth. The number of secure applications, such as public services, communication, control and healthcare, keeps on growing. Hardware devices that implement cryptography functions have become the Achilles' heel of these systems.

The TRUDEVICE Workshop will provide an environment for researchers from academic and industrial domains who want to discuss recent findings, theories and on-going work on all aspects of hardware security including design, manufacturing, testing, reliability, validation and utilization.

The topics of the workshop include:

- Manufacturing Test of Secure Devices
- Trustworthy Manufacturing of Secure Devices
- PUFs and TRNGs
- Hardware Trojans in IPs and ICs
- Reconfigurable Devices for Security
- Fault Attack Injection, Detection and Protection
- Validation and Evaluation Methodologies for Physical Security
- Side Channel Attacks and Countermeasures

0830 **Session 1: Physical attacks**

0830 **Keynote 1**

0930 **Automatic Application of Side Channel Countermeasures: History and Perspectives**
Speaker: Francesco Regazzoni, AlaRI, CH

1000 Poster Session 1 + Coffee Break

1000 **Dummy rounds side-channel attack protection of round-based encryption algorithms**

Authors: Stanislav Jerabek¹, Jan Schmidt¹ and Martin Novotny²
¹Czech Technical University in Prague, CZ; ²CVUT, CZ

1000 **A New Metric for the Side-Channel Vulnerability Evaluation?**

Authors: Jan Bělohoubek, Petr Fiser and Jan Schmidt, Czech Technical University in Prague, CZ

1000 **Influence of Fault-Tolerance Techniques on Power-Analysis Resistance of AES implemented in FPGA**

Authors: Vojtěch Miškovský¹, Hana Kubatova¹ and Martin Novotny²
¹Czech Technical University in Prague, CZ; ²CVUT, CZ

1030 Session 2: Active attacks and systems integrity

1030 **A Hybrid Approach for Ensuring the Security of Hardware Control Systems**

Authors: Naceur Maha and Ulrich Kuehne, Télécom ParisTech, FR

1100 **On Security Metrics for Evaluating Fault-injection Countermeasures**

Authors: Maël Gay¹, Batya Karp², Osnat Keren² and Ilia Polian³
¹University of Passau, DE; ²Bar Ilan University, IL; ³University of Stuttgart, DE

1130 **SCA & Glitch Rogue: An Accurate Side Channel Analysis and Glitch Attack Evaluation Platform for Embedded Systems**

Authors: Athanasios Papadimitriou and David Hely
 Univ. Grenoble Alpes, FR

1145 **Nonlinear Codes for Control Flow Checking**

Authors: Giorgio Di Natale¹ and Osnat Keren²
¹LIRMM, FR; ²Bar Ilan University, IL

1200 Lunch Break

1300 Session 3: Design and test of secure hardware

1300 **Keynote 2**

1400 **Does stream cipher-based scan chains encryption really prevent scan attacks?**

Authors: Mathieu Da Silva, Marie-Lise Flottes, Giorgio Di Natale and Bruno Rouzeyre, LIRMM, FR

1430 Poster Session 2 + Coffee Break

1430 Dynamic reconfiguration used for side channel attacks protection of various encryption algorithms

Authors: Jan Brejnik¹, Stanislav Jerabek¹ and Martin Novotny²
¹Czech Technical University in Prague, CZ; ²CVUT, CZ

1430 Xilinx 7-Series FPGA Based Evaluation Platform for Physically Unclonable Function

Author: Matej Bartik, Czech Technical University in Prague, CZ

1430 Design and Implementation of a Security Processor for Satellite Communication Systems

Authors: Stavroula Zouzoula¹, Nicolas Sklavos² and Apostolos Fournaris¹
¹University of Patras, GR; ²University of Patra, GR

1500 Session 4: Hardware circuit security

1500 Using Convolutional Codes for Key Extraction in SRAM Physical Unclonable Functions

Authors: Sven Mueelich, Sven Puchinger and Martin Bossert, Ulm University, DE

1530 Towards Inter-Vendor Compatibility of TRNGs for FPGAs

Authors: Milos Grujic¹, Bohan Yang², Vladimir Rozič³ and Ingrid Verbauwhede⁴
¹Katholieke Universiteit Leuven, BE; ²ESAT/COSIC, BE; ³K.U.Leuven, BE; ⁴KU Leuven and UCLA, BE

1600 Two Methods of the Clock Jitter Measurement Aimed at Embedded TRNG testing

Authors: Oto Petura¹, Marek Laban², Elie Noumon Allini³ and Viktor Fischer⁴

¹Hubert Curien Laboratory, Jean Monnet University, FR; ²Technical University of Kosice, SK; ³Jean Monnet University Saint-Etienne, FR; ⁴Laboratoire Hubert Curien, FR

1615 Random Bit Generation Based on The Association of Serial CBRAM Devices

Authors: Daniel Arumi, Salvador Manich and Rosa Rodriguez, Universitat Politècnica de Catalunya – BarcelonaTech, ES

1630 Hardware Trojan Detection and Obfuscation based on Approximate Circuits

Authors: Honorio Martin¹, Giorgio Di Natale², Sophie Dupuis² and Luis Entrena¹

¹University Carlos III de Madrid, ES; ²LIRMM, FR

1645 Using different LUT paths to increase area efficiency of RO-PUFs on Altera FPGAs

Authors: Linus Feiten, Karsten Scheibler, Bernd Becker and Matthias Sauer, Universität Freiburg, DE

Embedded Software for Industrial IoTs (ESIIT 2018)

Konferenz 6 0830 - 1700

Organisers: **Oliver Bringmann**, University of Tuebingen / FZI, DE
Wolfgang Ecker, Infineon Technologies, DE
Wolfgang Müller, Universität Paderborn, DE
Daniel Müller-Gritschneider, Technische Universität München, DE
 Motivation and Objectives

The Internet-of-things (IoT) is emerging as the backbone for industrial automation. The tremendous impact of IoT to industrial applications is a key reason for IoT research and developments to grow dramatically in importance and economic impact for the next decade. At the edge of the IoT, ultra-thin devices with extremely small software memory footprints need to be cheap and capable to run with extremely small amounts of energy support over a very long lifetime. At the same time, IoT software must provide smart functions including real-time computing capabilities, connectivity, security, safety, and remote update mechanisms. These constraints put a high pressure on IoT software development based on the specific properties of IoT devices.

The ESIIT 2018 joint academic/industry workshop will focus on software development and maintenance of IoT devices addressing the very limited resources and power dissipation of IoT edge nodes in the context of a very long life cycle in an operational IoT network. This covers issues like software synthesis, configurability, safety, security, upgrades, fault recovery, maintenance as well as constraints and opportunities from newly emerging IoT hardware platforms. The workshop intends to provide an open platform for exchange and communication on new directions and requirements to academia and industry.

Proceedings

Proceedings will be published shortly before the workshop.

0845 **Opening****0900** **Keynote Address: Rethinking Firmware Design**
Speaker: Wolfgang Ecker, Infineon Technologies, DE**0930** **Invited Talk: Connected Sensors as Sense Organs of the IIoT**
Speaker: Alexander Buhmann, Robert Bosch, DE**1000** **Wo6.4 Break: Refreshments & Poster Discussions (Session I)****1030** **Invited Talk: Ultra Low Power Solutions for IoT Devices**
Speaker: Lauri Koskinen, Minima Processor Ltd., FI**1100** **Session I: Applications**
1100 **Towards Context-Dependent Robot Platform for Industrial Automation**
H.Watanabe¹, T.Ohkawa³, M.Sato¹, N.Ogura², M.Imamura¹
¹U Tokai, ²Tokyo City U, ³Utsunomiya U, JP**1115** **Virtual Prototype Based Analysis Framework in Model-Driven Development: A Use Case Study**
F. Haxel¹, L. Hielscher¹, S. Reiter¹, A. Viehl¹, O. Bringmann^{1,2}, W. Rosenstiel^{1,2}
¹FZI, DE, ²U Tübingen, DE

- 1130 **Distributed Visual SLAM Processing in Robot-Cloud Cooperative System**
T. Ohkawa, A. Soya, Y. Sugata, T. Matsumoto, K. Ootsu, T. Yokota
Utsunomiya U, JP
- 1145 **Gesture Recognition for Embedded Interactions in Industrial Automation Applications**
J.-P. Wolff, Ch. Haubelt (U Rostock, DE)
- 1200 Break: Lunch & Poster Discussions (Session I & II)
- 1300 **Invited Talk: Bridging the Gap between Hardware Description Languages and IP-XACT**
Speakers: Esko Pekkarinen, Tampere University of Technology, FI
Timo Hämäläinen, Tampere University of Technology, FI
- 1330 **Session II: Model-Driven Design and HW& SW Generation**
- 1330 **The Third Major Revolution in Embedded Development**
P. Lieber, R. Bretz (SparxServices, AT)
- 1345 **A Structured Approach for Generating Embedded Software**
D. Keerthikumara,^{1,2} W. Ecker^{2,3}, S. Lorenzo^{2,4}, W. Michael² (1U Kaiserslautern, DE, 2Infineon Technologies AG, DE, 3TU Munich, DE, 4U Linz, AT)
- 1400 **A Model for the Generation of Firmware and HW/SW Interfaces**
M. Dittrich, R. Stahl, D. Müller-Gritschneider, U. Schlichtmann (TU Munich)
- 1415 **Automatic Generation of Sensor Hardware by a Declarative Distributed Stream Processing System**
S. Coe, A. Mokhov, P. Watson (U Newcastle, UK)
- 1430 Break: Refreshments & Poster Discussions (Session II & III)
- 1500 **Session III: Optimization & Analysis**
- 1500 **Model-Driven Analysis and Design of IoT Systems**
E. Villar (U Cantabria, ES)
- 1515 **Modeling and Generating Timing-Predictable Firmware for IoT Nodes Using Standard C++**
J.-J. Benz, O. Bringmann (U Tübingen, DE)
- 1530 **Design-Time Optimization Techniques for Low-Power Embedded Memory Subsystems**
M. Strobel, M. Radetzki (U Stuttgart, DE)
- 1545 **ESL Black Box Power Estimation: Automatic Calibration for IEEE UPF 3.0 Power Models**
G. Onnebrink¹, F. Walbroel¹, R. Leupers¹, S. Schürmans², X. Chen³
(¹RWTH Aachen, DE, ²Silexica GmbH, DE, ³Huawei Technologies Co, CN)
- 1600 **Evaluation of Power State Cross Coverage in Firmware-Based Power Management**
V. Herdt¹, H.M. Le¹, D. Große^{1,2}, R. Drechsler^{1,2} (1U Bremen, 2DFKI GmbH, DE)
- 1615 **HW/SW Co-Equivalence Checking for Firmware Optimization**
M. Schwarz, D. Stoffel, W. Kunz (U Kaiserslautern, DE)
- 1630 **Break: Poster Discussions (Session III)**
- 1645 **Plenary Discussion & Closing**

In addition to the conference programme there will be 6 Exhibition Workshops as part of the exhibition with technical presentations on the state-of-the-art in our industry. The theatre is located in the centre of the exhibition area on the Terrace Level, close to the rooms of the technical conference.

The Exhibition Theatre sessions are open to conference delegates as well as to exhibition visitors.

Enabling ICT Innovations for European SMEs (2.8)

Projects of the EC's Smart Anything Everywhere Initiative will demonstrate by use of concrete examples how technology transfer can be initiated and implemented in practice and how to overcome the associated pitfalls and use the innovation opportunities.

Components for Secure IoT Systems (4.8)

Leading microelectronics suppliers present their newest solutions for designing and securing the IoT systems of the upcoming digital age. By elaborating on their technical approaches and design examples, they will provide attendees with valuable advice for the challenges in their own job.

Innovative Products for Autonomous Driving (3.8, 6.8)

Market leaders from the semiconductor and microelectronics industry present their solutions and visions for automotive applications including autonomous driving. By elaborating on their technical approaches and the experience made during the design and in the field, they will provide attendees with valuable advice for the challenges in their own job.

22FDX – the superior technology for IoT, RF, Automotive and Mobility (7.8, 8.8)

At the Special Day "Future and Emerging Technologies" this workshop is focussing on one of the hottest technologies used today in the industry, 22FDX. It will provide lots of information on how to design with these technologies, including best practice of a bunch of designs done recently.

An Industry Approach to FPGA and SOC System Development and Verification (10.8)

This tutorial-like workshop will discuss a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows, functional verification is used throughout the design process.

Functional Safety – Indispensable for Autonomous Driving (11.8)

At the Special Day "Autonomous Driving" this workshop is focussing on how to design chips and electronic systems fulfilling the functional safety requirements of devices used in the car. A challenge absolutely key also for autonomous driving.

2.8

Enabling ICT Innovations for European SMEs

Tuesday 1130 - 1300

→ See Page 45

3.8

Innovative Products for Autonomous Driving (part 1)

Tuesday 1430 - 1600

→ See Page 50

4.8

Components for Secure IoT Systems

Tuesday 1700 - 1830

→ See Page 57

6.8

Innovative Products for Autonomous Driving (part 2)

Wednesday 1100 - 1230

→ See Page 67

7.8

22FDX – the superior technology for IoT, RF, Automotive and Mobility: Advanced Design Methodologies for Ultra-low Power Solutions

Wednesday 1430 - 1600

→ See Page 73

8.8

22FDX - the superior technology for IoT, RF, Automotive and Mobility: Best-in Class RF, 5G and mmWave designs

Wednesday 1700 - 1830

→ See Page 80

10.8

An Industry Approach to FPGA and SOC System Development and Verification

Thursday 1100 - 1230

→ See Page 92

11.8

A Powerful Framework for Functional Safety

Thursday 1400 - 1530

→ See Page 98

University Booth at DATE 2018

The University Booth is organised during DATE and will be located in the exhibition area. All demonstrations will take place from Tuesday, March 20 to Thursday, March 22, 2018 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 34 demonstrations from 14 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Future and Emerging Technologies Prototypes
- Autonomous Systems Prototypes

The University Booth at DATE 2018 invites you to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information is available online at <https://www.date-conference.com/exhibition/u-booth>. The University Booth programme is included in the conference booklet and available online at <https://www.date-conference.com/exhibition/ub-programme>. The following demonstrators will be presented at the University Booth.

ABSYNTH: A COMPREHENSIVE APPROACH TO FRONT TO BACK ANALOG BLOCK DESIGN AUTOMATION

Authors: Abhaya Chandra Kammara S.¹, Sidney Pontes Filho² and Andreas König²

¹ISE, TU Kaiserslautern, DE; ²TU Kaiserslautern, DE

Timeslots:

- **UB01.5** (Tuesday, March 20, 2018 1030 - 1230)
- **UB02.5** (Tuesday, March 20, 2018 1230 - 1500)
- **UB09.9** (Thursday, March 22, 2018 1000 - 1200)
- **UB10.9** (Thursday, March 22, 2018 1200 - 1430)
- **UB11.9** (Thursday, March 22, 2018 1430 - 1630)

Abstract: ABSYNTH was first presented in CEBIT 2014 where complete, practical circuit sizing approaches have been shown using meta-heuristics on trusted simulators. This tool was then proven by its use in design of several cells in a research project. Here, we present the extension to our nested optimization approach that creates a symmetric and well matched layout in every step for every instance in the population of the swarm, that is extracted in our flow to provide feedback to the cost function impacting on the population update for more viable and robust circuits. The layout optimization presented in this DEMO works with Cadence Layout design tools. Our initial focus is, motivated by Industry 4.0, IoT, on cells for signal conditioning electronics with reconfigurability and Self-X features. [1] Abhaya C. Kammara, L.Palanichamy, and A. König, "Multi-Objective optimization and visualization for analog automation", Complex. Intell. Syst, Springer, DOI 10.1007/s40747-016-0027-3, 2016

ADVANCED SIMULATION OF QUANTUM COMPUTATIONS

Authors: Zulehner Alwin and Robert Wille, Johannes Kepler University Linz, AT

Timeslots:

- **UB01.3** (Tuesday, March 20, 2018 1030 - 1230)
- **UB06.3** (Wednesday, March 21, 2018 1200 - 1400)
- **UB10.3** (Thursday, March 22, 2018 1200 - 1430)

Abstract: Quantum computation is a promising emerging technology which allows for substantial speed-ups compared to classical computation. Since physical realizations of quantum computers are in their infancy, most research in this domain still relies on simulations on classical machines. This causes an exponential overhead which current simulators try to tackle with straight forward array-based representations and massive hardware power. There also exist solutions based on decision diagrams (graph-based approaches) that try to tackle the complexity by exploiting redundancies in quantum states and operations. However, they did not get established since they yield speedups only for certain benchmarks. Here, we demonstrate a new graph-based simulation approach which clearly outperforms state-of-the-art simulators. By this, users can efficiently execute quantum algorithms even if the respective quantum computers are not broadly available yet.

ARCHON: AN ARCHITECTURE-OPEN RESOURCE-DRIVEN CROSS-LAYER MODELLING FRAMEWORK

Authors: Fei Xia¹, Ashur Rafiev¹, Mohammed Al-Hayanni², Alexei Iliasov¹, Rishad Shafik¹, Alexander Romanovsky³ and Alex Yakovlev⁴
¹Newcastle University, UK; ²Newcastle University, UK and University of Technology and HCED, IQ

Timeslots:

- **UB01.1** (Tuesday, March 20, 2018 1030 - 1230)
- **UB02.1** (Tuesday, March 20, 2018 1230 - 1500)
- **UB10.1** (Thursday, March 22, 2018 1200 - 1430)
- **UB11.1** (Thursday, March 22, 2018 1430 - 1630)

Abstract: This demonstration showcases a modelling method for large complex computing systems focusing on many-core types and concentrating on the crosslayer aspects. The resource-driven models aim to help system designers reason about, analyse, and ultimately design such systems across all conventional computing and communication layers, from application, operating system, down to the finest hardware details. The framework and tool support the notion of selective abstraction and are suitable for studying such non-functional properties such as performance, reliability and energy consumption.

CCF: A CGRA COMPILATION FRAMEWORK

Authors: Shail Dave and Aviral Shrivastava, Arizona State University, US

Timeslots:

- **UB05.1** (Wednesday, March 21, 2018 1000 - 1200)
- **UB09.1** (Thursday, March 22, 2018 1000 - 1200)

Abstract: Coarse-grained reconfigurable array (CGRA) can efficiently accelerate even non-parallel loops. Although scores of techniques have been developed in the past decade to map loops on CGRA PEs, several challenges in enabling acceleration of general-purpose applications on CGRAs remained unresolved, in particular, the automatic code generation for the CGRA accelerator coupled with modern processor cores. In

this demonstration, we showcase CCF – CGRA compiler framework. CCF is implemented in LLVM 4.0 and includes a set of transformation and analysis passes. We show that given performance-critical loops annotated in embedded applications, how CCF extracts the loop, constructs the data dependency graph (DDG), maps it onto CGRA architecture, off-loads necessary configuration instructions for CGRA PEs, and automatically communicates data between the CPU and CGRA.

CJTAG: CONCURRENT IJTAG DEMONSTRATOR

Author: Krenz-Baath René, Hamm-Lippstadt University of Applied Sciences, DE

Timeslots:

- **UB01.9** (Tuesday, March 20, 2018 1030 - 1230)
- **UB03.9** (Tuesday, March 20, 2018 1500 - 1730)
- **UB05.9** (Wednesday, March 21, 2018 1000 - 1200)
- **UB07.9** (Wednesday, March 21, 2018 1400 - 1600)

Abstract: The flexibility of on-chip instrument access enabled by IEEE 1687 (IJTAG) has shown tremendous improvements in modern industrial designs. Due to a constantly increasing spektrum of tasks performed through 1687 networks such as performing test operations during production test, on-line test operations as well as operating health monitors the test requirements in modern designs increase dramatically with respect to test performance, responsiveness and low power. These requirements have a major impact on the design of such test infrastructures. In complex designs with large test infrastructures it might be challenging to comply with the large spectrum of requirements. Concurrent IJTAG is novel partitioning concept to a reconfigurable test infrastructure in order to enable an independent operation of different sections of the test infrastructure. The proposed demonstrator shows the first FPGA-based implementation of concurrent IJTAG test infrastructures.

CLAVA-MARGOT: CLAVA + MARGOT = C/ C++ TO C/C++ COMPILER AND RUNTIME AUTOTUNING FRAMEWORK

Authors: João Bispo¹, Davide Gadioli², Pedro Pinto¹, Emanuele Vitali², Hamid Arabnejad¹, Gianluca Palermo², Cristina Silvano², Jorge G. Barbosa¹ and João M. P. Cardoso¹

¹Porto University, PT; ²Politecnico di Milano (POLIMI), IT

Timeslots:

- **UB02.10** (Tuesday, March 20, 2018 1230 - 1500)
- **UB03.10** (Tuesday, March 20, 2018 1500 - 1730)
- **UB07.2** (Wednesday, March 21, 2018 1400 - 1600)

Abstract: Current computing platforms consist of heterogeneous architectures. To efficiently target those platforms, compilers can be extended with code transformations and insertion of code to interface to runtime autotuning schemes, which tune application parameters according to: the actual execution, target architecture, and workload. We present an approach consisting of a C/C++ source-to-source compiler (Clava) and an autotuner (mARGOT). They are part of the toolflow of the FET-HPC ANTAREX project and allow parallelization, multiversioning and code transformations in the context of runtime autotuning. mARGOT is an autotuner that allows application adaptation to changing conditions and goals. Clava is a source-to-source compiler to transform C/C++ programs, including code instrumentation and integration with components such as mARGOT. We will demonstrate how to use Clava to integrate the mARGOT autotuner in an example application, and several mARGOT functionalities exposed through a Clava API.

USING FORMAL METHODS FOR AUTOMATIC PLATFORM-INDEPENDENT CODE GENERATION OF RUN-TIME MANAGEMENT

Authors: Mohammadsadegh Dalvandi, Michael Butler and Asieh Salehi Fathabadi, University of Southampton, UK

Timeslots:

- **UB10.7** (Thursday, March 22, 2018 1200 - 1430)
- **UB11.7** (Thursday, March 22, 2018 1430 - 1630)

Abstract: Run-Time Management (RTM) systems are used in embedded systems to dynamically adapt hardware performance to minimise energy consumption. In this demonstration, we present a framework for automatic generation of RTM implementations from platform-independent formal models. The methodology in designing the RTM systems uses a high-level mathematical language, Event-B, which can describe systems at different abstraction levels. A code generation tool is used to translate platform-independent Event-B RTM models to platform-specific implementations in C. Formal verification is used to ensure correctness of the Event-B models. The portability offered by our methodology is demonstrated by modelling a Reinforcement Learning (RL) based RTM and generating implementations for two different platforms that all achieve energy savings on the respective platforms. The generated RTM code has been integrated with the PRiME framework, a cross-layer framework for embedded power management.

CONSTRAINED RANDOM APPLICATION GENERATION FOR FIRMWARE-BASED POWER MANAGEMENT VALIDATION

Authors: Vladimir Herdt¹, Hoang M. Le², Daniel Große² and Rolf Drechsler²

¹Universität Bremen, DE; ²University of Bremen, DFKI GmbH, DE

Timeslots:

- **UB09.3** (Thursday, March 22, 2018 1000 - 1200)

Abstract: Efficient power management (PM) is very important for modern SoCs. To handle the every rising complexity of embedded system design, power aware virtual prototypes (VPs) are employed to enable an early power analysis. Most modern SoCs implement the PM strategy in firmware (FW) due to ease of development. Validation of these strategies at VP level is crucial as undetected flaws will propagate. However, existing validation approaches are based on engineered software (SW), which might miss rare corner cases. We propose a demonstrator based on a novel approach to assess the power-versus-performance trade-off of FW-based PM. Instead of executing real SW applications, our approach makes use of workload scenarios described by a set of constraints to automatically generate SW with a specific power consumption profile. The main novelty is the modeling of scenarios based on constrained random techniques that are very successful in the area of SoC/HW functional validation.

DISGUIISING THE INTERCONNECTS: EFFICIENT PROTECTION OF DESIGN IP

Authors: Johann Knechtel¹, Satwik Patnaik², Mohammed Ashraf³ and Ozgur Sinanoglu³

¹NYU Abu Dhabi, AE; ²New York University, US; ³New York University Abu Dhabi, AE

Timeslots:

- **UB03.3** (Tuesday, March 20, 2018 1500 - 1730)

Abstract: Ensuring the trustworthiness and security of electronics has become an urgent challenge in recent years. Among various concerns, the protection of design intellectual property (IP) is to be addressed, due to outsourcing trends for the manufacturing supply chain and malicious end-user. In other words, adversaries either residing in the off-shore fab or in the field may want to obtain and pirate the design IP. As classical design tools do not consider such threats, there is clearly a need for security-aware EDA techniques. Here we present novel but proven techniques for efficient protection of design IP, embedded in an industrial-level design flow using Cadence Innovus. The key idea in our work is that disguising the interconnects is supremely suitable to protect design IP, while inducing only little additional cost and providing strong resilience. We share our customized libraries with the community, and we demonstrate our design flow and its security measures.

EMBEDDED ACCELERATION OF IMAGE CLASSIFICATION APPLICATIONS FOR STEREO VISION SYSTEMS

Authors: Mohammad Lonj¹, Carl Ahlberg², Masoud Daneshalab², Mikael Ekström² and Mikael Sjödin²

¹MDH, SE; ²Mälardalen University, SE

Timeslots:

- **UB02.9** (Tuesday, March 20, 2018 1230 - 1500)
- **UB07.6** (Wednesday, March 21, 2018 1400 - 1600)

Abstract: Autonomous systems are used in a broad range of applications from indoor utensils to medical application. Stereo vision cameras probably are the most flexible sensing way in these systems since they can extract depth, luminance, color, and shape information. However, stereo vision based applications suffer from huge image sizes, computational complexity and high energy consumption. To tackle these challenges, we first developed GIMME2 [1], a high-throughput, and cost efficient FPGA-based stereo vision system. In the next step, we present a novel approximation accelerator which is also compatible with GIMME2. Our accelerator tries to map neural network (NN) based image classification algorithms to FPGA by using DeepMaker which is an evolutionary based module embed in our accelerator that regenerates a near-optimal NN in term of accuracy. Then, the back-end side of DeepMaker maps the generated NN to FPGA. We will demo a GIMME2-based accelerator for image classification applications.

EVOAPPROX: LIBRARIES AND GENERATORS OF APPROXIMATE CIRCUITS

Authors: Lukas Sekanina, Zdenek Vasicek and Vojtech Mrazek, Brno University of Technology, CZ

Timeslots:

- **UB05.7** (Wednesday, March 21, 2018 1000 - 1200)
- **UB08.2** (Wednesday, March 21, 2018 1600 - 1800)

Abstract: Our contribution deals with a fully automated functional approximation methodology for combinational digital circuits. We present open

libraries of approximate circuits and tools performing desired approximations. Our approach uses a multi-objective genetic programming-based method to automatically design approximate k-bit adders and multipliers ($k = 8, 12, 16, 32$). All circuits can be downloaded from [1] at the level of a source code (C, Verilog, and Matlab). Several error metrics are pre-calculated and formal guarantees are given in terms of these errors. By means of an interactive web interface the user can easily find the best trade-off between the error and electrical parameters provided for 45/90/180 nm technology process. We will also demonstrate the circuit design flow developed. References: [1] <http://www.fit.vutbr.cz/research/groups/ehw/approxlib/>

FWCMS: AN EMBEDDED WALK-CYCLE MONITORING SYSTEM USING BODY AREA COMMUNICATION AND SECURE LOW-POWER DYNAMIC SIGNALING

Authors: Shahzad Muzaffar¹ and Ibrahim (Abe) M. Elfadel²

¹Masdar Institute, Khalifa University of Science and Technology, AE;

²Khalifa University of Science and Technology, AE

Timeslots:

- **UB04.1** (Tuesday, March 20, 2018 1730 - 1930)
- **UB08.1** (Wednesday, March 21, 2018 1600 - 1800)

Abstract: The demo presents a novel ultra-low power, embedded, and wearable walk-cycle monitoring system with applications in areas such as healthcare, robotics, sports medicine, physical therapy, prosthesis, and animal sports. Customized shoes with sensors continuously measure the forces, and an electronic digital assistant is used to analyze the acquired measurements in real time by employing an IMU free and self-synchronizing method in order to estimate weight and study motion patterns. To achieve ultra-low power operation, the human body is used as a communication medium between the sensors and the digital assistant. The single-channel behavior of the human body is accommodated with a novel, simple yet robust single-wire signaling technique, Pulsed-Index Communication (PIC), that significantly reduces the system footprint and overall power consumption as it eliminates the need for clock and data recovery. The system prototype has been rigorously and successfully tested.

EXPERIENCE-BASED AUTOMATION OF ANALOG IC DESIGN

Authors: Florian Leber and Juergen Scheible, Reutlingen University, DE

Timeslots:

- **UB02.4** (Tuesday, March 20, 2018 1230 - 1500)
- **UB04.10** (Tuesday, March 20, 2018 1730 - 1930)
- **UB05.10** (Wednesday, March 21, 2018 1000 - 1200)
- **UB06.10** (Wednesday, March 21, 2018 1200 - 1400)
- **UB07.10** (Wednesday, March 21, 2018 1400 - 1600)
- **UB08.10** (Wednesday, March 21, 2018 1600 - 1800)
- **UB09.10** (Thursday, March 22, 2018 1000 - 1200)

Abstract: While digital design automation is highly developed, analog design automation still remains behind the demands. Previous circuit synthesis approaches, which are usually based on optimization algorithms, do not satisfy industrial requirements. A promising alternative is given by procedural approaches (also known as "generators"): They (a) emulate experts' decisions, thus (b) make expert knowledge re-usable and (c) can consider all relevant aspects and constraints implicitly. Nowadays, generators are successfully applied in analog layout (Pcells, Pycells). We aim at an entire design flow completely based on procedural automation techniques. This flow will consist of procedures for the generation of schematics and layouts for every typical analog circuit class, such as amplifier, bandgap, filter a.s.o. In our presentation we give an overview on such a design flow and we show an approach for capturing an analog circuit designer's strategy as an executable "expert design plan".

FPGA-BASED HARDWARE ACCELERATOR FOR DRUG DISCOVERY

Authors: Ghaith Tarawneh, Alessandro de Gennaro, Georgy Lukyanov and Andrey Mokhov, Newcastle University, UK

Timeslots:

- **UB03.8** (Tuesday, March 20, 2018 1500 - 1730)
- **UB10.2** (Thursday, March 22, 2018 1200 - 1430)

Abstract: We present an FPGA-based hardware accelerator for drug discovery, developed during the EPSRC programme grant POETS (EP/N031768/1) in partnership with e-Therapeutics, an Oxford based drug discovery company. e-Therapeutics is pioneering a novel form of drug discovery based on analyzing protein interactome networks (<https://www.youtube.com/watch?v=wQFpTtuzrgA>). This approach can discover suitable drug candidates much more efficiently compared to wet lab testing but requires considerable computing power, particularly because commodity computers are generally inefficient at analyzing large-scale networks. The presented accelerator, consisting of an FPGA board with a silicon-mapped protein interactome plus accompanying software formalisms and tools, can deliver a 1000x speed up in this application compared to software running on commodity computers. We will showcase demos in which we run in-silico analysis of protein interactomes to test drug effects and visualize the results in real-time.

GENERATING FULL-CUSTOM SCHEMATICS IN A MIXED-SIGNAL TOP-DOWN DESIGN FLOW

Authors: Tobias Markus¹, Markus Mueller² and Ulrich Bruening¹
¹University of Heidelberg, DE; ²Extoll GmbH, DE

Timeslots:

- **UB02.2** (Tuesday, March 20, 2018 1230 - 1500)
- **UB03.2** (Tuesday, March 20, 2018 1500 - 1730)
- **UB04.2** (Tuesday, March 20, 2018 1730 - 1930)
- **UB07.1** (Wednesday, March 21, 2018 1400 - 1600)

Abstract: Design time is one of the precious assets in the cycle of hardware design. The top down methodology has been used in digital designs very successfully and now we also apply it for analog and mixed signal designs. Generating most of the structures automatically saves time and avoids errors. A Top Down Design Flow for Mixed Signal Designs is used which generates the schematic structure from the system RNM representation. Since the structural verilog part of the system level design will automatically generate the schematic structure it is only the functional part which is missing and has to be implemented by the analog designer. Some often used blocks can be used as an entry point to partially generate parts of the design in the schematic and furthermore even parts of the layout. We will demonstrate this design method with an example project.

HARDENING THE HARDWARE: A REVERSE-ENGINEERING RESILIENT SECURE CHIP

Authors: Abhrajit Sengupta¹, Muhammad Yasin², Mohammed Nabeel³, Mohammed Ashraf³, Jeyavijayan Rajendran⁴ and Ozgur Sinanoglu³
¹New York University, AE; ²New York University, US; ³New York University Abu Dhabi, AE; ⁴Texas A&M, US

Timeslots:

- **UB03.4** (Tuesday, March 20, 2018 1500 - 1730)

Abstract: With the globalization of integrated circuit (IC) supply chain, the semi-conductor industry is facing a number of threats, such as Intellectual Property (IP) piracy, hardware Trojans, and counterfeiting. To defend against such threats at the hardware level, logic locking was pro-

posed as a promising countermeasure. Yet, several recent attacks have completely undermined its security by successfully retrieving the secret key. Here, we present stripped-functionality logic locking (SFLL), which resists all existing attacks by hiding a part of the functionality in the form of a secret key. We leverage security-aware synthesis to develop a computer-aided design (CAD) framework that meets the desired security criterion at a minimal cost of 5%, 0.5%, and 8% for power, performance, and area, respectively. Moreover, we taped out a chip, the first such prototype of its kind, by applying our technique on an industry level processor, namely, ARM Cortex-M0 microprocessor in 65nm technology.

IIDEAA: DESIGN SPACE EXPLORATION FOR FUNCTIONAL-LEVEL APPROXIMATION

Authors: Marcello Traiola¹, Mario Barbareschi², Marcello Traiola³ and Alberto Bosio³

¹LIRMM, FR; ²DIETI - University of Naples Federico II, IT; ³LIRMM - University of Montpellier / CNRS, FR

Timeslots:

- **UB01.7** (Tuesday, March 20, 2018 1030 - 1230)

Abstract: Approximate Computing (AxC) aims at enabling the production of computing systems which can satisfy the rising performance demands and can improve the energy efficiency. AxC exploits the gap between the level of accuracy required by the users and the precision provided by the computing system, for achieving diverse optimizations. Various AxC techniques have been proposed so far for several applications and, unfortunately, existing approaches are application specific and a general and systematic methodology to automatically define approximate algorithms is still an open challenge. In this work we introduce a methodology which makes use of mutation techniques to obtain approximate versions of a given application described as a C/C++ code. We designed and implemented IIDEAA, an automatic tool exploiting (i) a source-to-source manipulation technique and (ii) an Evolutionary search engine, in order to search for the best functional approximation version of the given C/C++ code.

IIP GENERATORS TO EASE ANALOG IC DESIGN

Authors: Benjamin Prautsch, Uwe Eichler and Torsten Reich, Fraunhofer Institute for Integrated Circuits IIS/EAS, DE

Timeslots:

- **UB01.8** (Tuesday, March 20, 2018 1030 - 1230)
- **UB07.8** (Wednesday, March 21, 2018 1400 - 1600)
- **UB09.8** (Thursday, March 22, 2018 1000 - 1200)
- **UB10.8** (Thursday, March 22, 2018 1200 - 1430)

Abstract: Semiconductor technology has shown significant progress over the last decades. Digital EDA (electronic design automation) allowed that this progress could be converted to high-performance digital ICs. Analog components are part of Systems-on-Chip (SoC) too, but analog EDA lags far behind. Therefore, a lot of effort was spent to automate analog IC design. Major results are constraint-based layout-aware optimization tools using predefined layout templates or pure automation as well as analog generators containing expert knowledge. While optimization is a holistic top-down approach, generators allow parameterized and fast bottom-up generation of critical schematic and layout parts, pre-planned by experienced designers. With IIP Generators, we follow three use cases to ease analog design: 1) design on higher hierarchy levels, 2) development of hierarchical high-level IIPs, and 3) automated design porting due to highly technology-independent blocks down to 22nm.

OISC MULTICORE STENCIL PROCESSOR: ONE INSTRUCTION-SET COMPUTER-BASED MULTICORE PROCESSOR FOR STENCIL COMPUTING

Authors: Kaoru Saso, Jing Yuan Zhao and Yuko Hara-Azumi, School of Engineering, Tokyo Institute of Technology, JP

Timeslots:

- **UB02.3** (Tuesday, March 20, 2018 1230 - 1500)
- **UB05.3** (Wednesday, March 21, 2018 1000 - 1200)
- **UB07.3** (Wednesday, March 21, 2018 1400 - 1600)
- **UB11.3** (Thursday, March 22, 2018 1430 - 1630)

Abstract: Subtract and Branch on NEGative with 4 operands (SUBNEG4) is one of One Instruction-Set Computers that execute only one type of instruction. Thanks to its simplicity, SUBNEG4 has only 1/20x circuit area and 1/10x power consumption against MIPS processor. As SUBNEG4 is Turing-complete, it is suitable for parallel computing by multiple cores, while keeping its low-power feature. Our on-going project is seeking for effective use and deployment of SUBNEG4 cores on embedded systems. Our booth will demonstrate the significant speed-up by a SUBNEG4-based many-core processor against a conventional processor, for stencil computing. Our 64-core processor efficiently handles 2D von-Neumann neighborhood stencils, e.g., wave simulation by Verlet integration and 2D Jacobi iteration, to compute 64 points simultaneously. We show that small many-core processors can be realized even with such large number of cores while achieving good speed-up for heaving computation.

OTPG: SPECIFICATION-BASED CONSTRUCTION OF ONLINE TPGS FOR MICROPROCESSORS

Authors: Mikhail Chupilko, Alexander Kamkin and Andrei Tatarnikov, ISP RAS, RU

Timeslots:

- **UB01.4** (Tuesday, March 20, 2018 1030 - 1230)
- **UB04.4** (Tuesday, March 20, 2018 1730 - 1930)
- **UB09.7** (Thursday, March 22, 2018 1000 - 1200)

Abstract: This work presents an approach to construction of online test program generators (TPGs). The approach is intended to use specifications of ISA presented in nML/mmuSL specification languages. They are processed by a meta-generator to obtain their binary representations supplied with meta information and a test generation core compatible with the target microprocessor. The test generation core is loaded as a binary image into the target microprocessor's memory (for experiments we're using QEMU for MIPS) and produces test cases to be processed (incl. results checking) by an executor. It should be noticed that the meta-generator and the executor are not obligatory run at the same microprocessor (especially, if it is highly incomplete). The final goal of the project is to propose a method of obtaining online TPGs for a wide range of ISAs, and to develop a mature tool implementing this method.

POWER-AWARE SOFTWARE MAPPING OF PARALLEL APPLICATIONS ONTO HETEROGENEOUS MPSOCS

Authors: Gereon Onnebrink and Rainer Leupers, RWTH Aachen University, DE

Timeslots:

- **UB09.4** (Thursday, March 22, 2018 1000 - 1200)

Abstract: Heterogeneous multi- and many-processor systems-on-chip provide the best trade-off between performance, cost, and power. One

of the biggest hurdles to exploit multicore architectures from the SW side. Considering an application that has been properly partitioned into multiple concurrent tasks, and programmed in a parallel language, the process of mapping those tasks onto the processors with optimal DVFS is a huge challenge for a certain design goal. An automatic approach is needed that determines the optimal decision. A great amount of research has been conducted aiming to optimise the performance of a parallelised application. Another research track is the ESL power estimation methodology. Combining both, a novel power-aware software mapping heuristic has been implemented to develop performance and power co-optimized parallel software. This algorithm can be used to identify the gain of sophisticated power management techniques by providing the power-performance trade-off.

PRIME: PLATFORM- AND APPLICATION-AGNOSTIC RUN-TIME POWER MANAGEMENT OF HETEROGENEOUS EMBEDDED SYSTEMS

Authors: Domenico Balsamo, Graeme M. Bragg, Charles Leech and Geoff V. Merrett, University of Southampton, UK

Timeslots:

- **UB02.7** (Tuesday, March 20, 2018 1230 - 1500)
- **UB04.3** (Tuesday, March 20, 2018 1730 - 1930)
- **UB06.7** (Wednesday, March 21, 2018 1200 - 1400)

Abstract: Increasing energy efficiency and reliability at runtime is a key challenge of heterogeneous many-core systems. We demonstrate how contributions from the PRIME project integrate to enable application- and platform-agnostic runtime management that respects application performance targets. We consider opportunities to enable runtime management across the system stack and we enable cross-layer interactions to trade-off power and reliability with performance and accuracy. We consider a system as three distinct layers, with abstracted communication between them, which enables the direct comparison of different approaches, without requiring specific application or platform knowledge. Application-agnostic runtime management is demonstrated with a selection of runtime managers from PRIME, including linear regression modelling and predictive thermal management, operating across multiple applications. Platform-independent runtime management is demonstrated using two heterogeneous platforms.

RECONFIGURABLE SELF-TIMED DATAFLOW ACCELERATOR

Authors: Danil Sokolov, Alessandro de Gennaro and Andrey Mokhov, Newcastle University, UK

Timeslots:

- **UB03.5** (Tuesday, March 20, 2018 1500 - 1730)
- **UB10.5** (Thursday, March 22, 2018 1200 - 1430)

Abstract: Many applications require reconfigurable pipelines to handle incoming data items differently depending on their values or the operating mode. Currently, reconfigurable synchronous pipelines are the mainstream of dataflow accelerators. However, there are certain advantages to be gained from self-timed dataflow processing, e.g. robustness to unstable power supply, data-dependent performance, etc. To become attractive for industry, reconfigurable asynchronous pipelines need a formal behavioural model and design automation. This demo will present a design flow for the specification, verification and synthesis of reconfigurable self-timed pipelines using Dataflow Structure formalism in Workcraft (<https://workcraft.org/>). As a case study we will use an asynchronous accelerator for Ordinal Pattern Encoding (OPE) with reconfigurable pipeline depth. We will exhibit the resultant OPE chip fabricated in TSMC90nm to show the benefits of reconfigurability and asynchrony for dataflow processing.

REPABIT: AUTOMATED DESIGN OF RELOCATABLE PARTIAL BITSTREAMS

Authors: Jens Rettkowski¹ and Diana Göhringer²

¹Ruhr-University Bochum, DE; ²Technische Universität Dresden, DE

Timeslots:

- **UB05.8** (Wednesday, March 21, 2018 1000 - 1200)

Abstract: Dynamic partial reconfiguration of FPGAs enables the replacement of hardware modules at runtime without disturbing remaining hardware modules. The standard vendor tools generate a specific partial bitstream for each reconfigurable region. Relocation generates a partial bitstream in such a way, that it can be moved to different regions. Hence, the number and the time to generate bitstreams is reduced. In this work, RePaBit is presented that automates the generation of relocatable partial bitstreams for Xilinx Vivado. TCL scripts check the compatibility of resource footprints and arrange identical partition pins in all regions for the connection of relocatable modules with the remaining design. Feedthrough routes are avoided using the isolation design flow from Xilinx. The results show an overhead of LUTs by 0.7% and a frequency reduction of only 1.5%. Nevertheless, RePaBit simplifies the design and reduces the design time as well as the needed memory for storing the partial bitstreams.

RISC-V PROCESSOR MODELING IN IP-XACT USING KACTUS²

Authors: Esko Pekkarinen and Timo Hämäläinen, Tampere University of Technology, FI

Timeslots:

- **UB02.8** (Tuesday, March 20, 2018 1230 - 1500)
- **UB06.8** (Wednesday, March 21, 2018 1200 - 1400)
- **UB10.4** (Thursday, March 22, 2018 1200 - 1430)

Abstract: The complexity of modern embedded system design is managed by advanced, high-level design methodologies such as IP-XACT. However, integrating IP-XACT as a part of an existing design flow and packaging legacy sources is too often inhibited by the inherent differences between IP-XACT and the traditional hardware description languages. In this work, we take an existing Verilog implementation of a RISC-V microprocessor and package it with our open-source IP-XACT tool Kactus². The resulting IP-XACT description will be publicly available and based on the modeling experience we report the observed pitfalls in the transition from HDL to IP-XACT.

ROS X FPGA FOR ROBOT-CLOUD SYSTEM: ROBOT-CLOUD COOPERATIVE VISUAL SLAM PROCESSING USING ROS-COMPLIANT FPGA COMPONENT

Authors: Takeshi Ohkawa, Yuhei Sugata, Aoi Soya, Kanemitsu Ootsu and Takashi Yokota, Utsunomiya University, JP

Timeslots:

- **UB05.4** (Wednesday, March 21, 2018 1000 - 1200)
- **UB06.4** (Wednesday, March 21, 2018 1200 - 1400)
- **UB07.4** (Wednesday, March 21, 2018 1400 - 1600)
- **UB08.4** (Wednesday, March 21, 2018 1600 - 1800)

Abstract: Distributed processing in robot-cloud cooperative system is discussed in terms of processing performance and communication performance. Cooperation of robots and cloud-servers is inevitable for realizing intelligent robots in the next generation society and industry. To

improve processing performance of the cooperative system, we utilize ROS-compliant FPGA component as a robot-side embedded processing for low-power and high-performance image processing. We prepare two demonstrations. (1) Key-point Detection from camera image using Fully-hardwired ROS-Compliant FPGA component In the evaluation, the processing performance of the component is almost same as PC, while it operates at more than 10 times less power (5W), compared to PC (50W). (2) Distributed Visual SLAM using two-wheeled robot (TurtleBot3) Distributed Visual SLAM (Simultaneous Localization and Mapping) are presented as a concrete example of the robot-cloud cooperative system.

SPANNER: SELF-REPAIRING SPIKING NEURAL NETWORK CONTROLLER FOR AN AUTONOMOUS ROBOT

Authors: Alan Millard¹, Anju Johnson¹, James Hilder¹, David Halliday¹, Andy Tyrrell¹, Jon Timmis¹, Junxiu Liu², Shvan Karim², Jim Harkin² and Liam McDavid²

¹University of York, UK; ²Ulster University, UK

Timeslots:

- **UB03.6** (Tuesday, March 20, 2018 1500 - 1730)
- **UB05.6** (Wednesday, March 21, 2018 1000 - 1200)
- **UB11.6** (Thursday, March 22, 2018 1430 - 1630)

Abstract: The human brain is remarkably resilient, and is able to self-repair following injury or a stroke. In contrast, electronic systems typically exhibit limited self-repair capabilities, and cannot recover from faults. We demonstrate a bio-inspired approach to self-repair that allows an autonomous robot to recover from faults in its artificial 'brain'. Astrocytes are support cells in the human brain that interact with neurons to regulate synaptic activity. We have modelled this interaction to create a spiking neural network that can self-repair when synapses between neurons are damaged, by strengthening redundant pathways. We demonstrate a robot platform controlled by a self-repairing spiking neural network that is implemented on an FPGA. We demonstrate that injecting faults into the synapses of the network initially causes the robot to behave erratically, but that the neural controller is able to automatically repair itself, thus allowing the robot to resume normal function.

SYSTEM-LEVEL OPERATING CONDITION CHECKS: AUTOMATED AUGMENTATION OF VERILOGAMS MODELS

Authors: Georg Gläser¹, Martin Grabmann¹, Gerrit Kropp¹ and Andreas Fürtig²

¹Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE; ²Goethe University Frankfurt, DE

Timeslots:

- **UB06.1** (Wednesday, March 21, 2018 1200 - 1400)

Abstract: Analog/Mixed-Signal design and verification strongly relies on more or less abstract models to make extensive simulations feasible. Maintaining consistent behavior between system model and implementation is crucial for a correct verification. This also involves the operating conditions: A faulty model might introduce false-positive verification results despite of e.g. an incorrect supply voltage or missing bias currents. We present an automated workflow for extracting these checks from a transistor-level implementation and transfer it into a given Verilog-AMS model. The correctness of our approach is proved by evaluating the model coverage between the implementation and the model. As a demonstration scenario, we use a demodulator component of a HF RFID communication system. We extract the acceptance region from the transistor-level schematic and automatically generate and integrate a model safe-guard unit for performing the operating condition check.

T-CREST: THE OPEN-SOURCE REAL-TIME MULTICORE PROCESSOR

Authors: Martin Schoeberl, Luca Pezzarossa and Jens Sparsø, Technical University of Denmark, DK

Timeslots:

- **UB03.7** (Tuesday, March 20, 2018 1500 - 1730)
- **UB04.7** (Tuesday, March 20, 2018 1730 - 1930)
- **UB07.7** (Wednesday, March 21, 2018 1400 - 1600)
- **UB08.7** (Wednesday, March 21, 2018 1600 - 1800)

Abstract: Future real-time systems, such as advanced control systems or real-time image recognition, need more powerful processors, but still a system where the worst-case execution time (WCET) can be statically predicted. Multicore processors are one answer to the need for more processing power. However, it is still an open research question how to best organize and implement time-predictable communication between processing cores. T-CREST is an open-source multicore processor for research on time-predictable computer architecture. It consists of several Patmos processors connected by various time-predictable communication structures: access to shared off-chip, access to shared on-chip memory, and the Argo network-on-chip for fast inter-processor communication. T-CREST is supported by open-source development tools, such as compilation and WCET analysis. To best of our knowledge, T-CREST is the only fully open-source architecture for research on future real-time multicore architectures.

TOPOLINANO & MAGCAD: A DESIGN AND SIMULATION FRAMEWORK FOR THE EXPLORATION OF EMERGING TECHNOLOGIES

Authors: Umberto Garlando and Fabrizio Riente, Politecnico di Torino, IT

Timeslots:

- **UB01.2** (Tuesday, March 20, 2018 1030 - 1230)
- **UB03.1** (Tuesday, March 20, 2018 1500 - 1730)
- **UB05.2** (Wednesday, March 21, 2018 1000 - 1200)
- **UB06.2** (Wednesday, March 21, 2018 1200 - 1400)
- **UB09.2** (Thursday, March 22, 2018 1000 - 1200)

Abstract: We developed a design framework that enables the exploration and analysis of emerging beyond-CMOS technologies. It is composed of two powerful tools: ToPoliNano and MagCAD. Different technologies are supported, and new ones could be added thanks to their modular structure. ToPoliNano starts from a VHDL description of a circuit and performs the place&route following the technological constraints. The resulting circuit can be simulated both at logical or physical level. MagCAD is a layout editor where the user can design custom circuits, by placing basic elements of the selected technology. The tool can extract a VHDL netlist based on compact models of placed elements derived from experiments or physical simulations. Circuits can be verified with standard VHDL simulators. The design workflow will be demonstrated at the U-booth to show how those tools could be a valuable help in the studying and development of emerging technologies and to obtain feedbacks from the scientific community.

TTOOL/OMC: OPTIMIZED COMPILATION OF EXECUTABLE UML/SYSML DIAGRAMS FOR THE DESIGN OF DATA-FLOW APPLICATIONS

Authors: Andrea Enrici¹, Julien Lallet¹, Renaud Pacalet² and Ludovic Apvrille²

¹Nokia Bell Labs, FR; ²Telecom ParisTech, FR

Timeslots:

- **UB02.6** (Tuesday, March 20, 2018 1230 - 1500)
- **UB06.6** (Wednesday, March 21, 2018 1200 - 1400)
- **UB10.6** (Thursday, March 22, 2018 1200 - 1430)

Abstract: Future 5G networks are expected to increase data rates by a factor of 10x. To meet this requirement, baseband stations will be equipped with both programmable (e.g., CPUs, DSPs) and reconfigurable components (e.g., FPGAs). Efficiently programming these architectures is not trivial due to the inner complexity and interactions of these two types of components. This raises the need for unified design flows capable of rapidly partitioning and programming these mixed architectures. Our demonstration will show the complete system-level design and Design Space Exploration, based on UML/SysML diagrams, of a 5G data-link layer receiver, that is partitioned onto both programmable and reconfigurable hardware. We realize an implementation of such a UML/SysML design by compiling it into an executable C application whose memory footprint is optimized with respect to a given scheduling. We will validate the effectiveness of our solution by comparing automated vs manual designs.

VIRTUAL PROTOTYPE MAKANI: ANALYZING THE USAGE OF POWER MANAGEMENT TECHNIQUES AND EXTRA-FUNCTIONAL PROPERTIES BY USING VIRTUAL PROTOTYPING

Author: Sören Schreiner, OFFIS – Institute for Information Technology, DE

Timeslots:

- **UB01.10** (Tuesday, March 20, 2018 1030 - 1230)
- **UB05.5** (Wednesday, March 21, 2018 1000 - 1200)
- **UB09.5** (Thursday, March 22, 2018 1000 - 1200)

Abstract: My Phd work consists of analyzing the correct usage of power management techniques, as well as the analysis of extra-functional properties, including power and timing properties, in MPSoCs. Especially in safety-critical environments the power management gets safety-critical too, since it is able to influence the overall system behavior. To demonstrate my methodologies a mixed-critical multi-rotor system and its corresponding virtual prototype is used. The multi-rotor system's avionics is served by a Xilinx Zynq 7000 MPSoC. The hardware architecture includes ARM and MicroBlaze cores, a NoC for communication and peripherals. The MPSoC processes the flight algorithms with triple modular redundancy and a mission-critical video processing task. The virtual prototype consists of a virtual platform and an environmental model. The virtual platform is equipped with my measuring tool libraries to generate traces of the observed power management techniques and the extra-functional properties.

WARE: WEARABLE ELECTRONICS DIRECTIONAL AUGMENTED REALITY

Authors: Gabriele Miorandi¹, Walter Vendraminetto², Federico Fracca-
roli³, Davide Quaglia⁴ and Gianluca Benedetti⁴

¹University of Verona, IT; ²EDALab Srl, IT; ³Wagoo LLC, IT; ⁴Wagoo Italia
srls, IT

Timeslots:

- **UB01.6** (Tuesday, March 20, 2018 1030 - 1230)
- **UB08.6** (Wednesday, March 21, 2018 1600 - 1800)
- **UB09.6** (Thursday, March 22, 2018 1000 - 1200)

Abstract: Augmented Reality (AR) currently require large form factors, weight, cost and frequent recharging cycles that reduce usability. Connectivity, image processing, localization, and direction evaluation lead to high processing and power requirements. A multi-antenna system, patented by the industrial partner, enables a new generation of smart eye-wear that elegantly requires less hardware, connectivity, and power to provide AR functionalities. They will allow users to directionally locate nearby radio emitting sources that highlight objects of interest (e.g., people or retail items) by using existing standards like Bluetooth Low Energy, Apple's iBeacon and Google's Eddystone. This booth will report the current level of research addressed by the Computer Science Department of University of Verona, Wagoo LLC, and Wagoo Italia srls. In the presented demo, different objects emit an "I am here" signal and a prototype of the smart glasses shows the information related to the observed object.

WIRELESS SENSOR SYSTEM WITH ELECTROMAGNETIC ENERGY HARVESTER FOR INDUSTRY 4.0 APPLICATIONS

Authors: Bianca Leistritz, Elena Chervakova, Sven Engelhardt, Axl
Schreiber and Wolfram Kattaneck, Institut für Mikroelektronik- und
Mechatronik-Systeme gemeinnützige GmbH, DE

Timeslots:

- **UB06.5** (Wednesday, March 21, 2018 1200 - 1400)
- **UB07.5** (Wednesday, March 21, 2018 1400 - 1600)
- **UB08.5** (Wednesday, March 21, 2018 1600 - 1800)

Abstract: An energy-autonomous and adaptive wireless multi-sensor system for a wide range of Industry 4.0 applications is presented here. By taking a holistic view of the sensor system and of the specific interactions of its components, technological barriers of individual system elements can be overcome. The energy supply of the demonstrator is realized by a miniaturized electromagnetic energy harvester, which could be easily and quickly adapted to the application-specific boundary conditions with the help of a computer assisted design process. Variations in the available energy are monitored by advanced energy management functions. The modular hardware and software platform is demonstrated by an adaptive measurement and data transmission rate. Communication takes place by means of industry 4.0 compliant standard protocols. The demonstrator was developed in the research group Green-ISAS funded by the Free State of Thuringia from the European Social Fund (ESF) under grant no. 2016 FGR 0055.

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University Booth Co-Chairs

Jens Lienig, Technische Universität Dresden, DE and
Andreas Vörg, edacentrum, DE

university-booth@date-conference.com

MON

TUE

WED

THU

FRI

FRINGE TECHNICAL MEETINGS

A number of specialist interest groups will be holding their meetings at DATE 2018. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage www.date-conference.com

Date & Time	Title	Room
MON 1400–1800	FM04 Forum: Advancing Diversity in EDA	Seminar 1
MON 1800–2100	FM01 Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA	Saal 1
TUE 1300–1430	FM05 eTTTC Meeting	Seminar 5
TUE 1400–1800	CW01 Carbon Nanotubes: The key to unlock future VLSI Interconnects?	Seminar 1
TUE 1615–1800	FM02 EDAA General Assembly	Seminar 2
WED 1230–1430	FM06 Meeting of the IFIP Working Group 10.5	Seminar 5
THU 1230–1300	FM07 DATE Sister Events Meeting	Lunch area (Großer Saal+ Saal 1)

MON

Forum: Advancing Diversity in EDA

Seminar 1 1400 - 1800

Organisers: Ayse Coskun, Boston University, US
Eli Bozorgzadeh, Univ. of California, Irvine, US

This is the first edition of a half-day forum, including talks, panels, structured networking and mentoring sessions, and more. The goal of the event is to help improve the number and visibility of women and underrepresented minorities broadly in the EDA community. The event is sponsored by IEEE CEDA.

1400

Welcome and Introduction

Organisers: Ayse Coskun, Boston University, US
Elaheh Bozorgzadeh, University of California, Irvine, US

1415

Keynote: "VLSI Design Methods for Low Power Encryption"

Speaker: Ingrid Verbauwhede, KU Leuven and UCLA, BE

1445

Panel 1: Mastering Your Leadership Skills

Moderator: Elaheh Bozorgzadeh, University of California, Irvine, US
Panelists: Marilyn Wolf, Georgia Institute of Technology, US
Nuria Llin, Texas Instruments Europe, DE
Cristiana Bolchini, Politecnico di Milano, IT

1530

Coffee Break

- 1600 **Panel 2: Negotiating: Practical Strategies for Women and URM in Tech**
 Moderator: Ingrid Verbauwhede, KU Leuven and UCLA, BE
 Panelists: Ian Harris, University of California Irvine, US
 X. Sharon Hu, University of Notre Dame, US
 Aida Todri-Sanial, LIRMM, FR
- 1645 **Panel 3: Work-Life Balance: Myth or Reality?**
 Moderator: Hai Li, University of Pittsburgh, US
 Panelists: Nele Mentens, Katholieke Universiteit Leuven, BE
 Chengmo Yang, University of Delaware, US
 Laura Pozzi, USI Lugano, CH
- 1730 **Speed Mentoring Session**
- 1800 **Closing Remarks, followed by DATE Reception**

MON

Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Saal 1 1800 - 2100

Organiser: Cecilia Metra, University of Bologna, IT

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2018 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 19, 2018, from 1800 - 2100 in "Saal 1" of the ICC Dresden.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

- FM01-1 **An Optimization-Based Methodology for the Exploration of Cyber-Physical System Architectures**
 Author: Dmitrii Kirov, University of Trento, IT
- FM01-2 **Resilient Energy-Constrained Microprocessor Architectures**
 Authors: Anteneh Gebregiorgis and Mehdi Tahoori, Karlsruhe Institute of Technology, DE
- FM01-3 **Verified Model Refactorings for Hybrid Control Systems**
 Author: Sebastian Schlesinger, Technische Universität Berlin, DE
- FM01-4 **Exact Design of Digital Microfluidic Biochips**
 Author: Oliver Keszocze, University of Bremen, DE
- FM01-5 **A Functional Safety Approach for Cyber-Physical Systems**
 Author: Enrico Fraccaroli, Università degli Studi di Verona, IT
- FM01-6 **Research on Accuracy-Configurable Architecture for Applications and Systems**

Author: Tongxin Yang, Fukuoka University, JP

FM01-7 Social Insect-inspired Adaptive Hardware Systems

Authors: Matthew Rowlings, Andy Tyrrell and Martin Albrecht Trefzger
University of York, GB

FM01-8 Power Modeling for Fast Power Estimation on FPGA

Authors: Yehya Nasser, Jean-Christophe Prevotet and Maryline Helard
Institut national des sciences appliquées de Rennes (INSA) Rennes-IETR,
FR

FM01-9 Machine Learning Approaches for Hardware Reliability Modelling and Mitigation

Authors: Arunkumar Vijayan and Mehdi Tahoori, Karlsruhe Institute of
Technology, DE

FM01-10 Multi-formalism in Different Levels of Abstraction for Requirements Engineering and Design of Real-Time Systems

Authors: Fabiola Ribeiro¹, Achim Rettberg², Carlos E. Pereira³ and Michel
dos Santos Soares⁴

¹Universidade Federal de Uberlandia, BR; ²Carl von Ossietzky Universität
Oldenburg, DE; ³UFRGS, BR; ⁴Federal University of Sergipe, BR

FM01-11 Early Evaluation of Multicore Systems Soft Error Reliability Using Virtual Platforms

Author: Felipe Rocha da Rosa, UFRGS, BR

FM01-12 Spintronic memory towards Secure and Energy-Efficient Computing

Authors: Anirudh Iyengar and Swaroop Ghosh, Pennsylvania State
University, US

FM01-13 Energy-Efficient and Reliable Computing in Dark Silicon Era

Author: Mohammad-Hashem Haghbayan, University of Turku, FI

TUE

eTTTC Meeting

Seminar 5 1300 - 1430

Organiser: Alberto Bosio, LIRMM - University of Montpellier 2, FR

The European Test Technology Technical Council (eTTTC) is the European section of the TTTC. eTTTC is a volunteer professional organization sponsored by the IEEE Computer Society. TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art. This meeting provides all actors involved in test technology to share information on upcoming events and projects.

TUE

EDAA General Assembly

Seminar 2 1615 - 1800

Organiser: Norbert Wehn, University of Kaiserslautern, DE

General assembly meeting for the members of EDAA, open to everyone interested in Electronic Design Automation.

WED

Meeting of the IFIP Working Group 10.5

Seminar 5 1230 - 1430

International Federation for Information Processing (IFIP) is the leading multinational, non-political organization in Information & Communications Technologies and Sciences and is recognized by United Nations and other world bodies. It has over 100 Working Groups and 13 Technical Committees. This is a meeting organized by WK10.5 (VLSI related technologies).

THU

DATE Sister Events Meeting

Lunch area (Großer Saal+Saal 1) 1230 - 1300

Meeting of the representatives from ASP-DAC, ICCAD, DAC, DATE

CO-LOCATED WORKSHOPS

TUE

**Carbon Nanotubes:
The key to unlock future VLSI Interconnects?**

Seminar 1 1400 - 1830

Organisers: Salvatore Amoroso, Synopsys Inc., GB
Benjamin Uhlig, Fraunhofer IPMS, DE
Aida Todri-Sanial, CNRS-LIRMM/University of Montpellier, FR
Martin Landgraf, Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung, DE

The workshop will focus on Carbon Nanotube (CNT) technology as possible candidate for future VLSI interconnects. The major aspects of CNT interconnects will be covered, from the issues and solutions to growth/deposition local and global lines to the novel measurement and simulation methodologies necessary to characterize and understand CNT performances. Aim of the workshop is to disseminate the latest results arising from the H2020 EU-funded project CONNECT as well as to host invited talks from academia and industry to deepen the understanding of future Interconnect scenarios.



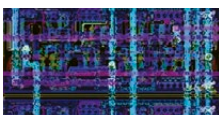
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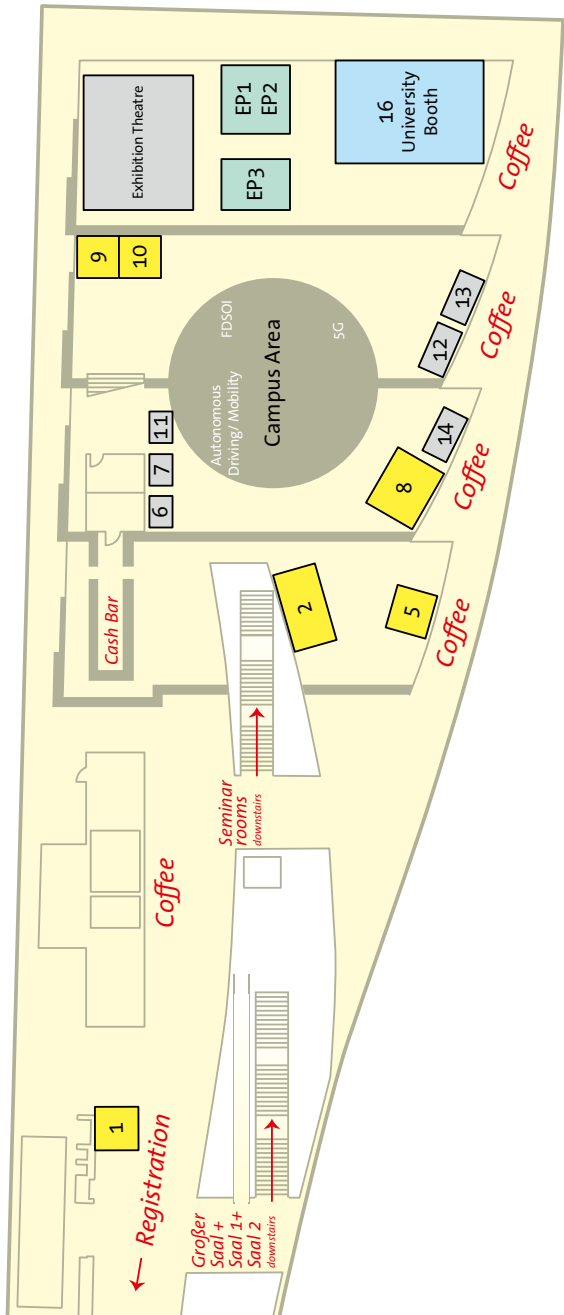
EXHIBITION GUIDE

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2018 and are happy to welcoming you in the beautiful city of Dresden, Germany!

All corporate sponsors and participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

EXHIBITION FLOOR PLAN	146
DATE 2018 SPONSORS AND EXHIBITORS	147
COMPANY PROFILES	148

EXHIBITION FLOOR PLAN



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Company	Booth
Advantest Europe GmbH	8
Arm Ltd.	6
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Circuits Multi-Projects (CMP)	9
City of Dresden, Economic Development Office	Sponsor 1
COEMS - Continuous Observation of Embedded Multicore Systems	EP 1
COSEDA Technologies GmbH	14
Dream Chip Technologies GmbH	Campus FDSOI
dReDBox (Disaggregated Data Center in a Box)	EP 2
EUROPRACTICE	10
Fraunhofer Institute for Integrated Circuits IIS	Campus FDSOI
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BOOTH 8

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A world-class technology company, Advantest is a leading producer of automatic test equipment for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Our exhibit, Cloud Testing Service, offers an alternative to standard test hardware. CTS addresses the challenges facing major chipmakers, R&D engineers, design labs, universities and research institutes to get access to large ATE testers to debug and test their devices. It is specially set up with a flexibly, pay per use model, ideal for R&D.

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W www.arm.com

Arm technology is at the heart of a computing and connectivity revolution that is transforming the way people live and businesses operate. From the unmissable to the invisible; our advanced, energy-efficient processor designs are enabling the intelligence in 90 billion silicon chips and securely powering products from smartphones to supercomputers, medical devices to agricultural sensors and base stations to servers. With more than 1,000 technology partners including the world's most famous business and consumer brands, we are collaborating to drive Arm innovation into all areas compute is happening from the chip to the network and the cloud.

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Cadence Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems. Cadence Academic Network is sponsoring the DATE Interactive Presentations (IPs) again.

CAMPUS
5G**cfaed Excellence Cluster / CRC HAEC**

TU Dresden
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W www.cfaed.tu-dresden.de

The Cluster of Excellence 'Center for Advancing Electronics Dresden' (cfaed) of Technische Universität Dresden comprises eleven research institutes in Saxony. Further members are the Technische Universität Chemnitz, two Max Planck Institutes, two Fraunhofer Institutes, two Leibniz Institutes and the Helmholtz-Research Center Dresden-Rossendorf. About 300 scientists are working in nine research paths to investigate completely new technologies for electronic information processing. These technologies are inspired by innovative materials such as silicon nanowires, carbon nanotubes or polymers or based on completely new conceptions such as circuit fabrication methods by self-assembling structures, e.g. DNA-Origami. The orchestration of these new devices into heterogeneous information processing systems with focus on their resilience and energy-efficiency is also part of cfaed's research program. To complement the Cluster, the Collaborative Research Center (CRC) 912 'Highly Adaptive Energy-Efficient Computing' (HAEC) has been integrated in cfaed. Both, cfaed and HAEC, are coordinated by Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis, who holds the Vodafone Chair Mobile Communications Systems at TU Dresden.

ASIC and SOC Design:

Design Entry • Behavioural Modelling & Simulation • Power & Optimisation

System-Level Design:

Behavioural Modelling & Analysis • Acceleration & Emulation • Hardware/Software Co-Design

Embedded Software Development:

Real Time Operating Systems • Software/Modelling

BOOTH 9

Circuits Multi-Projects (CMP)

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Circuits Multi-Projects (CMP) is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 70 countries have been served, more than 7000 projects have been prototyped through 1200 manufacturing runs, and 72 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and ams down to 28 nm FDSOI. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.

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Welcome to Dresden!

COEMS – Continuous Observation of Embedded Multicore Systems

University of Lübeck/
Institute for Software Engineering and Programming Languages
Ratzeburger Allee 160
23562 Lübeck
Germany

Contact: Nina Strugalla
T +49 451 31016530
M info@coems.eu
W www.coems.eu

The ability to observe the internals of an execution of a computer-based system is a fundamental requirement for ultimately ensuring correctness and safe behaviour. Within COEMS (Continuous Observation of Embedded Multicore Systems) a novel observer platform with supporting verification methods for software systems is developed. COEMS tackles the issues of detection and identification of non-deterministic software failures caused by race conditions and access to inconsistent data due to the inherent parallelism of modern multi-core processors. It gives insight to the system's actual behaviour without affecting it allowing new verification methods.

An efficient real-time access and analysis as a critical element for operating safe systems is developed and validated by COEMS. COEMS aims at shortening the development cycle by considerably increased test efficiency and effectivity, by increased debug efficiency (especially for non-deterministically occurring failures) and by supporting performance optimization. COEMS improves the reliability of delivered systems, enabling developers to identify, understand, and remove defects before release, as well as improving efficiency of software for multi-/many-core computing systems in terms of performance, real-time behaviour and energy consumption.

The two Global Players Thales Group and Airbus Group, both active in safety-critical domains, will validate the COEMS approach by suitable demonstrators, i.e. testing and debugging of real-world multicore applications. In addition to these two domains, we will address the domains of safety-critical medical applications, automation and automotive industry, as well as the Internet of Things.

The COEMS project is funded by the European Union's Horizon 2020 research and innovation programme under project id 732016.

Consortium:
University of Lübeck (DE)
Accemic Technologies (DE)
SC Thales Systems Romania SRL (RO)
Thales Austria GmbH (AT)
Airbus (DE)
Western Norway University of Applied Sciences (NO)

COSEDA Technologies GmbH

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01099 Dresden
Germany

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COSEDA Technologies provides software solutions in the field of system level design for complex electronic hard- & software products. We make latest modelling and simulation technologies available for our customers to enable them to master new concepts cost-effectively for innovative, complex and safety-critical products.

Our technologies have an over 18 year's history and are being used by leading companies, which develop circuits for automotive, communication, power, security critical (e.g. smart cards) and safety-critical applications. The founders of the company are experts, which were involved in the development and standardization (IEEE & Accellera) of the SystemC AMS modelling and simulation technology which is the basis for our main product COSIDE®.

The Design Environment COSIDE® is the first tool, which permits the design of electronic hard- & software components in the context of the whole system. It is easy to adapt and enables a cross-domain optimization of the system concept & architecture and thus the design of next generation products. COSIDE® is intuitive to use for soft- and hardware designers, while reducing the effort for modelling and simulation by the factor of 10.

Our Mission: We makes latest System modeling, simulation, design as well as verification methodologies efficient, practical and usable.

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Behavioural Modelling & Simulation • Verification • Analogue and Mixed-Signal Design • RF Design

System-Level Design:

Behavioural Modelling & Analysis • Hardware/Software Co-Design

Services:

Training

Embedded Software Development:

Software/Modelling

Dream Chip Technologies GmbH

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Germany

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W www.dreamchip.de

Dream Chip Technologies (DCT) is Germany's largest independent Engineering Service Provider with a cutting edge focus on the development and design of ASICs, SoCs, FPGAs, Embedded Software and discrete Systems with a special focus on ADAS ASICs for automotive vision systems (360 deg Top View, CMS).

More than 25 years of experience in the micro-electronics industry make us experts in turnkey solutions from specification to production and delivery – including embedded Linux or Android based board support packages (BSP), Linux or Android driver development or porting and high-speed PCB design with all necessary qualifications like CE and FCC.

Whether they are in the automotive, broadcast, consumer, industrial or medical market – our clients know they can always rely on our expertise and outstanding engineering skills.

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System-Level Design:

Physical Analysis • Acceleration & Emulation • Hardware/Software Co-Design • Package Design • PCB & MCM Design

Test:

Design for Test • Design for Manufacture and Yield • Logic Analysis • Test Automation (ATPG, BIST) • Boundary Scan • Silicon Validation • System Test

Services:

Design Consultancy • Prototyping • Foundry & Manufacturing

dReDBox (Disaggregated Data Center in a Box)

IBM Research/ IBM Dublin Technology Campus
Damastown Industrial Estate
Dublin 15, Mulhuddart
Ireland

Contact: Kostas Katrinis
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W www.dredbox.eu

For all the superior features that low-power computing systems exhibit compared to conventional high-end server designs, there has been a common design axiom that both technological trends are based on: the main-board and its hardware components form the baseline, monolithic building block that the rest of the hardware/software stack design builds upon. In such conventional systems, the proportionality of IT resources is fixed during design time and remains static throughout machine lifetime, with known ramifications in terms of low system resource utilization, costly upgrade cycles and degraded energy proportionality.

dReDBox takes on the challenge of revolutionizing the low-power computing ecosystem by breaking once and for all server boundaries through materialization of the concept of disaggregation. dReDBox is strategically tailored to entirely break the root cause of such effects by modularizing low-power components, innovating with optical interconnection technology of adequately low latency to sustain this paradigm shift and

providing for all required system software to drive fine-granular resource utilization. Through a highly modular, rack-scale architecture, dReDBox specifies, designs and prototypes modular blocks of SoC-based microservers, memory and accelerators, interconnected via a high-speed, low-latency optical fabric and integrated into a single platform. In a dReDBox system, pool instances can be allocated in arbitrary sets, as driven by fit-for-purpose resource/power management software.

dReDBox components allow for deployment in various integration form factors and target scenarios, as manifested by three target application use-cases being realized in the project, namely Security, Network Analytics and Telecom.

BOOTH 10

EUROPRACTICE

IMEC vzw
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3001 Leuven
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Contact: Paul Malisse
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M Paul.Malisse@imec.be
W www.imec.be

The EUROPRACTICE Service offers CAD tools to European academics for education, low cost and easy access to prototyping and small volume fabrication in ASIC, MEMS and photonics technologies. The service is offered by IMEC (B), STFC (UK) and Fraunhofer IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW runs whereby many designs are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7 μ to 22nm at well-known foundries (ONSem, ams, XFAB, IHP, GLOBALFOUNDRIES, TSMC, UMC). Additionally more than Moore technologies are offered from Memscap, imec and Leti. A total integrated design and manufacturing flow is offered including cell library, design kit access and support, ASIC prototyping on MPW. Commercial companies and overseas institutes can use the fabrication services at different conditions, including dedicated single project prototype runs, volume fabrication, qualification, assembly and test.

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Fraunhofer Institute for Integrated Circuits IIS

Am Wolfsmantel 33
91058 Erlangen
Germany

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T +49 9131 7764406
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W www.iis.fraunhofer.de

The Fraunhofer Institute for Integrated Circuits IIS is one of the world's leading application-oriented research institutions for microelectronic and IT system solutions and services. With the creation of mp3 and the co-development of AAC, the institute has reached worldwide recognition.

As one of the leading IC design facilities in Europe, we develop customized solutions to meet the constantly evolving requirements of industrial applications. Our work being independent of technology and manufacturer, we are able to provide our customers with optimum solutions. Our focus is on mixed-signal ASIC and IP design, complete solutions for integrated sensor systems, development of intelligent design flows for automated analog design as well as on design solutions for increasingly complex electronic systems. Here we can provide our customers with designs in ultra-deep sub-micron-technologies e.g. 22nm FDSOI. Whether for industrial, communications, automotive or any other applications, we are your partner from the idea to the final product.

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CAMPUS
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Dresden, Germany

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GLOBALFOUNDRIES is a leading full-service semiconductor foundry providing a unique combination of design, development, and fabrication services to some of the world's most inspired technology companies. With a global manufacturing footprint spanning three continents, GLOBALFOUNDRIES makes possible the technologies and systems that transform industries and give customers the power to shape their markets.

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For more information, visit <https://www.globalfoundries.com>.

EP 3

HiPEAC – European Network on High Performance and Embedded Architecture and Compilation

HiPEAC

UGENT - ELIS Technologiepark-

Zwijnaarde 15

9052 Gent

Belgium

Contact: Vicky Wandels

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M vicky.wandels@gent.beW www.hipeac.net

Since 2004, the HiPEAC (High Performance and Embedded Architecture and Compilation) project has provided a hub for European researchers in computing systems; today, its network, the biggest of its kind in the world, numbers around 2000 specialists. HiPEAC members include both top-class researchers and industry representatives who want to shape the development of computing systems. Members benefit from a series of advantages, including industry insight, training, recruitment and peer-to-peer interaction. HiPEAC organizes four networking events per year: the HiPEAC conference, two Computing Systems Weeks and a summer school. As part of the HiPEAC community, you can also contribute to the biennial HiPEAC Vision, an influential roadmap which informs European technology research policy areas. In addition, the project offers training, mobility support, help in finding excellent computing candidates and dissemination support. The latest incarnation of the project, HiPEAC 5, began on 1 December 2017 and is delivered by 13 partners, led by Ghent University. It is funded by the European Union's Horizon 2020 research and innovation programme under grant agreement no. 779656. To join for free email membership@hipeac.net. For further information visit www.hipeac.net/industry and don't forget to visit our stand here at DATE 2018!

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IDT Europe GmbH

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01109 Dresden
Germany

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IDT Europe GmbH is a Dresden, Germany-based, automotive-certified company acquired by Integrated Device Technology, Inc. in 2015 as former ZMDI, and which operates today as the IDT Automotive and Industrial Division.

IDT's market-leading products in RF, timing, wireless power transfer, serial switching, interfaces and sensing solutions are among the company's broad array of complete mixed-signal solutions. These products are used for development in areas such as 4G infrastructure, network communications, automotive and industrial, cloud datacenters and power management.

The company develops a wide range of robust sensor solutions, leveraging its many years of experience delivering products to automotive customers. With autonomous driving triggering the next wave of connectivity for vehicles, new technologies and solutions will be required to enable this revolution in transportation. IDT's wide spectrum of technologies includes, but is not limited to:

- Sensor platforms (e.g. for pressure sensing, gas sensing, optical sensing, position sensing etc) including flexible sensor signal conditioner products
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Due to its extensive experience in circuit development, IDT is capable to offer ICs for very demanding applications, in some cases operating at temperatures up to +160° C and with voltages from 0.85 to 40 volts and is perfectly positioned to provide system solutions, including key enabling technologies, to its customers.

IDT has approximately 1500 employees, and serves its customers with sales offices and design centers throughout Europe (Bulgaria, Finland, France, Germany, Italy, Netherlands, Sweden, United Kingdom), Asia (China, Japan, Korea, Malaysia, Singapore, Taiwan), and North America (United States, Canada).

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Behavioural Modelling & Analysis • Physical Analysis • Hardware/Software Co-Design • PCB & MCM Design

Test:

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Hardware:

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IEEE Council on Electronic Design Automation (IEEE CEDA)

Contact: Kartik Patel
 M admin@ieee-ceda.com
 W www.ieee-ceda.org

The Council on Electronic Design Automation (CEDA) was established to foster design automation of electronic circuits and systems at all levels. The Council's field of interest spans the theory, implementation, and use of EDA/CAD tools to design integrated electronic circuits and systems. This includes tools that automate all levels of the design, analysis, and verification of hardware and embedded software up to and including complete working systems. CEDA enables the exchange of technical information by sponsoring publications, conferences and workshops and through local chapters for volunteers activities. If you are interested please contact admin@ieee-ceda.com or check our website for more information about our activities and how to become a member for free.

BOOTH 7

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System-Level Design:

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Services:

Design Consultancy • Training

Test:

System Test

The European University Program (EUP) was established in 1994, with the objective of facilitating the inclusion of world-class embedded processing and analog technologies into electrical engineering research and course curricula.

Educators

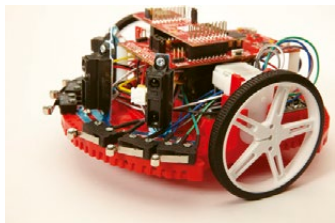
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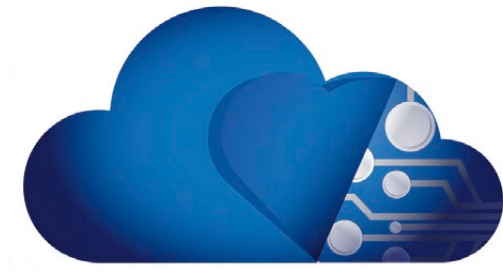
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The mission of the EU-funded TETRAMAX innovation action is to build on three activity lines in the domain of Customized Low-Energy Computing (CLEC) for Cyber-Physical Systems and the Internet of Things: (1) stimulating, co-funding, and evaluating different cross-border Technology Transfer Experiments (TTX) via innovative CLEC technologies to first-time users and broad markets in European ICT industries, (2) building and leveraging a new European CLEC competence center network, offering technology brokerage, one-stop shop assistance and CLEC training to SMEs and mid-caps, with a clear path towards new regional Digital Innovation Hubs (DIH), and (3) paving the way towards self-sustainability. Within the framework of a variety of open calls for application of TTX, the immediate ambition of TETRAMAX is to support 50+ industry clients all over Europe with innovative technologies, leading to an estimated revenue increase of €25m based on 50+ new or improved CLEC-based products, 10+ entirely new businesses/SMEs initiated, as well as 30+ new permanent jobs and significant cost savings in product manufacturing. Being the leading European DIH for CLEC, TETRAMAX will accelerate digitalization within European industries. In the long term, TETRAMAX will be the trailblazer towards a reinforced and sustainable ecosystem infrastructure, providing CLEC competence, services and a continuous innovation stream at European scale, yet with strong regional presence as preferred by SMEs.

The TETRAMAX project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement number 761349.

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Awards	040
Co-Located Workshops	141
Contact Event Secretariat	020
DATE At A Glance	021-028
DATE Executive Committee	168-169
DATE Party Networking Event	013
Event Overview	020
Executive Sessions	015
Exhibition Guide	143
Exhibition Theatre Programme	120-121
Friday Workshops	104-119
Fringe Technical Meetings	138-141
General Information	011-014
Interactive Presentations	014
Keynote Addresses	006-009
Media Partners	002
Opening Plenary and Awards Presentation	040
Programme Guide	001
Special Day – Wednesday: Future and Emerging Technologies	016
Special Day – Thursday: Designing Autonomous Systems	017
Special & EU Sessions	018-019
Sponsors	C02
Technical Programme	039-103
Technical Programme Topic Chairs	170-172
Tutorials	029-037
University Booth Demonstrations	122-136
Vendor Exhibition	144-166
Venue	011
Venue Plan	C04
Welcome	004-005

Scope of the Event

The 22nd DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers, and vendors, as well as specialists in hardware and software design, test, and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems, and embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days, and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design, and test communities. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website: www.date-conference.com.

**CONFERENCE
& EXHIBITION**
MARCH 25 – 29, 2019
Firenze Fiera, Florence, Italy

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, EDA algorithms and tools, testing of electronic circuits and systems, embedded software, application design, and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis, and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Green Computing Systems and Applications
- Temperature-Aware Design
- Temperature Modeling and Management
- Emerging Technologies for Computing Systems
- Emerging Memory Technologies and Applications
- Formal Methods and Verification
- Network-on-Chip
- Architectural and Microarchitectural Design
- Reconfigurable Computing
- Physical Design and Verification
- Analog and Mixed-Signal Circuits and Systems
- Interconnect and Packaging Modeling
- Communication, Consumer, and Multimedia Systems
- Transportation Systems
- Medical, Healthcare, and Assistive Technology Systems
- Energy Generation, Recovery, and Management Systems
- Secure Systems
- Reliable and Dependable Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation, and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time and Networked Systems
- Compilers and Code Generation for Embedded Systems
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software and Optimization for MPSoCs, Many-core, GPU-based, or Heterogeneous Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 9, 2018,

via: www.date-conference.com

Papers can be submitted either for standard oral presentation or for interactive presentation. The Program Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.

Chairs

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VENUE PLAN

International Congress Center Dresden (ICCD)

