ADVANCE PROGRAMME

www.date-conference.com

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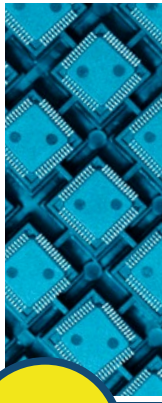

20th EDITION

DATE 17

Design, Automation and Test in Europe

March 27 – 31, 2017, Lausanne, Switzerland

DATE 2017 SPONSORS

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Electronic System Design Alliance

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European Electronic Chips & Systems design Initiative

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MEDIA PARTNERS

The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found on-site.

EDA Confidential

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

www.aycinena.com

EDACafé

EDACafe.Com is the #1 EDA web portal. Thousands of IC, FPGA and System designers visit EDACafé.com to learn the latest news and research design tools and services. The sites attract more than 75,000 unique visitors each month and leverages TechJobsCafé.com to bring you job opportunities targeted to engineering and design. And daily e-newsletters reach more than 40,000 engineering professionals. For more details visitwww.EDACafe.com and www.TechJobsCafe.com.

www.edacafe.com

Engineering & Technology

Engineering & Technology is packed with articles on the latest technology covering the areas of communications, control, consumer technology, electronics, IT, manufacturing & power engineering. It is Europe's largest circulation engineering magazine, published monthly & offers a global circulation of over 140,000 copies to more than 100 countries & a high pass-on readership.
Each member of the Institution of Engineering & Technology

(IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users.
With its HQ in London & regional offices in Europe, North America & Asia-Pacific, the Institution of Engineering & Technology provides a global knowledge network to facilitate the exchange of ideas & promote the positive role of technology around the World. The Institution of Electrical Engineers, dating from 1889, became the Institution of Engineering & Technology in 2006. It now organises more than 120 conferences & other events each year whilst providing professional advice & briefings to industry, education & governments.

www.eandtmagazine.com

SEMICON Europa 2017: New Opportunities in a Mature Industry Environment

November 14-17, 2017, Messe München, Munich, DE

The SEMICON Europa technology and business programs address the critical issues and challenges facing the microelectronics industries and provide the information, education, and guidance that needed to move your innovations and products to market. Connect with the facts.

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- It is the premier European showcase for business and exploration in areas like flexible hybrid electronics, MedTech, automotive, imaging, design and fabless, SMART Manufacturing, materials, power electronics, and more.
- 70% of visitors are involved in buying and investment decisions while 45% of visitors represent engineering job functions

Detailed information on **semiconeuropa.org**

WELCOME TO DATE 2017

Dear Colleague,

We proudly present to you the Advance Programme of **DATE 2017!** 2017 is a special year for the world's favourite electronic systems design and test conference, as we celebrate its **20th edition.** This year, the DATE conference will be held for the first time in Switzerland, at the SwissTech Convention Center on the EPFL campus in Lausanne, from March 27 to 31, 2017. This edition includes an international exhibition for electronic design, automation and test with special emphasis on the areas of Internet of Things (IoT), Cloud Computing, and Wearables and Smart Medical Devices, covering from system-level hardware and software implementation right down to integrated circuit design.

For the 20th successive year, DATE has prepared an exciting technical programme. Out of a total of 794 paper submissions received, a large share (42%) is coming from authors in Europe, 32% of submissions are from America, 25% from Asia, and 1% from the rest of the world. This clearly demonstrates DATE's international character, its global reach and impact.

With the help of 336 members of the Technical Program Committee who carried out 3187 reviews (about four per submission), finally 193 papers (24%) were selected for regular presentation and 92 additional ones (11.5%) for interactive presentation.

The DATE event will start on Monday with **9 in-depth technical tutorials** which will be given by leading experts in their respective fields, with topics on Design Solutions, Emerging Technologies, System Development and Verification, and Dependability.

The **plenary keynote speakers on Tuesday** are Dr. Arvind Krishna from IBM who will talk about "Design Automation in the Era of AI and IoT: Challenges and Pitfalls" and Dr. Doug Burger from Microsoft to talk about "A New Era of Hardware Microservices in the Cloud". In addition, a keynote lecture from Prof. Giovanni De Micheli (Professor at EPFL and Director of Nano-Tera.ch) will be given on Tuesday on "Distributed Systems for Health and Environmental Monitoring" within the Nano-Tera.ch initiative. On the same day, the **Executive Track,** including one Executive Panel Session and three Innovative Technologies & Applications (IT&A) Sessions, offers a series of business panels discussing hot topics. Executive speakers from companies leading the design and automation industry will address some of the complexity issues in electronics design and discuss about the advanced technology challenges and opportunities.
The main conference programme from Tuesday to Thursday includes 79 technical sessions organized in parallel tracks from the four areas
D – Design Methods and Tools
A – Application Design
T – Test and Robustness
E – Embedded Systems Software
and from several special sessions on Hot Topics, such as, emerging technologies, low power challenges and approximate computing for IoT devices, security-aware design in cyber-physical systems, new benchmarking methods and applications for emerging devices, circuits, and architectures, methodologies to design and manage exascale computing system technologies, as well as results and lessons learned from European projects. A special session is dedicated to Ralph Otten, pioneer of physical design, who prematurely died in an accident.

WELCOME TO DATE 2017

David Atienza

Giorgio Di Natale

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: **Designing Electronics for the Internet of Things Era** and **Designing Wearable and Smart Medical Devices,** each having a full programme of keynotes, panels, tutorials and technical presentations.

During the Special Day on "Electronics for the Internet of Things Era" on **Wednesday,** Dr. Keith Willett from Merck Serono will talk about "Internet of Everything is our Opportunity".
On **Thursday, a keynote** from Dr. Sani Nassif from Radyalis LLC will be given about "The Engineering to Medicine Metamorphosis" in the frame of the Special Day on "Wearable and Smart Medical Devices".

Additionally, there is a good coverage of topics in **Interactive Presentations** which are organized into five IP sessions.

To inform attendees on commercial and design related topics, there will be a full programme in the **Exhibition Theatre** which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. The conference is complemented by an **exhibition, running for three days** (Tuesday – Thursday), which provides a unique networking opportunity and states the perfect venue for industries to meet University Professors to foster University Programme and especially for PhD Students to meet future employees. The full list of applied exhibitors and sponsors can be found here: www.date-conference.com/exhibition/exhibitors-sponsors

On Friday, the last day of the DATE week, **8 full-day workshops** cover a large number of hot topics, including IoT Design, Emerging Memories and Interconnections Technologies, Design of Future Autonomous Cars, and Engineering Multi-Scale Systems for Health, Energy and the Environment.

For further information please visit: www.date-conference.com

We wish you an exciting and memorable DATE 2017, a successful exhibition visit and an entertaining DATE 20th edition party on Wednesday evening, which will take place in the extraordinary scenario of the Olympic Museum in Lausanne, overlooking the Lake Geneva and the Swiss-French Alps.

DATE 2017 General Chair
David Atienza
EPFL, CH

DATE 2017 Programme Chair
Giorgio Di Natale
LIRMM, FR

Arvind Krishna

0915 – 0945 Auditorium A

1.1.1

Design Automation in the Era of AI and IoT: Challenges and Pitfalls

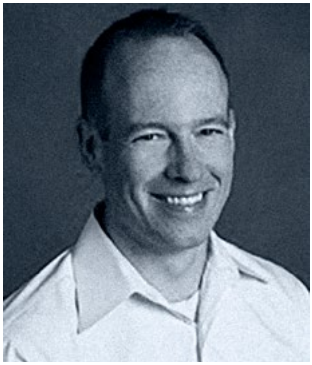
Arvind Krishna, Senior Vice President, Hybrid Cloud and Director, IBM Research, US

The AI and IoT revolutions are twin phenomena that are reshaping business models, industries, and society. If we are to maximize their potential, we must overcome significant technical challenges with the help of the Design Automation and Test Community.

First, new computer architectures are required to accelerate solutions driven by cognitive computing, the term given to a comprehensive set of AI capabilities that includes not just machine learning but also data ingestion, data privacy, learning, reasoning, natural language, and conversation. These architectures must support each of these new technologies and manage extreme, cognitive workloads marked by unprecedented volumes of structured and unstructured data. This challenge poses important questions for the Design Automation and Test community about what new approaches can be taken.

A similar challenge is inherent in the rapid development of IoT, where the span of computing architecture varies from extremely low power constraints, limited bandwidth, and sporadic access at the "edge" of the network to the nearly infinite power and compute of data centers. This raises the question of how to maximize the design and placement of IoT systems, which will have to function for extended periods of time (up to ten years or more, like a pacemaker). Unlike smartphones, these systems can't simply be disposed of, which raises significant security concerns.

In his talk exploring these challenges, Dr. Krishna will emphasize that solutions can only come from an integrated hardware-software co-design approach. He will also highlight some of the leading-edge technologies IBM Research is developing to drive further innovation in the computing stack as the era governed by Moore's law comes to a close.



Doug Burger

0945 – 1015 Auditorium A

1.1.2

A New Era of Hardware Microservices in the Cloud

Doug Burger, Distinguished Engineer, Director of Client & Cloud Apps, Microsoft Research, US

The Cloud is causing a major shift in both the business ecosystem and system infrastructures. The major hyperscale providers are building out highly-interconnected, worldwide computers at a scale that allows them to make significant first-party investments. This verticalization allows them to make cross-layer architectural changes more rapidly than would the old horizontal model. A second trend is the emergence of ultra-low latency requirements in the Cloud, moving storage, networking, and services from the millisecond to the microsecond regime. In this talk, I will describe how these architectural shifts are enabling the emergence of specialized hardware in datacenters, that enable services to be operated in the microsecond regime. On FPGAs, GPUs, and ASICs, these services can run with no CPU intervention, allowing much lower latencies and better cost structures than previously possible for key services such as deep learning. Over time this transition will enable a much broader collection of hardware IP to run at scale in the Cloud.

TUESDAY KEYNOTE ADDRESS

Giovanni De Micheli

1350 – 1420 Garden Foyer

3.0

Precision Medicine: Where Engineering and Life Science meet

Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH

As we witness the relentless growth of computing power, storage capacity and communication bandwidth, we also see a major trend in bio-medical sciences to become more quantitative and amenable to benefit from the support of electronic systems. Moreover, societal and economic needs push us to develop and adopt health-management approaches that are more effective, less expensive and flexible enough to be personalized to individual and community needs.

Within this frame, precision medicine promises to better society by applying engineering technology to personalized health, with devices that are in/on the body and ubiquitously connected. Examples from the Swiss-wide Nano-Tera.ch program will show various techniques related remote patient monitoring, emergency care as well as routine care. These examples show the advantages that stem from organized and optimized means to quantify clinical data, handle large data sets as well as controlling and personalizing therapy and drug administration.

Electronic design automation is a key technology to realize systems for precision medicine. Examples of specific EDA tools and methods encompass physical design of integrated sensors and their coupling to electronics, simulation of complex systems with bio-chemical stimuli, synthesis of decision making circuitry based on plurality of inexact inputs, policies design for therapies exploiting on-line data acquisition, and verification of life-critical applications under broadly-varying and unpredictable input conditions.

Overall, precision medicine represents an important and large market opportunity. EDA is a necessary underlying technology to realize the promises of better and less expensive care for everyone.

Keith Willett

1350 – 1420 Garden Foyer

7.0 Internet of Everything is our Opportunity

Keith Willett, Director of Software Engineering for Merck Serono, CH

Merck Serono is working to revolutionize patient care and doctor assist through utilization of technology that is built of the Internet of Everything. Using global resources to consolidate medical devices under a single platform that will store, analyze and recommend patient care to physicians, Merck is leveraging the Internet of Everything to improve patient care.

The IoE is not limited to medical devices, as everything from automobiles to light bulbs are looking for ways to connect to the Internet. These devices gather, store and analyze data to improve the user experience and create value for people and businesses that have yet to be recognized. However, connecting so many products will cause an increased strain on the network infrastructures, and most importantly expose personal information to potential threats; if not managed correctly. All companies connecting devices are having similar problems and are working to solve these issues.

As the Internet of Everything continues to evolve, critical strategies will need to be in place for all companies to be successful. This presentation will discuss the strategies companies need to play in this space and how collaboration and cooperation will become more common in IoE.

THURSDAY KEYNOTE ADDRESS

Sani R. Nassif

1320 – 1350 Garden Foyer

11.0 The Engineering to Medicine Metamorphosis

Sani R. Nassif, Chief Engineering Officer, Radyalis LLC, US

We EDA engineers are justifiably proud of the tremendous success that integrated electronics has enjoyed over the last 50 years. After all the world has been irrevocably changed by the pervasive connectivity and computing capability we have enabled. Today's smart devices are just the beginning of an avalanche of "intelligence" that will be enabled by the internet of things and further change our lives for the better. But it can sometimes be difficult to explain to a layperson what part we have played in this narrative, somehow a 2% improvement in routing density or simulation accuracy sounds quite far from "the next iPhone". As technology slows down, matures, and the industry consolidates, we are presented with opportunities for applying our talents for the analysis, modeling, optimization and solution of difficult large scale problems in adjacent fields. This talk is about one such opportunity in the area of radiation therapy, where Medical Physicists work hand-in-hand with Oncologists to provide life-saving treatments for Cancer. Making the transition from EDA to Medicine required some significant sacrifices and humility -but the end result is a commercial and scientific success and a far greater level of relevance to people's lives.

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2017. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website **www.date-conference.com**

Dates and Venue

The conference will take place from 27 to 31 March, 2017 in the SwissTech Convention Center (STCC).

SwissTech Convention Center
Quartier Nord de l'EPFL
Route Louis-Favre 2
1024 Ecublens, CH
www.stcc.ch/en/home

The accompanying exhibition is scheduled from 28 to 30 March, 2017, and will take place in the heart of the conference area, directly next to the session rooms, hosting the coffee break area as well.

Interactive Programme Online

A fully interactive DATE 2017 programme is available on the website **www.date-conference.com** where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

Free wireless internet access is available on-site throughout the whole congress center during the entire DATE week. The WLAN login code will be provided at the registration desk upon arrival (entrance foyer of the congress center). There is also Eduroam coverage, and DATE attendees can directly use their own credentials to connect to the network.

Proceedings

The conference proceedings are available on memory stick on-site, which will be given together with the conference bag (to delegates who registered for the full conference or a day ticket only).

WHOVA Conference App

The WHOVA App can be downloaded via the following link or in the Apple/Google stores for free: **https://whova.com/download**
Please install the app and search for the conference
"DATE 2017" → Password: "DATE"

Online Conference Evaluation via the WHOVA App ("survey" button): every fully registered delegate who fills in the online conference evaluation via the app, will receive one of the exclusive DATE collector mugs at the registration desk (when showing the confirmation page).

Coffee Break in the Exhibition Area

On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks at the below-mentioned times in the exhibition area.

Lunch Break in the Garden Foyer

On all conference days (Tuesday to Thursday), a buffet lunch will be offered in the Garden Foyer, in front of the session rooms. Kindly note that this is restricted to conference delegates possessing a lunch voucher only. When entering the lunch break area, delegates will be asked to present the corresponding lunch voucher of the day. Once the lunch area has been left, re-entrance is not allowed for the respective lunch.

Tuesday, March 28, 2017	
Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Keynote Lecture in "Garden Foyer"	*1350 – 1420*
Coffee Break	1600 – 1700
Wednesday, March 29, 2017	
Coffee Break	1000 – 1100
Lunch Break	1230 – 1430
Keynote Lecture in "Garden Foyer"	*1350 – 1420*
Coffee Break	1600 – 1700
Thursday, March 30, 2017	
Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Keynote Lecture in "Garden Foyer"	*1320 – 1350*
Coffee Break	1530 – 1600

Welcome Reception & PhD Forum

Mon, March 27, 2017

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2017 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 27, 2017, from 1800 – 2100 in the Campus Foyer (Grätzel, First Level) of the SwissTech.
The PhD Forum is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

Exhibition Reception

Tue, March 28, 2017

The Exhibition Reception will take place on Tuesday, March 28, 2017, from 1830 – 1930 in the exhibition area (Garden Foyer, Ground Level), where free drinks for all conference delegates and exhibition visitors will be offered. All exhibitors are welcome to also provide drinks and snacks for the attendees.

DATE Party – Networking Event

Wed, March 29, 2017

The highlight of the DATE week will again be the DATE Party, which offers the perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. Thus, it states one of the main networking opportunities during the DATE week. In addition, this year the DATE Best Paper Awards and Best IP Award will be given during the DATE Party. Also, there will be special prizes for the best pictures taken by the DATE attendees in the 20 editions of DATE so far. **Do not miss the key event at DATE 2017!**
The party is scheduled on March 29, 2017, from 1900 to 2300, and will take place in Lausanne's most outstanding museum location: The Olympic Museum. It is beautifully located in the heart of the city, with magnificent views over the Lake Geneva and the Swiss-French Alps. Since its renovation at the end of 2013, it now hosts more than 3,000 sqm of exhibition space and a new scenography which perfectly reflects the idea and spirit behind and how rich and diverse Olympism is. Some of the themes highlighted include sports, history, culture, design, sociology, and technology. During the evening, all delegates will have the chance to visit the different expositions for free.
Please kindly note that it is not a seated dinner. A continuous flying buffet and drinks will be served during the whole evening.
All delegates, exhibitors and their guests are invited to attend the party. Please be aware that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Price for extra ticket: CHF 80.00 per person.

How to get there

→ www.olympic.org/museum/visit/practical-information/getting-here

By public transportation:
Take the metro line M1 from the SwissTech convention center (EPFL stop) to the stop Lausanne-Flon. Change to metro line M2 to stop Ouchy-Olympique.
Check times here: www.sbb.ch/en/home.html or www.t-l.ch/en/

By car:
Take the A9 motorway, Maladière exit and continue straight until Ouchy. The underground car park at the Place de la Navigation in Ouchy is located just 400m from the museum. Street parking in the disc parking zones ("blue zones") and disabled parking at the museum's north entrance (Elysée entrance) are also available.

Walking distance:
10 minutes from the metro M2 Ouchy-Olympique
10 minutes from the landing CGN Ouchy
20 minutes from the train station Lausanne (Gare)

Interactive Presentations

(sponsored by the Cadence Academic Network)

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress, which may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.
To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the foyer of the Conference Level in 30-minute time slots on the following days:

Tuesday, March 28, 2017

IP Session 1	Garden Foyer (in front of rooms 4A and 5A)	1600 – 1630

Wednesday, March 29, 2017

IP Session 2	Garden Foyer (in front of rooms 4A and 5A)	1000 – 1030
IP Session 3	Garden Foyer (in front of rooms 4A and 5A)	1600 – 1630
Presentation of the Best IP Award during the DATE Party	Olympic Museum, TOM café	2000

Thursday, March 30, 2017

IP Session 4	Garden Foyer (in front of rooms 4A and 5A)	1000 – 1030
IP Session 5	Garden Foyer (in front of rooms 4A and 5A)	1530 – 1600

Organisers: Giovanni De Micheli, EPF Lausanne, CH
Marco Casale-Rossi, Synopsys, IT

DATE 2017 will feature an Executive and Innovative Technologies & Applications (IT&A) Track, with presentations by representatives leading electronic companies, applied research organizations, and universities around the world. The programme will start on Tuesday March 27 with an Executive Panel Session, which will be held immediately after the Opening Session, and will be followed by two IT&A Sessions. The last IT&A Session will be held on Wednesday March 29. Each session will feature 3-5 speakers and run in parallel to the technical conference tracks. All the sessions will first provide each speaker with a timeslot to present his/her vision, followed by a Q&A. The Track should offer prospective attendees valuable information about the vision of the high-profile speakers with regard to the technology and industry roadmap.

2.1 **EXECUTIVE PANEL SESSION:**
The Electronics Innovation Landscape: Opportunities, Challenges and Strategies

See Page 37

3.1 **IT&A SESSION:**
Parallel Ultra-Low-Power Computing for the IoT: Applications, Platforms, Circuits

See Page 41

4.1 **IT&A SESSION:**
The Emergence of Silicon Photonics: From High Performance Computing to Data Centers and Quantum Computing

See Page 47

6.2 **IT&A SESSION:**
Panel: Ultra-Low-Power (ULP) Autonomously Powered Systems

See Page 58

A TRIBUTE TO RALPH OTTEN — Tue, March 28, 2017

3.9 **A tribute to Ralph Otten**
Organiser: Giovanni De Micheli, EPFL, CH

World renowned leaders in Physical Design will talk about accomplishments in this field over the last four decades, as a tribute to Ralph Otten, pioneer of this field who prematurely died in an accident.

See Page 45

SPECIAL DAY — WEDNESDAY

Organisers and Chairs: Marilyn Wolf, Georgia Tech, US
Andreas Herkersdorf, TU Muenchen, DE

Designing Electronics for the Internet of Things Era

Our society is evolving to a point where objects and people will be almost permanently connected and exchanging information. This scenario, called the Internet of Things (IoT), is the result of the convergence in the evolution and integration of communication, computing, storage and sensing technologies. The potential influence of IoT in our daily life is enormous – Gartner Inc. expects 26 billion devices to be on the Internet of Things (IoT) by 2020, other forecasts even project 50 billion by the same time frame. IoT is perceived as key enabling technology for smart-X (cities, households, buildings, fabs (industry 4.0), mobility, health, energy) applications and has also been highlighted in the 2014 (US) President's National Security Telecommunications Advisory Committee report and by the NSF. On the other hand, it is also clear that IoT will require radically new approaches to high-performance, small(est) form factor and lowest cost, lowest energy computing platforms, memory and sensor technology, design methods as well as ICT infrastructure integration. Robust and secure design inside and outside of IoT devices / systems are equally important properties and objectives.
This special day will shed light on major challenges related to IoT microelectronics design, novel paradigms for data acquisition and fusion, as well as analysis and storage of the large volume of collected information. Internationally renowned experts from industry, start-ups and academia share their expertise and experience on how the progress in technologies and applications of IoT can be nurtured and cultivated for the benefit of society.

5.1 IoT Day: IoT Perspectives

See Page 52

6.1 IoT Day Hot Topic Session: IoT Enabling Technologies

See Page 58

7.0 LUNCH TIME KEYNOTE SESSION

See Page 62

7.1 IoT Day Hot Topic Session: IoT Deployment

Ten Cents SoC Challenge posters are being introduced as IPs
See Page 62

8.1 IoT Day Hot Topic Session: Challenges and Potentials for IoT Rollout

See Page 68

Organisers and Chairs: José L. Ayala, Universidad Complutense de Madrid, ES
Chris Van Hoof, IMEC, BE

Designing Wearable and Smart Medical Devices

The technological convergence of portable consumer electronics such as smartphones, smart watches and fitness devices with that of professional medical equipment such as pulse oximetry, ECG and Glucose meters as well as ultrasound scanners and kidney diagnostics, is increasingly blurring the lines between equipment designed for practitioners and devices used by consumers. The benefits of wearable and portable medical devices are clear. Wearables make patient data readily accessible and they may reduce the frequency of visits to a doctor and in doing so alleviate the burden on our healthcare system. As well as this, it is becoming cheaper to produce wearable medical devices that fulfil the function traditionally limited to large and expensive medical devices in hospitals. But designing wearable and smart medical devices is more than that; it is the convergence of the applied research, the clinical data, the work posed by practitioners and engineers, and the continuous effort from the industry in electronic integration. In this Special Day we will cover all these aspects, with a clear and explicit target on the application domain and the end-user (and patients). Novel medical devices will be presented, advanced data and processing techniques will be described, and the words from the industry will always accompany the academic world. Join us in this challenging goal!

9.1 **Wearable and Smart Medical Devices Day: New tools and devices for chronic and acute care**

See Page 73

10.1 **Wearable and Smart Medical Devices Day: Diagnosis and prevention systems**

See Page 79

11.0 **LUNCH TIME KEYNOTE SESSION**

See Page 84

11.1 **Wearable and Smart Medical Devices Day: HW and SW design constraints in medical devices**

See Page 89

12.1 **Wearable and Smart Medical Devices Day: Industry panel: Industrial challenges for tomorrow's medical devices and tools**

See Page XX

SPECIAL & EU SESSIONS

Special Session Chairs: Giovanni De Micheli, EPFL, CH
Marco Casale-Rossi, Synopsys, IT
EU SESSIONS Chair: Lorena Anghel, TIMA Laboratory, FR

The following Special Sessions have been organized, which should be of great general interest, and make a technical status about topics such as high-performance computing, IoT, spintronic, quantum computing, EDA, ultra-low-power systems, self-aware systems, and secure cyber-physical systems.

2.7 EU Project Special Session: from Secure Clouds to reliable and variable HPC

Chair: Lorena Anghel, TIMA Laboratory, FR

See Page 40

3.2 Hot Topic Session: New Benchmarking Vectors for Emerging Devices, Circuits, and Architectures: Energy, Delay, and ... Accuracy

Chairs: Xiaobo Sharon Hu, University of Notre Dame, US
Pierre-Emmanuel Gaillardon, The University of Utah at Salt Lake City, US

See Page 42

4.5 Hot Topic Session: On How to Design and Manage Exascale Computing System Technologies

Organiser: Donatella Sciuto, Politecnico di Milano, IT

See Page 50

5.3 Hot Topic Session: I'm Gonna Make an Approximation IoT Can't Refuse - Approximate Computing for Improving Power Efficiency of IoT and HPC

Organiser: Christian Enz, EPFL, CH

See Page 53

5.5 Hot Topic Session: Spintronics-based Computing

Organisers: Lionel Torres, LIRMM, CNRS/University of Montpellier, FR
Weisheng Zhao, Beihang University, CN

See Page 54

6.5 Hot Topic Session: Memristor for High Performance Computing: Myth or Reality?

Organisers: Koen Bertels, Delft University of Technology, NL
Said Hamdioui, Delft University of Technology, NL

See Page 60

6.6 **Industrial Experiences & EU Projects**
Chairs: Mario Diaz Nava, ST Microelectronics, FR
Eugenio Villar, University of Cantabria, ES
See Page 60

7.5 **Hot Topic Session: The Engineering Challenges for Quantum Computing**
Organiser: Koen Bertels, QuTech & Computer Engineering Lab, NL
Carmen G. Almudéver, QuTech & Computer Engineering Lab, NL
See Page 64

8.2 **Hot Topic Session: No Power? No Problem! Exploiting Non-Volatility in Energy Constrained Environments**
Organisers: Xiaobo Sharon Hu, University of Notre Dame, US
Michael Niemier, University of Notre Dame, US
See Page 68

8.6 **Hot Topic Session: Self-aware Systems: Concepts and Applications**
Organiser: Nikil Dutt, UC Irvine, US
Axel Jantsch, TU Wien, AT
See Page 71

9.3 **Hot Topic Session: Security in Cyber-Physical Systems: Attacks All The Way**
Organiser: Anupam Chattopadhyay, Nanyang Technological University, SG
Muhammad Shafique, CARE-Tech, TU Wien, AT
See Page 74

10.2 **Hot Topic Session: EDA as an Emerging Technology Enabler**
Organiser: Pierre-Emmanuel Gaillardon, The University of Utah at Salt Lake City, US
Mathias Soeken, EPFL, CH
See Page 80

11.8 **Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs**
Organiser: Andy M. Tyrrell, University of York, GB
Lukas Sekanina, Brno University of Technology, CZ
See Page 112

12.8 **Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology**
Organiser: Seetal Potluri, Technical University of Denmark, DK
Paul Pop, Technical University of Denmark, DK
See Page 113

EVENT OVERVIEW

MONDAY

- Educational Tutorials
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

TUESDAY

- Opening Session: Plenary, Awards Ceremony & Keynote Addresses and Keynote Addresses
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Executive and IT&A Sessions
- Lunchtime Keynote
- University Booth
- Fringe Meetings
- Exhibition Reception

WEDNESDAY

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on "Designing Electronics for the Internet of Things Era" and Keynote
- University Booth
- Fringe Meetings
- DATE Party – Networking Event

THURSDAY

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on "Designing Wearable and Smart Medical Devices" and Keynote
- University Booth
- Fringe Meetings

FRIDAY

- Special Interest Workshops

CONTACTS

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MONDAY 27 MARCH, 2017

0800 – 0930	Registration and Tutorial Welcome Refreshments Garden Foyer				
Breaks	1100-1130 Morning Coffee Break 1600-1630 Afternoon Coffee Break				
	4BC		3A	3B	3C
0930 – 1300	M01 Nano-Tera.ch | Data science techniques and machine learning for EDA		M03 Emerging Technologies | 3D Integration: Quo Vadis?	M04 System Development and Verification | Developing Next-Generation Embedded Systems: Functional Reactive Programming, Formal Verification, and Real-Time Virtual Resources	M05 Dependability | From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test
1300 – 1430	Lunch Break				
1330	Conference registration begins				
	4BC	4A	3A	3B	3C
1430 – 1800	M06 Nano-Tera.ch | Next 1000x Gains: from Clouds to IoT Systems	M07 Design Solutions | Stochastic Computation: the Hypes and the Hopes	M08 Emerging Technologies | Is energy wearable?	M09 System Development and Verification | An Industry Approach to FPGA and SOC System Development and Verification	M10 Dependability | Reliable VLSI Systems
1800 – 2100	Welcome Reception & PhD Forum Campus Foyer (Grätzel)				

STUDENT COMPETITIONS

Mon, March 27, 2017

On Monday, March 27, 2017, two student competitions will take place in parallel (a separate registration is required).

IEEE CEDA IoT Students Challenge

Room 5BC 0900 - 1800

Organizer: José L. Ayala, Universidad Complutense de Madrid, ES, jayala@ucm.es

SEL-EPFL and TI Student Competition on Apps development for handheld game consoles, tablets and smartphones

Room 5A 1600 - 1800

Organizer: Dominique Poissonnier, Texas Instruments Europe, FR, d-poissonnier@ti.com

For more information, please visit: **www.date-conference.com**

TUESDAY 28 MARCH, 2017

0730	Registration | Speaker's Breakfast, Garden Foyer			
0830 – 1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses, Auditorium A			
1030 – 1130	Exhibition and Coffee Break			
	Track 1	Track 2	Track 3	Track 4
	Auditorium A	4BC	2BC	3A
1130 – 1300	2.1 Executive Panel: The Electronics Innovation Landscape: Opportunities, Challenges and Strategies	2.2 Stochastic, Approximate and Neural Computing	2.3 Cache memory management for performance and reliability	2.4 Performance and Power Analysis
1300 – 1430	Lunch Break 1350 – 1420 3.0 LUNCH TIME KEYNOTE SESSION, Garden Foyer			
	5BC	4BC	2BC	3A
1430 – 1600	3.1 IT&A Session: Parallel Ultra-Low-Power Computing for the IoT: Applications, Platforms, Circuits	3.2 Hot Topic Session: New Benchmarking Vectors for Emerging Devices, Circuits, and Architectures: Energy, Delay, and ... Accuracy	3.3 Hardware Trojans and Fault Attacks	3.4 Guardbanding and Approximation
1600 – 1700	Coffee Break 1600 – 1630 IP1 Interactive Presentations, IP Area			
	5BC	4BC	2BC	3A
1700 – 1830	4.1 IT&A Session: The Emergence of Silicon Photonics: From High Performance Computing to Data Centers and Quantum Computing	4.2 Logic, Interconnects, Neurons: New Realizations	4.3 Efficient memory design	4.4 From functional validation to functional qualification
1830 – 1930	EXHIBITION RECEPTION in the Exhibition Area			

TUESDAY 28 MARCH, 2017

Registration | Speaker's Breakfast, Garden Foyer				0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses, Auditorium A				0830 – 1030
Exhibition and Coffee Break				1030 – 1130
Track 5	Track 6	Track 7	TRACK 8	
3C	5A	3B	Exhibition Theatre	
2.5 Reliability and Energy-Efficiency: Two Pillars of NoC Design	2.6 Advancing Test for Mixed-Signal and Microfluidic Circuits and Systems	2.7 EU Project Special Session: from Secure Clouds to reliable and variable HPC	2.8 Smart Medical Devices	1130 – 1300
1350 – 1420 Lunch Break 3.0 LUNCH TIME KEYNOTE SESSION, Garden Foyer				1300 – 1430
3C	5A	3B	Exhibition Theatre	
3.5 Low-power brain inspired computing for embedded systems	3.6 Mechanisms for hardware fault testing, recovery and metastability management	3.7 Scheduling and Optimization	3.8 Eco-Cloud TRACK 9 Auditorium A 1430 – 1600 3.9 A tribute to Ralph Otten	1430 – 1600
1600 – 1630 Coffee Break IP1 Interactive Presentations, IP Area				1600 – 1700
3C	5A	3B	Exhibition Theatre	
4.5 Hot Topic Session: On How to Design and Manage Exascale Computing System Technologies	4.6 Fault modeling, test generation and diagnosis	4.7 Process variation management for today's and tomorrow's computing	4.8 CV Fair DATE 2017	1700 – 1830
EXHIBITION RECEPTION in the Exhibition Area				1830 – 1930

PLENARY OPENING
EXECUTIVE AND IT&A
TUE KEYNOTE
D-TRACK
SPECIAL Prof. R. OTTEN
SPECIAL & EU SESSION
A-TRACK
IP SESSION
T-TRACK
EXHIBITION THEATRE
E-TRACK

WEDNESDAY 29 MARCH, 2017

0730	Registration | Speaker's Breakfast, Garden Foyer			
	Track 1	Track 2	Track 3	Track 4
	5BC	4BC	2BC	3A
0830–1000	5.1 IoT Day: IoT Perspectives	5.2 Emerging Computer Paradigms	5.3 Hot Topic Session: I'm Gonna Make an Approximation IoT Can't Refuse – Approximate Computing for Improving Power Efficiency of IoT and HPC	5.4 Solutions for efficient simulation and validation
1000 – 1100	Coffee Break 1000 – 1030 IP2 Interactive Presentations			
	5BC	4BC	2BC	3A
1100 – 1230	6.1 IoT Day Hot Topic Session: IoT Enabling Technologies	6.2 IT&A Session: Panel: Ultra-Low-Power (ULP) Autonomously Powered Systems	6.3 Security Primitives	6.4 High-performance Reconfigurable Computing
1230 – 1430	Lunch Break 1350 – 1420 7.0 LUNCH TIME KEYNOTE SESSION, Garden Foyer			
	5BC	4BC	2BC	3A
1430 – 1600	7.1 IoT Day Hot Topic Session: IoT Deployment	7.2 In-memory Computing and Security for Non-volatile Memory Technologies	7.3 Optimizing performance, energy and predictability via hardware/ software codesign	7.4 Advances in Logic Synthesis
1600 – 1700	Coffee Break 1600 – 1630 IP3 Interactive Presentations			
	5BC	4BC	2BC	3A
1700 – 1830	8.1 IoT Day Hot Topic Session: Challenges and Potentials for IoT Rollout	8.2 Hot Topic Session: No Power? No Problem! Exploiting Non-Volatility in Energy Constrained Environments	8.3 Secure Processor Components	8.4 Advanced systems for healthcare and assistive technologies
1900 – 2300	DATE Party | Networking Event, Olympic Museum			

WEDNESDAY 29 MARCH, 2017

Registration | Speaker's Breakfast, Garden Foyer				0730
Track 5	Track 6	Track 7	TRACK 8	
3C	5A	3B	Exhibition Theatre	
5.5 Hot Topic Session: Spintronics-based Computing	5.6 Reuse and Integration of Test, Debug, and Reliability Infrastructure	5.7 Schedulability Analysis		0830–1000
Coffee Break 1000 – 1030 IP2 Interactive Presentations				1000 – 1100
3C	5A	3B	Exhibition Theatre	
6.5 Hot Topic Session: Memristor for High Performance Computing: Myth or Reality?	6.6 Industrial Experiences & EU Projects	6.7 Model-Based Design and Verification of Real-Time Systems	6.8 HiPEAC: European Network on High Performance and Embedded Architecture and Compilation	1100 – 1230
Lunch Break 1350 – 1420 7.0 LUNCH TIME KEYNOTE SESSION, Garden Foyer				1230 – 1430
3C	5A	3B	Exhibition Theatre	
7.5 Hot Topic Session: The Engineering Challenges for Quantum Computing	7.6 Memory Reliability: Modeling and Mitigation	7.7 Resource management and analysis for embedded architectures	7.8 Smart Energy and Self-Powered Devices	1430 – 1600
Coffee Break 1600 – 1630 IP3 Interactive Presentations				1600 – 1700
3C	5A	3B	Exhibition Theatre	
8.5 Learning and Resilience Techniques for Green Computing	8.6 Hot Topic Session: Self-aware Systems: Concepts and Applications	8.7 Instruction-level and thread-level parallelism in embedded systems	8.8 Panel: Technology startups. Vision from Academia and Industry	1700 – 1830
DATE Party | Networking Event, Olympic Museum				1900 – 2300

Executive and IT&A

Special Day Session | Special & EU Session | IP Session | Exhibition Theatre

D-Track | A-Track | T-Track | E-Track

THURSDAY 30 MARCH, 2017

0730	Registration | Speaker's Breakfast, Garden Foyer			
	Track 1	Track 2	Track 3	Track 4
	5BC	4BC	2BC	3A
0830–1000	9.1 Wearable and Smart Medical Devices Day: New tools and devices for chronic and acute care	9.2 Emerging Schemes for Memory Management	9.3 Hot Topic Session: Security in Cyber-Physical Systems: Attacks All The Way	9.4 Design Space Exploration
1000 – 1100	Coffee Break 1000 – 1030 IP4 Interactive Presentations			
	5BC	4BC	2BC	3A
1100 – 1230	10.1 Wearable and Smart Medical Devices Day: Diagnosis and prevention systems	10.2 Hot Topic Session: EDA as an Emerging Technology Enabler	10.3 Side-Channel Attacks	10.4 Emerging Architectures for Reconfigurable Computing
1230 – 1400	Lunch Break 1320 – 1350 11.0 LUNCH TIME KEYNOTE SESSION			
	5BC	4BC	2BC	3A
1400 – 1530	11.1 Wearable and Smart Medical Devices Day: HW and SW design constraints in medical devices	11.2 Emerging Technologies for Future Memory Design	11.3 Exploiting Heterogeneity for Big Data Computing	11.4 Advances in Timing and Layout
1530 – 1600	Coffee Break IP5 Interactive Presentations			
	5BC	4BC	2BC	3A
1600 – 1730	12.1 Wearable and Smart Medical Devices Day: Industry panel: Industrial challenges for tomorrow's medical devices and tools	12.2 Advances in Microfluidics and Neuromorphic Architectures	12.3 Security Tools	12.4 Formal and Predictive Models for System Design

Registration | Speaker's Breakfast, Garden Foyer				0730
Track 5	Track 6	Track 7	TRACK 8	
3C	5A	3B	Exhibition Theatre	
9.5 Modeling and optimization of Internet-of-things (IoT) devices	9.6 Reliability and Optimization Techniques for Analog Circuits	9.7 Front-row seats for Temperature and Variability	9.8 The Internet of INSECURE Things	0830–1000
Coffee Break 1000 – 1030 IP4 Interactive Presentations				1000 – 1100
3C	5A	3B	Exhibition Theatre	
10.5 Emerging NoC Directions	10.6 Approximate computing and neural networks for novel communication and multimedia systems	10.7 Adaptive and Resilient Cyber-Physical Systems	10.8a Smart and Wearable Sensors for Health 10.8b IoT Edge Devices	1100 – 1230
Lunch Break 1320 – 1350 11.0 LUNCH TIME KEYNOTE SESSION				1230 – 1400
3C	5A	3B	Exhibition Theatre	
11.5 Smart Energy and Automotive Systems	11.6 Dependable microprocessors and systems	11.7 Formal Methods and Verification: Core Technologies and Applications	11.8 Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs	1400 – 1530
Coffee Break IP5 Interactive Presentations				1530 – 1600
3C	5A	3B	Exhibition Theatre	
12.5 Power Modeling, Estimation and Verification	12.6 Efficient design methodologies for high-performance analog circuits and systems.	12.7 Software optimization for emerging memory architectures and technologies	12.8 Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology	1600 – 1730

SPECIAL DAY SESSION | SPECIAL & EU SESSION | IP SESSION | EXHIBITION THEATRE

D-TRACK | A-TRACK | T-TRACK | E-TRACK

FRIDAY 31 MARCH, 2017

0730 – 0830	Workshop Registration and Welcome Refreshments
Breaks	Please see individual workshop programmes for lunch and break times

0830 – 1730 Room 3B	0830 – 1700 Room 2A	0830 – 1730 Room 2B	0900 – 1700 Room 2C
W01 VLSI for IoT	W02 Emerging Memory Solutions – Technology, Manufacturing, Architectures, Design and Test	W03 4th Workshop on Design Automation for Understanding Hardware Designs DUHDe 2017	W04 MOS-AK Workshop
0830 – 1700 Room 3C	**0830 – 1730 Room 4A**	**0815 – 1640 Room 3A**	**0900 – 1730 Room 5ABC**
W05 Second International Workshop on Resiliency in Embedded Electronic Systems (REES 2017)	W06 The 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)	W07 New Platforms for Future Cars: Safety and Security Challenges	W08 Engineering Multi-Scale Systems for Health, Energy and the Environment

TUTORIALS — MONDAY 27 MARCH

	0800 - 0930	**Registration and Tutorial Welcome Refreshments**
	0930 - 1300	**Morning Tutorials** (1100-1130 Coffee Break)
M01	4BC	**Nano-Tera.ch | Data science techniques and machine learning for EDA**
M03	3A	**Emerging Technologies | 3D Integration: Quo Vadis?**
M04	3B	**System Development and Verification | Developing Next-Generation Embedded Systems: Functional Reactive Programming, Formal Verification, and Real-Time Virtual Resources**
M05	3C	**Dependability | From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test**
	1300 - 1430	**Lunch Break**
	1330	**Conference Registration begins**
	1430 - 1800	**Afternoon Tutorials** (1600-1630 Coffee Break)
M06	4BC	**Nano-Tera.ch | Next 1000x Gains: from Clouds to IoT Systems**
M07	4A	**Design Solutions | Stochastic Computation: the Hypes and the Hopes**
M08	3A	**Emerging Technologies | Is energy wearable?**
M09	3B	**System Development and Verification | An Industry Approach to FPGA and SOC System Development and Verification**
M10	3C	**Dependability | Reliable VLSI Systems**

M01 Nano-Tera.ch Data science techniques and machine learning for EDA

4BC 0930 - 1300

Organiser: Pierre Vandergheynst, EPFL, CH

Data science and machine learning have been instrumental in the development of new applications that affect everyone's life. At the same time, it opens new research challenges but also new opportunities for improving optimisation algorithms. As many other fields, EDA has also been impacted, with several recent works that have proposed to use machine learning towards effective design strategies.This tutorial proposes to give an introduction to data science and machine learning, with an emphasis on their potential benefits in EDA. The tutorial will put a specific focus on graph-based machine learning techniques, and on learning and inference from time-series data, which are two recent branches of machine learning that have high potential in design and system optimisation.

M03 Emerging Technologies 3D Integration: Quo Vadis?

3A 0930 - 1300

Organiser: Partha Pande, Washington State University, US
Chair: Krishnendu Chakrabarty, Duke University, US

Tutorial Plan:

0930 Physical Design for 3D ICs

Speaker: Aida-Todri-Sanial, CNRS-LIRMM/University of Montpellier

The topics covered are:

1. 3D ICs Motivation
2. 3D IC Design
3. 3D Power Delivery Network Design
4. 3D Clock Network Design

1015 The Changing Landscape of 3D Memory Architectures

Speaker: Sudeep Pasricha, Colorado State University

The topics covered are:

1. State-of-the-art in 3D-Stacked Memory Solutions
2. New Architectures and Directions in 3D-Stacked Memory Design
3. Communication Interfaces for 3D-Stacked Memory
4. CAD Tools for 3D-Stacked Memory Design

1130 Energy-Efficient and Reliable 3D Network-on-Chip Design

Speaker: Partha Pratim Pande, Washington State University

The topics covered are:

1. Limitations of Existing 3D NoC Architectures
2. Incorporating Small-Worldness in 3D NoC
3. Architecture Optimization
4. Robustness Against Vertical Link Failures
5. Performance Evaluation

1215 The Hype, Myths, and Realities of Testing 3D ICs

Speaker: Krishnendu Chakrabarty, Duke University

The topics covered are:

1. Defects and Fault Modeling
2. Pre-Bond Testing
3. Post-Bond Testing
4. Test-flow Selection

M04 System Development and Verification Developing Next-Generation Embedded Systems: Functional Reactive Programming, Formal Verification, and Real-Time Virtual Resources

3B 0930 - 1300

Organiser: Albert M. K. Cheng, University of Houston, US
Presenter: Albert M. K. Cheng, University of Houston, Texas, US

Embedded systems are becoming increasingly complex and highly interconnected in cyber-physical systems, thus necessitating new paradigms for their design and implementation. Functional reactive programming (FRP) has several benefits over imperative programming for implementing embedded software, and can potentially transform the way we implement next-generation embedded systems. The first part of this tutorial introduces a framework for accurate response time analysis, scheduling, and verification of embedded controllers implemented as FRP programs. Real-time resource partitioning divides hardware resources into temporal partitions and allocates these partitions as virtual resources to application tasks. Open embedded systems make it easy to add and remove software applications as well as to increase resource utilization and reduce implementation cost when compared to systems which physically assign distinct computing resources to run different applications. The second part of this tutorial describes ways to maintain the schedulability of real-time tasks as if they were scheduled on dedicated physical resources.

M04.1 Introduction to embedded/RT systems and Cyber-Physical Systems
M04.2 Functional reactive programming (FRP) and its Response time analysis (Part 1)
M04.3 Functional reactive programming (FRP) and its Response time analysis (Part 2)
M04.4 Formal analysis & verification techniques based on Real-Time Logic (RTL)
M04.5 Real-Time Virtual Resources (RTVR)

M05 Dependability From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test

3C 0930 - 1300

Speakers: Haralampos-G. Stratigopoulos, Sorbonne Universités, UPMC Univ. Paris 6, CNRS, LIP6, FR
Yiorgos Makris, The University of Texas at Dallas, US

Throughout the design and production lifetime of an integrated circuit, a wealth of data is collected for ensuring its robust and reliable operation. Ranging from design-time simulations to process characterization monitors on first silicon, and from high-volume specification tests to diagnostic measurements on chips returned from the field, the information inherent in this data is invaluable. At the same time, the need for cost-effective solutions for various test-related tasks is becoming more pressing, especially in complex mixed-signal SoCs. As a result, using data analytics methods to mine this information and identify meaningful correlations has seen intense interest and numerous breakthroughs have been made during the last decade. This tutorial seeks to elucidate the utility of data analytics in semiconductor manufacturing and test. Relevant concepts from data analytics theory will be introduced and agglomerated with current practice, showcasing their effectiveness on actual case studies with industrial data.

M05.1 Introduction and Motivation
M05.2 Machine Learning-based Test
M05.3 Adaptive Test
M05.5 Spatial & Spatiotemporal Correlation Modeling
M05.6 Process Monitoring, Yield Forecasting & Fab Attestation
M05.7 Q&A

M06

Nano-Tera.ch
Next 1000x Gains: from Clouds to IoT Systems

4BC 1430 - 1800

Organiser: Subhasish Mitra, Stanford University, US

The computing demands of future aapplications far exceed the capabilities of today's electronics, and cannot be met by isolated improvements in transistor technologies, memories, or integrated circuit (IC) architectures alone. Transformative nanosystems, which leverage the unique properties of emerging nanotechnologies to create new IC architectures, are required to deliver unprecedented performance and energy efficiency. However, emerging nanomaterials and nanodevices face major obstacles such as inherent imperfections and variations. Thus, realizing working circuits, let alone transformative nanosystems, has been infeasible.This tutorial will present an overview of recent advances in nanosystems, from device technologies and design techniques all the way to new architectures, to overcome these challenges: (a) transistors using nanomaterials for high performance and energy efficiency, (b) high-density nonvolatile memories, (c) Ultra-dense (e.g., monolithic) three-dimensional integration of logic and memory for fine-grained connectivity, and (d) new architectures for computation immersed in memory. Hardware prototypes, that represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual nanosystems, will also be discussed. Compared to conventional approaches, the presented approaches promise to improve the energy efficiency of future applications significantly, in the range of three orders of magnitude, thereby enabling new frontiers of applications for both the cloud as well as IoT systems.

M07

Design Solutions
Stochastic Computation: the Hypes and the Hopes

4A 1430 - 1800

Organisers:Jie Han, University of Alberta, CA
Marc Riedel, University of Minnesota, US

An early paper by Gaines in 1969 established the concept of stochastic computing. Initially, much of the interest in the topic was in the field of neural networks, where the concept is known as "pulsed" or "pulse-coded" computation. In fact, the general concept of stochastic computing dates back even earlier, to work by J. von Neumann in the 1950s. He applied probabilistic logic to the study of thresholding and multiplexing operations on bundles of wires with stochastic signals. As he eloquently states in the introduction to his seminal paper, "Our present treatment of error is unsatisfactory and ad hoc. … Error is viewed (in this work), therefore, not as an extraneous and misdirected or misdirecting accident, but as an essential part of the process under consideration …" We find this view, that randomness and noise are integral to computation, to be compelling in the modern era of nanoscale electronics.

The interest in stochastic computing has resurged in recent years. Although intriguing and promising, the paradigm is a proverbial hammer in want of a nail. The hammer: a method for synthesizing circuits that compute complex functions with remarkably simple logic. The nail: applications where simple logic matters. The paradigm suffers from high latency, and so was never compelling for high-performance, high-accuracy computation. However, in the context of novel electronic substrates, it is a potentially transformative approach. It provides high clock skew tolerance and significant reductions in dynamic power.

Different researchers have developed the idea from different angles, some focusing on reliability, others on area and power advantages. A particularly promising application is for novel forms of electronics. The design paradigm of computation on stochastic bit streams is potentially transformative, allowing complex functions to be implemented with very limited transistor counts. For instance, multiplication can be performed with a single AND gate. Complex functions such as exponentials and trigonometric functions can be computed with a handful of gates. Because the bit stream representation is uniform, with all bits weighted equally, circuits designed this way are highly tolerant of soft errors (i.e., bit flips). This tutorial will provide an overview of the current state of the art, a discussion of the advantages and disadvantages of the various design methodologies, and a summary of the applications. It will also discuss open problems and future research directions.

1430 - 1800 **Stochastic Computation: the Hypes and the Hopes**

This tutorial is aimed at a review of the current status, a discussion of the advantages and disadvantages, and an attempt to identify some important questions that are to be addressed for stochastic computation.

1430 Introduction to Stochastic Computation: Background, History, and Underlying Theory
Speakers: Marc Riedel and Jie Han

1515 Stochastic Computational Models for Reliability Evaluation, Biological and Neural Networks
Speaker: Jie Han

1630 A General Synthesis methodology and a Deterministic Approach to "Stochastic Computing"
Speaker: Marc Riedel

1715 Applications: Skew Tolerance, Low Power and Novel Substrates
Speakers: Marc Riedel and Jie Han

M08 Emerging Technologies Is energy wearable?

3A 1430 - 1800

Organiser: Davide Quaglia, University of Verona, IT

Wearable technology will provide personal objects with computational, sensing and communication functions to improve our life. Power consumption is the limiting factor of such systems and energy harvesting seems a possible solution. This tutorial addresses the design and simulation of wearable devices by showing how optimally generate, store, convert and distribute the energy available in the system. The presentations will be accompanied by examples taken from actual case studies. A demo with an actual wearable platform that processes data from different sensors (i.e., microphone, camera, accelerometer,etc.) and supplied by human body energy (light/thermal/kinetic) will be presented.

1430 - 1904 **Session 1**
Chair: Michele Magno, ETH Zurich, CH

1430 Introduction to wearable devices: system architectures and design challenges
Speaker: Davide Quaglia, University of Verona, IT

1500 The energy path in wearable devices: generation, conversion, storage and distribution of energy. Concepts, non-idealities, misconceptions and design guidelines
Speaker: Massimo Poncino, Politecnico di Torino, IT

1630 - 1904 **Session 2**
Chair: Davide Quaglia, University of Verona, IT

1630 Designing wearable devices: energy harvesting technologies techniques, power management and energy neutral systems, trends for future wearable devices
Speaker: Michele Magno, ETH Zurich, CH

1730 Modeling and simulation techniques for wearable devices
Speaker: Davide Quaglia, University of Verona, IT

M09 System Development and Verification An Industry Approach to FPGA and SOC System Development and Verification

3B 1430 - 1800

Speakers: John Zhao, MathWorks, US
Stefano Olivieri, MathWorks Academia Group, US

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

In this set of tutorial sessions, you will learn

- How to implement an application that leverages the FPGA and ARM core of a Zynq SOC
- The flexibility and diversity of the approach through examples that include prototyping a motor control algorithm and a video-processing algorithm
- A HW/SW co-design workflow that combines system level design and simulation with automatic code generation
- Successful use of the HW/SW co-design workflow in commercial development
- Functional verification using MATLAB and Simulink in a SystemVerilog workflow illustrated by a detailed example

1430 Rapidly Implementing MATLAB and Simulink Algorithms on FPGA
Organiser: John Zhao, MathWorks, US

1630 A Hardware/Software Co-Design Approach for MPSoC
Organiser: John Zhao, MathWorks, US

1715 Connecting Simulink Wth SystemVerilog for Easy Functional Verification
Organiser: Stefano Olivieri, MathWorks Academia Group, US

M10 Dependability Reliable VLSI Systems

3C 1430 - 1800

Organisers: Marilyn Wolf, Georgia Tech, US
Joerg Henkel, Karlsruher Institut für Technologie (KIT), DE
Norbert Wehn, TU Kaiserslautern, DE

Reliability is a key concern for many growing semiconductor markets, including automotive, medical, and industrial IoT. Consumer electronics markets have traditionally had low reliability requirements due to the high turnover of products. Chips built for these emerging markets must operate at high levels of confidence and must provide long lifetimes. This tutorial will give a holistic view of reliability, including physical effects, system-level models, and applications. The speakers will discuss reliability models and their influence on system design; DRAM and wireless communication systems; and statistical modeling of thermal behavior.

1430 Reliability of On-chip Systems in the Nano-CMOS Era
Organiser: Jörg Henkel, Karlsruhe Institute of Technology, DE

1545 Dependability Issues in Memories: DRAM Subsystems and Wireless Communication Systems
Organiser: Norbert Wehn, TU Kaiserslautern, DE

1700 **System-Level Thermal Modeling and Optimization**
Organiser: Marilyn Wolf, Georgia Institute of Technology, US

MAIN CONFERENCE

28 – 30 MARCH, 2017

1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses

Tuesday, March 28, 2017
0830 – 1030
SwissTech, Auditorium A

Chair: David Atienza, EPFL, CH
Co-Chair: Giorgio Di Natale, LIRMM, FR

0830 **Welcome Addresses**

David Atienza
DATE 2017 General Chair, EPFL, CH

Giorgio Di Natale
DATE 2017 Programme Chair, LIRMM, FR

0845 **Presentation of distinguished awards**

EDAA Achievement Award 2017
(C. L. David Liu)

EDAA Outstanding Dissertations Award 2016

DATE Fellow Awards
(Luca Fanucci, University of Pisa, IT and Jürgen Haase, edacentrum, DE)

IEEE Fellow Awards
(Cristina Silvano, Politecnico di Milano, IT
Alex Yakovlev, Newcastle University, GB
Valeria Bertacco, University of Michigan, US
Todd Austin, University of Michigan, US)

IEEE CEDA Outstanding Service Contribution Award 2016 and IEEE CS TTTC Outstanding Contribution Award
(Luca Fanucci, University of Pisa, IT)

0915 **Keynote Addresses**

0915 **1.1.1 Keynote Address: Design Automation in the Era of AI and IoT: Challenges and Pitfalls**
Arvind Krishna, IBM Research, US

0945 **1.1.2 Keynote Address: A New Era of Hardware Microservices in the Cloud**
Doug Burger, Microsoft Research, US

1030 Coffee Break in the Exhibition Area

2.1 Executive Panel: The Electronics Innovation Landscape: Opportunities, Challenges and Strategies

Auditorium A 1130 - 1300

Chair: Alberto Sangiovanni-Vincentelli, UCB, US

From autonomous driving to big data, from machine learning to cyber-physical systems, from robotics to the internet of everything, from brain-machine interfaces to the human intranet, innovation is moving at a pace that has never been seen before. To face the large investments and increasing global competition, mergers and acquisitions have sped up in all areas including the semiconductor industry that has been possibly the most decisive enabling factors of these disruptive technologies. The panel will address what are the structural factors to sustain innovations and what are the strategies that some of important actors in the industrial and research sector are embracing. The panel will also address the opportunities and difficulties of the different regions of the world in the changing social and economic landscape. The panel will begin with an introductory presentation about the state of technology and innovations in the areas outlined above. Then executives from IBM, ST Microelectronics and Leti will address the problems to face and the strategies to embrace in a challenging competitive landscape.

Panelists:

Arvind Krishna, Senior Vice President, Hybrid Cloud and Director, IBM Research, US
Marie-Noëlle Semeria, CEO, CEA/Leti, FR
Benedetto Vigna, EVP & GM, Analog & MEMS Group, STMicroelectronics, IT

1300 Lunch Break in Garden Foyer

2.2 Stochastic, Approximate and Neural Computing

4BC 1130 - 1300

Chair: Lukas Sekanina, Brno University of Technology, CZ
Co-Chair: Andy Tyrrell, University of York, GB

Stochastic and approximate computing is an approach developed to improve energy efficiency of computer hardware. First paper presents a framework for quantifying and managing accuracy in stochastic circuits design. Second paper deals with a new approximate multipler design. Energy efficient hybrid stochastic-binary neural-networks are proposed in the third paper. The last paper addresses a new retraining method improving fault tolerance in RRAM crossbars.

1130 **Framework for Quantifying and Managing Accuracy in Stochastic Circuit Design**

Speaker: Florian Neugebauer, University of Passau, DE
Authors: Florian Neugebauer[1], Ilia Polian[1] and John Hayes[2]
[1]University of Passau, DE; [2]University of Michigan, US

1200 **Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression**

Speaker: Issa Qiqieh, School of Electrical and Electronic Engineering, Newcastle University, GB
Authors: Issa Qiqieh, Rishad Shafik, Ghaith Tarawneh, Danil Sokolov and Alex Yakovlev, Newcastle University, GB

1230 **Energy-Efficient Hybrid Stochastic-Binary Neural Networks for Near-Sensor Computing**

Speaker: Vincent Lee, University of Washington, US
Authors: Vincent Lee[1], Armin Alaghi[1], John Hayes[2], Visvesh Sathe[1] and Luis Ceze[1]
[1]University of Washington, US; [2]University of Michigan, US

1245 **Accelerator-friendly Neural-network Training: Learning Variations and Defects in RRAM Crossbar**

Speaker: Li Jiang, Shanghai Jiao Tong University, CN
Authors: Lerong Chen[1], Jiawen Li[1], Yiran Chen[2], Qiuping Deng[3], Jiyuan Shen[1], Xiaoyao Liang[1] and Li Jiang[4]
[1]Shanghai Jiao Tong University, CN; [2]University of Pittsburgh, US; [3]Lynmax Research, CN; [4]Department of Computer Science and Engineering, Shanghai Jiao Tong University, CN

IPs **IP1-1, IP1-2, IP1-3**

1300 Lunch Break in Garden Foyer

2.3 Cache memory management for performance and reliability

2BC 1130 - 1300

Chair: Dionisios Pnevmatikatos, Technical University of Crete, GR
Co-Chair: Cristina Silvano, Politecnico di Milano, IT

Cache memory design optimizations and management can have a significant effect on cost, performance, and reliability. The first paper proposes an asymmetric cache management policy for GPGPUs with hybrid main memories that significantly improve performance for memory intensive workloads. The second paper targets the optimization of the bank placement in GPUs' last level cache, with the goal of maximizing the performance of the GPU's on-chip network. The third paper proposes a methodology for jointly analyzing all the cache level configurations to determine and minimize the susceptibility of the caches to soft errors

1130 **Shared Last-level Cache Management for GPGPUs with Hybrid Main Memory**

Speaker: Lei Ju, Shandong University, CN
Authors: Guan Wang, Xiaojun Cai, Lei Ju, Chuanqi Zang, Mengying Zhao and Zhiping Jia, Shandong University, CN

1200 **Effective Cache Bank Placement for GPUs**

Speaker: Mohammad Sadrosadati, Sharif University of Technology, IR
Authors: Mohammad Sadrosadati[1], Amirhossein Mirhosseini[2], Shahin Roozkhosh[1], Hazhir Bakhishi[1] and Hamid Sarbazi-Azad[1]
[1]Sharif University of Technology, IR; [2]University of Michigan, US

1230 **Soft Error-Aware Architectural Exploration for Designing Reliability Adaptive Cache Hierarchies in Multi-Cores**

Speaker: Semeen Rehman, TU Dresden, DE
Authors: Arun Subramaniyan[1], Semeen Rehman[2], Muhammad Shafique[3], Akash Kumar[4] and Joerg Henkel[5]
[1]EECS, University of Michigan-Ann Arbor, US; [2]TU Dresden, DE; [3]Vienna University of Technology (TU Wien), AT; [4]Technische Universitaet Dresden, DE; [5]KIT, DE

IPs **IP1-4**

1300 Lunch Break in Garden Foyer

2.4 Performance and Power Analysis

3A 1130 - 1300

Chair: Gianluca Palermo, Politecnico di Milano, IT
Co-Chair: Ingo Sander, KTH Royal Institute of Technology, SE

Early performance and power estimation is critical for computer system design. This session covers novel analytical and semi-analytical approaches for fast and accurate modeling of different system components, including GPUs, DRAMs and caches.

1130 **GATSim: Abstract Timing Simulation of GPUs**

Speaker: Andreas Gerstlauer, The University of Texas at Austin, US
Authors: Kishore Punniyamurthy, Behzad Boroujerdian and Andreas Gerstlauer, The University of Texas at Austin, US

1200 **MeSAP: A fast analytic power model for DRAM memories**

Speaker: Sandeep Poddar, IBM Research, The Netherlands, NL
Authors: Sandeep Poddar[1], Rik Jongerius[1], Leandro Fiorin[1], Giovanni Mariani[1], Gero Dittmann[2], Andreea Anghel[2] and Henk Corporaal[3]
[1]IBM Research, NL; [2]IBM Research, CH; [3]TU/e (Eindhoven University of Technology), NL

1230 **AFEC: An Analytical Framework for Evaluating Cache Performance in Out-of-Order Processors**

Speaker: Kecheng Ji, Southeast University, CN
Authors: Kecheng Ji[1], Ming Ling[1], Qin Wang[1], Longxing Shi[1] and Jianping Pan[2]
[1]Southeast University, CN; [2]University of Victoria, CA

IPs **IP1-5**

1300 Lunch Break in Garden Foyer

2.5 Reliability and Energy-Efficiency: Two Pillars of NoC Design

3C 1130 - 1300

Chair: Sebastien Le Beux, Ecole Central du Lyon, FR
Co-Chair: Tushar Krishna, Georgia Institute of Technology, US

This session addresses challenges related to energy efficiency and reliability of NoCs. The first paper proposes an analytical approach to evaluate the reliability of adaptive routing algorithms. In the second paper, an online monitoring and routing approach is proposed to address the aging-related degradation in electrical NoC. Finally, the third paper shows how to use network traffic-aware spatial parallelism to improve the energy efficiency of the Epiphany SoC.

1130 **Reliability Assessment of Fault Tolerant Routing Algorithms in Networks-on-Chip: An Analytic Approach**

Speaker: Sadia Moriam, Technische Universitaet Dresden, DE
Authors: Sadia Moriam[1] and Gerhard Fettweis[2]
[1]Technische Universität Dresden, DE; [2]TU Dresden, DE

1200 **Online Monitoring and Adaptive Routing for Aging Mitigation in NoCs**

Speaker: Nader Bagherzadeh, University of California, Irvine, US
Authors: Zana Ghaderi, Ayed Alqahtani and Nader Bagherzadeh, University of California, Irvine, US

1230 **eBSP: Managing NoC Traffic for BSP workloads on the 16-core Adapteva Epiphany-III Processor**

Speaker: Siddhartha Siddhartha, Nanyang Technological University, SG
Authors: Siddhartha Siddhartha[1] and Nachiket Kapre[2]
[1]Nanyang Technological University, SG; [2]University of Waterloo, CA

1300 Lunch Break in Garden Foyer

2.6 Advancing Test for Mixed-Signal and Microfluidic Circuits and Systems

5A 1130 - 1300

Chair: Andre Ivanov, Univ. BC, CA
Co-Chair: Marie-Minerve Louerat, Univ. Pierre et Marie Curie, FR

Papers in this session discuss latest advances and methodologies for test, including the application of machine learning and sensitivity analysis to mixed-signal circuits, and also presents novel solutions to the test of microfluidic systems.

1130 **On the limits of machine learning-based test: a calibrated mixed-signal system case study**

Speaker: Manuel Barragan, TIMA Laboratory, FR
Authors: Manuel Barragan[1], Gildas Leger[2], Antonio Gines[3], Eduardo Peralias[4] and Adoracion Rueda[3]
[1]TIMA Laboratory, FR; [2]Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC - Universidad de Sevilla), ES; [3]Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC-Universidad de Sevilla), ES; [4]Instituto de Microelectronica de Sevilla, IMSE-CNM, (CISC-Universidad de Sevilla), ES

1200 **An Extension of Crohn's Sensitivity Theorem to Mismatch Analysis of 1-Port Resistor Networks**

Speaker: Sebastien Cliquennois, St Microelectronics, FR
Author: Sebastien Cliquennois, ST Microelectronics, FR

1230 **Testing Microfluidic Fully Programmable Valve Arrays (FPVAs)**

Speaker: Chunfeng Liu, Technical University of Munich, DE
Authors: Chunfeng Liu[1], Bing Li[2], Bhargab B. Bhattacharya[3], Krishnendu Chakrabarty[4], Tsung-Yi Ho[5] and Ulf Schlichtmann[6]
[1]Technical University of Munich (TUM), DE; [2]TU München (TUM), DE; [3]Indian Statistical Institute, IN; [4]Duke University, US; [5]National Tsing Hua University, TW; [6]TU München, DE

IPs **IP1-6, IP1-7**

1300 Lunch Break in Garden Foyer

2.7 EU Project Special Session: from Secure Clouds to reliable and variable HPC

3B 1130 - 1300

Chair: Lorena Anghel, TIMA Laboratory, FR

Covering the major topics presented in DATE, the European Projects presented in this session show lessons learned, best practices, scientific methods and evaluation platforms, successful strategies and roadmaps solving research and industry concerns in Europe.

1130 **HARPA: Tackling Physically Induced Performance Variability**

Speaker: Dimitrios Soudris, ICCS, GR
Authors: Nikolaos Zompakis[1] and Dimitrios Soudris[2]
[1]ICCS/NTUA, GR; [2]NTUA, GR

1200 **Dynamic Software Randomisation: Lessons Learned From an Aerospace Case Study**

Speaker: Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES
Authors: Leonidas Kosmidis[1], Jaume Abella[2] and Francisco Cazorla[3]
[1]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [2]Barcelona Supercomputing Center (BSC-CNS), ES; [3]Barcelona Supercomputing Center and IIIA-CSIC, ES

1215 **READEX: Linking Two Ends of the Computing Continuum to Improve Energy-efficiency in Dynamic Applications**

Speaker: Per Gunnar Kjeldsberg, Norwegian University of Science and Technology, NO
Authors: Per Gunnar Kjeldsberg[1], Andreas Gocht[2], Michael Gerndt[3], Riha Lubomir[4], Joseph Schuchart[5] and Umbreen Sabir Mian[2]
[1]Norwegian University of Science and Technology, NO; [2]Technische Universität Dresden, DE; [3]Technische Universität München, DE; [4]IT4Innovations, Ostrava, CZ; [5]Universität Stuttgart, DE

1230 **BASTION: Board and SoC Test Instrumentation for Ageing and No Failure Found**

Speaker: Matteo Sonza, Reorda, IT
Authors: Erik Larsson[1], Matteo Sonza Reorda[2], Maksim Jenihhin[3], Jaan Raik[4], Hans Kerkhoff[5], Rene Krenz-Baath[6] and Piet Engelke[7]
[1]Lund University, SE; [2]Politecnico di Torino - DAUIN, IT; [3]Tallinn University of Technology, EE; [4]Tallinn university of Technology, EE; [5]University of Twente / CTIT-TDT, NL; [6]Hochschule Hamm-Lippstadt University of applied Sciences, DE; [7]Infineon Technologies AG, DE

1245 **RETHINK big: European Roadmap for Hardware and Networking Optimizations for Big Data**

Speaker: Osman Unsal, Barcelona Supercomputing Center, ES
Authors: Gina Alioto[1] and Paul Carpenter[2]
[1]Barcelona Supercomputing Center, ES; [2]BSC, ES

IPs **IP1-8, IP1-9, IP1-10, IP1-11**

1300 Lunch Break in Garden Foyer

2.8a Smart Medical Devices, Part 1

Exhibition Theatre 1130 - 1230

Organiser: Patrick Mayor, EPFL, CH

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1300 Lunch Break in Garden Foyer

2.8b Smart Medical Devices, Part 2

Exhibition Theatre 1230 - 1300

Organiser: John Zhao, MathWorks, US

See Page 108

1300 Lunch Break in Garden Foyer

3.0 LUNCH TIME KEYNOTE SESSION:

Garden Foyer 1350 - 1420

Chair: David Atienza, EPFL, CH

See Page 8

1350 **Precision Medicine: Where Engineering and Life Science meet**

Speaker and Author: Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH

1430 Session 3

3.1 IT&A Session: Parallel Ultra-Low-Power Computing for the IoT: Applications, Platforms, Circuits

5BC 1430 - 1600

Organisers: Luca Benini, ETHZ, CH
Davide Rossi, University of Bologna, IT
Chair: Luca Benini, ETHZ, CH
Co-Chair: Davide Rossi, University of Bologna, IT

This special session will give a deep dive into Ultra-low power computing for Internet-of-Things applications, starting from leading-edge MCU-based commercial solutions, moving to next generation highly-parallel ULP architectures based on open-source hardware & software, fast-forwarding to advanced research solutions based new models of computations

1430 **Better than Worst Case Signoff Strategies for Low Power IoT Devices**

Speaker: Jose Pineda de Gyvez, NXP Semiconductors, NL
Authors: Jose Pineda and Hamed Fatemi, NXP Semiconductors, NL

1500 **GAP: an Open-source PULP-RiscV platform for Near-sensor Analytics**

Speaker and Author: Eric Flamand, GreenWaves Technologies, FR

1530 **Energy-quality scalable adaptive VLSI circuits and systems beyond approximate computing**

Speaker and Author: Massimo Alioto, National University of Singapore, SG

1600 Coffee Break in Exhibition Area

3.2 Hot Topic Session: New Benchmarking Vectors for Emerging Devices, Circuits, and Architectures: Energy, Delay, and ... Accuracy

4BC 1430 - 1600

Organizers: Xiaobo Sharon Hu and Michael Niemier, University of Notre Dame, US
Chair: Xiaobo Sharon Hu, University of Notre Dame, US
Co-Chair: Pierre-Emmanuel Gaillardon, The University of Utah at Salt Lake City, US

There is ever-growing interest in alternative computational models (e.g., neural networks, etc.), as well as how emerging technologies can best be exploited to address application-level needs. This hot topic session addresses the above issues from the perspective of benchmarking. It considers the impact of emerging devices, circuits, and architectures at the application level in the context of new metrics and benchmarking methodologies being developed via the Semiconductor Research Corporation (SRC). Subsequent presentations highlight benchmarking and design space exploration efforts that consider application-level energy and performance in the context of computational accuracy. They also highlight infrastructure that can be used to compare different devices, circuits, and architectures that ultimately address the same information processing task.

1430 **Beyond-CMOS Non-Boolean Logic Benchmarking: Insights and Future Directions**

Speaker: Azad Naeemi, Georgia Institute of Technology, US
Authors: Chenyun Pan and Azad Naeemi, Georgia Institute of Technology, US

1500 **Understanding the Design of IBM Neurosynaptic System and Its Tradeoffs: A User Perspective**

Speaker: Yiran Chen, Duke University, US
Authors: Hsin-Pai Cheng, Wei Wen, Chunpeng Wu, Sicheng Li, Hai (Helen) Li and Yiran Chen, University of Pittsburgh, US

1530 **Cellular Neural Network Friendly Convolutional Neural Networks - CNNs with CNNs**

Speaker: Michael Niemier, University of Notre Dame, US
Authors: András Horváth[1], Michael Hillmer[2], Qiuwen Lou[2], X, Sharon Hu[2] and Michael Niemier[2]
[1]Pázmány Péter Catholic University, HU; [2]University of Notre Dame, US

1600 Coffee Break in Exhibition Area

3.3 Hardware Trojans and Fault Attacks

2BC 1430 - 1600

Chair: Ilia Polian, University of Passau, DE
Co-Chair: Matthias Sauer, University of Freiburg, DE

This section focuses on two types of active attacks on system hardware modules: hardware Trojans (malicious modifications) and fault-injections into cryptographic modules. The papers cover Trojans that target coherence protocols in memory caches; Trojan detection based on measurement of path delays; detection of malware using machine learning; and fault attacks on the cryptographic hash function SHA-3.

1430 **Algebraic Fault Analysis of SHA-3**

Speaker: Pei Luo, Northeastern University, US
Authors: Pei Luo, Konstantinos Athanasiou, Yunsi Fei and Thomas Wahl, Northeastern University, US

1500 **Evaluating Coherence-exploiting Hardware Trojan**

Speaker: Minsu Kim, Korea University, KR
Authors: Minsu Kim[1], Sunhee Kong[1], Boeui Hong[1], Lei Xu[2], Weidong Shi[2] and Taeweon Suh[1]
[1]Korea University, KR; [2]University of Houston, US

1530 **Hardware Trojan Detection Based on Correlated Path Delays in Defiance of Variations with Spatial Correlations**
Speaker: Fatma Nur Esirci, Gebze Technical University, TR
Authors: Fatma Nur Esirci and Alp Arslan Bayrakci, Gebze Technical University, TR

1545 **Malware Detection using Machine Learning Based Analysis of Virtual Memory Access Patterns**
Speaker: Zhixing Xu, Princeton University, US
Authors: Zhixing Xu[1], Sayak Ray[2], Pramod Subramanyan[1] and Sharad Malik[1]
[1]Princeton University, US; [2]Intel corp, US

IPs **IP1-12**

1600 Coffee Break in Exhibition Area

3.4 Guardbanding and Approximation

3A 1430 - 1600

Chair: Michael Glass, Ulm University, DE
Co-Chair: Yuko Hara-Azumi, Tokyo Institute of Technology, JP

This session starts with a guardbanding-based approach that uses cell libraries designed and classified for different temperature ranges for improving circuit timing as well as lifetime. This is followed by several approximate computation techniques that optimize the energy consumption of the circuits. The second paper in the session compares the use of approximate arithmetic components (adders, multipliers) with truncation and rounding techniques to diminish the bit-width of the units. The third work proposes a source-to-source transformation to optimize the energy-accuracy tradeoff. This session concludes with two IP presentations on approximate errors symbolic system synthesis.

1430 **Optimizing Temperature Guardbands**
Speaker: Hussam Amrouch, Karlsruhe Institute of Technology (KIT), DE
Authors: Hussam Amrouch[1], Behnam Khaleghi[2] and Joerg Henkel[3]
[1]Karlsruhe Institute of Technology, DE; [2]Sharif University of Technology, IR; [3]KIT, DE

1500 **The Hidden Cost of Functional Approximation Against Careful Data Sizing: A Case Study**
Speaker: Benjamin Barrois, University of Rennes [1] / IRISA, FR
Authors: Benjamin Barrois[1], Olivier Sentieys[2] and Daniel Menard[3]
[1]University of Rennes - INRIA, FR; [2]INRIA, FR; [3]INSA Rennes, FR

1530 **High-Level Synthesis of Approximate Hardware under Joint Precision and Voltage Scaling**
Speaker: Seogoo Lee, The University of Texas at Austin, US
Authors: Seogoo Lee[1], Lizy John[2] and Andreas Gerstlauer[1]
[1]The University of Texas at Austin, US; [2]UT Austin, US

IPs **IP1-13, IP1-14, IP1-15**

1600 Coffee Break in Exhibition Area

3.5 Low-power brain inspired computing for embedded systems

3C 1430 - 1600

Chair: Johanna Sepulveda, TU Munich, DE
Co-Chair: Andrea Bartolini, Uniiversita' di Bologna - ETH Zurich, IT

Neural Networks are promising techniques for bringing brain inspired computing into embedded platforms. Energy efficiency is a primary concern in these computing domain. This track combines low power design techniques such as approximate computing and compression with state-of-the-art hardware architectures.

1430 **Approximate Computing for Spiking Neural Networks**

Speaker: Sanchari Sen, Purdue University, US
Authors: Sanchari Sen, Swagath Venkataramani and Anand Raghunathan, Purdue University, US

1500 **Adaptive Weight Compression for Memory-Efficient Neural Networks**

Speaker: Jong Hwan Ko, Georgia Institute of Technology, US
Authors: Jong Hwan Ko, Duckhwan Kim, Taesik Na, Jaeha Kung and Saibal Mukhopadhyay, Georgia Institute of Technology, US

1530 **Real-time Anomaly Detection for Streaming Data using Burst Code on a Neurosynaptic Processor**

Speaker: Qinru Qiu, Syracuse University, US
Authors: Qiuwen Chen and Qinru Qiu, Syracuse University, US

1545 **Fast, Low Power Evaluation of Elementary Functions Using Radial Basis Function Networks**

Speaker: Parami Wijesinghe, Purdue University, US
Authors: Parami Wijesinghe, Chamika Liyanagedera and Kaushik Roy, Purdue University, US

1600 Coffee Break in Exhibition Area

3.6 Mechanisms for hardware fault testing, recovery and metastability management

5A 1430 - 1600

Chair: Jaume Abella, Barcelona Supercomputing Center (BSC), ES
Co-Chair: Maria K. Michael, University of Cyprus, CY

Papers in this session provide new solutions for dealing with hardware faults and metastability issues, including testing and diagnosing mechanisms for NoCs, fault recovery approaches for 3D ICs, and containment solutions for metastability in sorting networks

1430 **Charka: A Reliability-Aware Test Scheme for Diagnosis of Channel Shorts Beyond Mesh NoCs**

Speaker: Santosh Biswas, IIT Guwahati, IN
Authors: Biswajit Bhowmik[1], Jatindra Kumar Deka[1] and Santosh Biswas[2]
[1]IIT Guwahati, IN; [2]I IT GUWAHATI, IN

1500 **Recovery-aware Proactive TSV Repair for Electromigration in 3D ICs**

Speaker: Shengcheng Wang, Chair of Dependable Nano Computing (CDNC), Karlsruhe Institute of Technology (KIT), DE
Authors: Shengcheng Wang[1], Hengyang Zhao[2], Sheldon Tan[3] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]University of California, Riverside, US; [3]University of California at Riverside, US

1530 **Near-Optimal Metastability-Containing Sorting Networks**

Speaker: Moti Medina, MPI for Informatics, DE
Authors: Johannes Bund[1], Christoph Lenzen[2] and Moti Medina[2]
[1]Saarland University, DE; [2]MPI-INF, DE

IPs **IP1-16, IP1-17**

1600 Coffee Break in Exhibition Area

3.7 Scheduling and Optimization

3B 1430 - 1600

Chair: Rolf Ernst, TU Braunschweig, DE
Co-Chair: Kai Lampka, Uppsala University, SE

This session focuses on methods to optimize the design of real-time embedded systems. The first two presentations cover priority assignment and task partitioning for scheduling on multi-core systems. The last long presentation and interactive presentations focus on architectural and OS considerations.

1430 **The Concept of Unschedulability Core for Optimizing Priority Assignment in Real-Time Systems**
Speaker: Yecheng Zhao, Virginia Polytechnic Institute and State University, US
Authors: Yecheng Zhao and Haibo Zeng, Virginia Tech, US

1500 **Utilization Difference Based Partitioned Scheduling of Mixed-Criticality Systems**
Speaker: Saravanan Ramanathan, Nanyang Technological University, SG
Authors: Saravanan Ramanathan and Arvind Easwaran, Nanyang Technological University, SG

1530 **Schedulability using native non-preemptive groups on an AUTOSAR/OSEK platform with caches**
Speaker: Leo Hatvani, Technische Universiteit Eindhoven, NL
Authors: Leo Hatvani[1], Reinder J. Bril[1] and Sebastian Altmeyer[2]
[1]Technische Universiteit Eindhoven (TU/e), NL; [2]University of Amsterdam (UvA), NL

IPs **IP1-18, IP1-19**

1600 Coffee Break in Exhibition Area

3.8 Addressing Challenges in Today's Datacenter Systems' Design

Exhibition Theatre 1430 - 1600

Organiser: Ousmane Diallo, EPFL, CH

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1600 Coffee Break in Exhibition Area

3.9 A tribute to Ralph Otten

Auditorium A 1430 - 1600

Organiser: Giovanni De Micheli, EPFL, CH
Chair: Michael Burstein, CEO Billy.com, CA
Co-Chair: Giovanni De Micheli, EPFL, CH

World renowned leaders in Physical Design will talk about accomplishments in this field over the last four decades, as a tribute to Ralph Otten, pioneer of this field and prematurely died in an accident.

1430 **Chip Design – Physical and Philosophical**
Speaker and Author: Dave Liu, NTHU, TW

1445 **Automatic Floorplan Design**
Speaker and Author: Martin Wong, University of Illinois at Urbana Champaign, US

1500 **The Evolution of Floorplanning**
Speaker and Author: Antun Domic, Synopsys, US

1515 **From silicon compiler to physical synthesis: Ralph Otten's contributions to EDA**
Speaker and Author: Patrick Groeneweld, Synopsys, US

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1530 **Dealing with Exploding Design Rule Numbers and Complexity**
Speaker and Author: Raul Camposano, Sage Design Automation, US

1545 **In memoriam of Ralph Otten: breaking down the complexity of layout design under Moore's Law**
Speaker and Author: Jochen Jess, Eindhoven University of Technology, NL

1600 Coffee Break in Exhibition Area

IP1 Interactive Presentations

IP sessions (in front of rooms 4A and 5A) 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. At the end of each afternoon Interactive Presentations session the award 'Best IP of the Day' is given.

IP1-1 **Structural Design Optimization for Deep Convolutional Neural Networks using Stochastic Computing**
Speaker: Yanzhi Wang, Syracuse University, US
Authors: Zhe Li[1], Ao Ren[1], Ji Li[2], Qinru Qiu[1], Bo Yuan[3], Jeffrey Draper[2] and Yanzhi Wang[1]
[1]Syracuse University, US; [2]University of Southern California, US; [3]City University of New York, City College, US

IP1-2 **ApproxQA: A Unified Quality Assurance Framework for Approximate Computing**
Speaker: Ting Wang, The Chinese University of Hong Kong, HK
Authors: Ting Wang, Qian Zhang and Qiang Xu, The Chinese University of Hong Kong, HK

IP1-3 **EvoApprox8b: Library of Approximate Adders and Multipliers for Circuit Design and Benchmarking of Approximation Methods**
Speaker: Lukas Sekanina, Brno University of Technology, CZ
Authors: Vojtech Mrazek, Radek Hrbacek, Zdenek Vasicek and Lukas Sekanina, Brno University of Technology, CZ

IP1-4 **Droop Mitigating Last Level Cache Architecture for STTRAM**
Speaker: Swaroop Ghosh, Pennsylvania State University, US
Authors: Radha Krishna Aluru[1] and Swaroop Ghosh[2]
[1]University of South Florida, US; [2]Pennsylvania State University, US

IP1-5 **Modeling Instruction cache and instruction buffer for performance estimation of VLIW architectures using native simulation**
Speaker: Omayma Matoussi, Grenoble INP, TIMA laboratory, FR
Authors: Omayma Matoussi[1] and Frédéric Pétrot[2]
[1]Tima Laboratory at Grenoble, FR; [2]TIMA Laboratory, Grenoble Institute of Technology, FR

IP1-6 **Analog Fault Testing Through Abstraction**
Speaker: Enrico Fraccaroli, Università degli Studi di Verona, IT
Authors: Enrico Fraccaroli and Franco Fummi, Università degli Studi di Verona, IT

IP1-7 **BISCC: Efficient Pre Through Post Silicon Validation of Mixed-Signal/RF Systems Using Built In State Consistency Checking**
Speaker: Abhijit Chatterjee, Georgia Institute of Technology, US
Authors: Sabyasachi Deyati[1], Barry Muldrey[1] and Abhijit Chatterjee[2]
[1]Georgia Institute of Technology, US; [2]Georgia Tech, US

IP1-8 **Computing with Nano-Crossbar Arrays: Logic Synthesis and Fault Tolerance**
Speaker: Mustafa Altun, Istanbul Technical University, TR
Authors: Mustafa Altun[1], Valentina Ciriani[2] and Mehdi Tahoori[3]
[1]Istanbul Technical University, TR; [2]University of Milan, IT; [3]Karlsruhe Institute of Technology, DE

IP1-9 **SecureCloud: Secure Big Data Processing in Untrusted Clouds**
Speaker and Author: Rafael Pires, University of Neuchâtel, CH

IP1-10 **WCET-Aware Parallelization of Model-Based Applications for Multi-Cores: the ARGO Approach**
Speaker: Steven Derrien, Universite de Rennes [1], FR
Authors: Steven Derrien[1] and Isabelle Puaut[2]
[1]sderrien, FR; [2]University of Rennes [1] / IRISA, FR

IP1-11 **Exploring the unknown through successive generations of low power and low resource versatile agents**
Speaker: Martin Andraud, TU Eindhoven, NL
Authors: Martin Andraud[1] and Marian Verhelst[2]
[1]TU Eindhoven, NL; [2]KU Leuven, BE

IP1-12 **Power Profiling of Microcontroller's Instruction Set for Run-time Hardware Trojans Detection without Golden Circuit Models**
Speaker: Falah Awwad, College of Engineering / Department of Electrical Engineering, UAE University, AE
Authors: Faiq Khalid Lodhi[1], Syed Rafay Hasan[2], Osman Hasan[1] and Falah Awwad[3]
[1]School of Electrical Engineering and Computer Science National University of Sciences and Technology (NUST), PK; [2]Department of Electrical and Computer Engineering, Tennessee Technological University, US; [3]College of Engineering, United Arab Emirates University, AE

IP1-13 **Accounting for Systematic Errors in Approximate Computing**
Speaker: Martin Bruestel, Technical University Dresden, DE
Authors: Martin Bruestel[1] and Akash Kumar[2]
[1]Technical University Dresden, DE; [2]Technische Universitaet Dresden, DE

IP1-14 **Gaussian Mixture Error Estimation for Approximate Circuits**
Speaker: Amin Ghasemazar, The University of British Columbia, CA
Authors: Amin Ghasemazar and Mieszko Lis, University of British Columbia, CA

IP1-15 **Enhancing Symbolic System Synthesis through ASPmT with Partial Assignment Evaluation**
Speaker: Kai Neubauer, University of Rostock, DE
Authors: Kai Neubauer[1], Philipp Wanko[2], Torsten Schaub[2] and Christian Haubelt[1]
[1]University of Rostock, DE; [2]University of Potsdam, DE

IP1-16 **3DFAR: A Three-Dimensional Fabric for Reliable Multicore Processors**
Speaker: Valeria Bertacco, University of Michigan-, US
Authors: Javad Bagherzadeh and Valeria Bertacco, University of Michigan, US

IP1-17 **Evaluating Impact of Human Errors on the Availability of Data Storage Systems**
Speaker: Hossein Asadi, Sharif University of Technology, IR
Authors: Mostafa Kishani, Reza Eftekhari and Hossein Asadi, Sharif University of Technology, IR

IP1-18 **GPUguard: Towards Supporting a Predictable Execution Model for Heterogeneous SoC**
Speaker: Björn Forsberg, ETH Zürich, CH
Authors: Björn Forsberg[1], Andrea Marongiu[2] and Luca Benini[3]
[1]ETH Zürich, CH; [2]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [3]Università di Bologna, IT

IP1-19 **A Non-Intrusive, Operating System Independent Spinlock Profiler for Embedded Multicore Systems**
Speaker: Lin Li, Infineon Technologies AG, DE
Authors: Lin Li[1], Philipp Wagner[2], Albrecht Mayer[3], Thomas Wild[2] and Andreas Herkersdorf[4]
[1]Infineon Technologies, DE; [2]Technical University of Munich, DE; [3]Infineon, DE; [4]TU München, DE

1700 Session 4

4.1 IT&A Session: The Emergence of Silicon Photonics: From High Performance Computing to Data Centers and Quantum Computing

5BC 1700 - 1830

Organiser: Luca Carloni, Columbia University, US
Chair: Luca Carloni, Columbia University, US

Recent years have seen major progress in the design and manufacturing of silicon photonics devices. This session provides an overview of the potential that this emerging technology offers for three different types of system and discusses the most important challenges that remain to be addressed. The first talk shows how silicon photonics components can be used to realize energy-efficient high-bandwidth optical interconnection networks. The second talk presents which further advances in manufacturing, packages and testing are needed in order to realize silicon photonics based products for data centers. Finally, the last talk explains how the generation of optical quantum states on an integrated platform can enable future practical implementations of quantum information processing systems.

1700 **Energy-Performance Optimized Design of Silicon Photonic Interconnection Networks for High-Performance Computing**

Speaker: Keren Bergman, Columbia University, US
Authors: Meisam Bahadori[1], Sebastien Rumley[1], Robert Polster[1], Alexander Gazman[1], Matt Traverso[2], Mark Webster[2], Kaushik Patel[2] and Keren Bergman[1]
[1]Columbia University, US; [2]Cisco System, US

1730 **Rapid Growth of IP Traffic Is Driving Adoption of Silicon Photonics in Data Centers**

Speaker and Author: Kaushik Patel, Cisco Systems, US

1800 **Generation of Complex Quantum States via Integrated Frequency Combs**

Speaker: Roberto Morandotti, INRS-EMT, CA
Authors: Christian Reimer[1], Michael Kues[2], Piotr Roztocki[1], Benjamin Wetzel[3], Brent E. Little[4], Sai T. Chu[5], Lucia Caspani[6], David J. Moss[7] and Roberto Morandotti[1]
[1]INRS-EMT, CA; [2]INRS-EMT & University of Glasgow, CA; [3]INRS-EMT & University of Sussex, CA; [4]Xi'an Institute of Optics and Precision Mechanics, CN; [5]City University of Hong Kong, CN; [6]University of Strathclyde, GB; [7]Swinburne University of Technology, AU

4.2 Logic, Interconnects, Neurons: New Realizations

4BC 1700 - 1830

Chair: Elena Gnani, University of Bologna, IT
Co-Chair: Aida Todri-Sanial, CNRS-LIRMM, FR

This session covers papers showing new approaches to realize optimized logic circuit using silicon nanowire reconfigurable transistors; intra- and inter-core optoelectronic interconnects for energy efficient communications; and magnetic skyrmions as novel nanoelectronic device for non-linear neuron networks.

1700 **Exploiting Transistor-Level Reconfiguration to Optimize Combinational Circuits**

Speaker: Michael Raitza, TU Dresden, DE
Authors: Michael Raitza[1], Jens Trommer[2], Akash Kumar[3], Marcus Völp[4], Dennis Walter[5], Walter Weber[6] and Thomas Mikolajick[7]
[1]Technische Universität Dresden and CfAED, DE; [2]Namlab gGmbH, DE; [3]Technische Universitaet Dresden, DE; [4]SNT University of Luxembourg, LU; [5]Technische Universität Dresden, DE; [6]NaMLab gGmbH and CfAED, DE; [7]NaMLab Gmbh / TU Dresden, DE

1730 **Automatic Place-and-Route of emerging LED-driven wires within a monolithically-integrated CMOS+III-V process**

Speaker: Tushar Krishna, Georgia Institute of Technology, US
Authors: Tushar Krishna[1], Arya Balachandran[2], Siau Ben Chiah[2], Li Zhang[3], Bing Wang[3], Cong Wang[2], Kenneth Lee Eng Kian[3], Jurgen Michel[4] and Li-Shiuan Peh[5]
[1]Georgia Institute of Technology, US; [2]NTU, SG; [3]SMART, SG; [4]MIT, US; [5]Professor, National University of Singapore, SG

1800 **A Tunable Magnetic Skyrmion Neuron Cluster for Energy Efficient Artificial Neural Network**

Speaker: Deliang Fan, University of Central Florida, US
Authors: Zhezhi He[1] and Deliang Fan[2]
[1]Department of ECE, University of Central Florida, US; [2]University of Central Florida, US

IPs **IP2-1, IP2-2, IP2-3, IP2-4**

4.3 Efficient memory design

2BC 1700 - 1830

Chair: Francisco Cazorla, CSIC and BSC, ES
Co-Chair: Cristina Silvano, Politecnico di Milano, IT

This session presents four papers on novel memory designs and efficient mapping in flash storage. The first two papers improve energy efficiency, with approximate caches on emerging technologies and with a novel DRAM tag-cache architecture. The third paper presents an energy-efficient memory hierarchy through software managed memories. At last, the session concludes with an adaptive page re-mapping architecture in flash-based storage with improved response time.

1700 **STAxCache: An Approximate, Energy Efficient STT-MRAM Cache**

Speaker: Ashish Ranjan, Purdue University, US
Authors: Ashish Ranjan[1], Swagath Venkataramani[1], Zoha Pajouhi[1], Rangharajan Venkatesan[2], Kaushik Roy[1] and Anand Raghunathan[1]
[1]Purdue University, US; [2]NVIDIA, US

1730 **Rethinking On-chip DRAM Cache for Simultaneous Performance and Energy Optimization**

Speaker: Fazal Hameed, Center for Advancing Electronics Dresden (cfaed), Technische Universitat Dresden, Germany, DE
Authors: Fazal Hameed[1] and Jeronimo Castrillon[2]
[1]Chair of Compiler Construction, TU-Dresden, DE; [2]TU Dresden, DE

1800 **An Energy-Efficient Memory Hierarchy for Multi-Issue Processors**

Speaker: Luigi Carro, Universidade Federal do Rio Grande do Sul, BR
Authors: Tiago Jost, Gabriel Nazar and Luigi Carro, UFRGS, BR

1815 **Mapping Granularity Adaptive FTL Based on Flash Page Re-programming**

Speaker: Yazhi Feng, Wuhan National Lab for Optoelectronics, School of Computer Science and Technology, Huazhong University of Science and Technology, CN
Authors: Yazhi Feng, Dan Feng, Chenye Yu, Wei Tong and Jingning Liu, Wuhan National Lab for Optoelectronics, School of Computer Science and Technology, Huazhong University of Science and Technology, Wuhan, China, CN

IPs **IP2-5, IP2-6, IP2-7**

4.4 From functional validation to functional qualification

3A 1700 - 1830

Chair: Graziano Pravadelli, University of Verona, IT
Co-Chair: Elena Ioana Vatajelu, TIMA Laboratory, FR

The section presents techniques and tools to generate testcases for functional validation and to define coverage metrics for functional qualification.

1700 **Data Flow Testing for Virtual Prototypes**

Speaker: Muhammad Hassan, University of Bremen, DE
Authors: Muhammad Hassan[1], Vladimir Herdt[1], Hoang M. Le[1], Mingsong Chen[2], Daniel Grosse[3] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]East China Normal University, CN; [3]University of Bremen/DFKI, DE

1730 **MINIME-Validator: Validating Hardware with Synthetic Parallel Testcases**

Speaker: Alper Sen, Bogazici University, TR
Authors: Alper Sen[1], Etem Deniz[2] and Brian Kahne[3]
[1]Bogazici University, TR; [2]TUBITAK, TR; [3]NXP, US

1800 **Cost-Effective Analysis of Post-Silicon Functional Coverage Events**

Speaker: Avi Ziv, IBM Research - Haifa, IL
Authors: Farimah Farahmandi[1], Ronny Morad[2], Avi Ziv[2], Ziv Nevo[2] and Prabhat Mishra[1]
[1]University of Florida, US; [2]IBM Research - Haifa, IL

IPs **IP2-8, IP2-9**

4.5 Hot Topic Session: On How to Design and Manage Exascale Computing System Technologies

3C 1700 - 1830

Organiser: Donatella Sciuto, Politecnico di Milano, IT
Chair: Donatella Sciuto, Politecnico di Milano, IT
Co-Chair: José L. Ayala, Universidad Complutense de Madrid, ES

The growing race towards exascale computing is pushing the adoption of ever more heterogeneous systems into mainstream. The resources available on a chip, the level of integration and the speed of components have increased dramatically over the years. Moreover, To handle the stringent performance requirements of future exascale-class applications, High Performance Computing (HPC) systems need ultra-efficient heterogeneous compute nodes. However, we keep on adopting superseded approaches to the exploitation of these resources. In this session, the speakers will focus on this requirements providing insight on how to enable the definition and the efficient deployment of such a technology.

1700 **Towards Exascale Computing with Heterogeneous Architectures**

Speaker: Kenneth O'Brien, Xilinx Inc., IE
Authors: Kenneth O'Brien[1], Lorenzo Di Tucci[2], Gianluca Durelli[1] and Michaela Blott[1]
[1]Xilinx, IE; [2]Politecnico di Milano, IT

1718 **From exaflop to exaflow**

Speaker: Tobias Becker, Maxeler Technologies, GB
Authors: Tobias Becker[1], Pavel Burovskiy[2], Anna Maria Nestorov[3], Hristina Palikareva[2], Enrico Reggiani[3] and Georgi Gaydadjiev[4]
[1]Maxeler Technologies, GB; [2]Maxeler Technologies Ltd, GB; [3]Politecnico di Milano, IT; [4]Maxeler / Imperial College, GB

1736 **Heterogeneous exascale supercomputing: the role of CAD in the exaFPGA project**

Speaker: Marco Santambrogio, Politecnico di Milano, IT
Authors: Marco Rabozzi, Giuseppe Natale, Emanuele Del Sozzo, Alberto Scolari, Marco D. Santambrogio and Luca Stornaiuolo, Politecnico di Milano, IT

1754 **An Open Reconfigurable Research Platform as Stepping Stone to Exascale High-Performance Computing**

Speaker: Dirk Stroobandt, Ghent University, BE
Authors: Dirk Stroobandt[1], Catalin Bogdan Ciobanu[2], Marco D. Santambrogio[3], Jose Gabriel Coutinho[4], Andreas Brokalakis[5], Dionisios Pnevmatikatos[6], Michael Huebner[7], Tobias Becker[8] and Alex J. W. Thom[9]
[1]Ghent University, BE; [2]UvA, NL; [3]Politecnico di Milano, IT; [4]Imperial College London, GB; [5]Synelixis, GR; [6]ECE Department, Technical Univrsity of Crete & FORTH-ICS, GR; [7]Ruhr-University Bochum, DE; [8]Maxeler Technologies, GB; [9]University of Cambridge, GB

1812 **GEOPM: A Vehicle for exascale Community Collaboration Toward Co-Designed Energy Management Solutions**

Speaker: Matthias Maiterth, Intel, US
Author: Jonathan Eastep, Intel, US

4.6 Fault modeling, test generation and diagnosis

5A 1700 - 1830

Chair: Stephan Eggersgluss, University of Bremen, DE
Co-Chair: Martin Keim, Mentor, DE

This session includes a presentation about new SAT-based ATPG techniques for robust initialization of transistor stuck-open faults. Further, a diagnosis method for arbiter physical unclonable functions to identify systematic manufacturing issues is presented. The last paper analyzes failure modes of Flash memories and proposes suitable fault models.

1700 **Fast and Waveform-Accurate Hazard-Aware SAT-Based TSOF ATPG**

Speaker: Jan Burchard, University of Freiburg, DE
Authors: Jan Burchard[1], Dominik Erb[1], Adit D. Singh[2], Sudhakar M. Reddy[3] and Bernd Becker[1]
[1]University of Freiburg, DE; [2]Auburn University, US; [3]University of Iowa, US

1730 **Fault Diagnosis of Arbiter Physical Unclonable Function**

Speaker: Yu Hu, Institute of Computing Technology, Chinese Academy of Sciences, CN
Authors: Jing Ye[1], Qingli Guo[2], Yu Hu[1] and Xiaowei Li[1]
[1]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, CN; [2]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences, CN

1800 **FPGA-Based Failure Mode Testing and Analysis for MLC NAND Flash Memory**

Speaker: Fei Wu, Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, CN
Authors: Meng Zhang[1], Fei Wu[1], Qian Xia[1], He Huang[1], Jian Zhou[2] and Changsheng Xie[1]
[1]Huazhong University of Science and Technology, CN; [2]University of Central Florida, US

IPs **IP2-10, IP2-11, IP2-12**

4.7 Process variation management for today's and tomorrow's computing

3B 1700 - 1830

Chair: Mohamed Sabry, Stanford University, US

The session covers variable-aware solutions at the system and circuit level. Firstly, neuromorphic circuits are addressed and its relation with process variation. After that, variability is again addressed but, this time, for entire computing systems.

1700 **Robust Neuromorphic Computing in the Presence of Process Variation**

Speaker: Mehdi Kamal, University of Tehran, IR
Authors: Ali BanaGozar[1], Mohammad Ali Maleki[1], Mehdi Kamal[1], Ali Afzali-Kusha[1] and Massoud Pedram[2]
[1]University of Tehran, IR; [2]University of Southern California, US

1730 **An On-Line Framework for Improving Reliability of Real-Time Systems on "Big-Little" Type MPSoCs**

Speaker: Yue Ma, University of Notre Dame, US
Authors: Yue Ma[1], Thidapat Chantem[2], Robert Dick[3], Shige Wang[4] and X, Sharon Hu[1]
[1]University of Notre Dame, US; [2]Virginia Polytechnic Institute and State University, US; [3]University of Michigan and Stryd, US; [4]General Motors R&D, US

1800 **Application Performance Improvement By Exploiting Process Variability On FPGA Devices**

Speaker: Konstantinos Maragos, National Technical University of Athens, GR
Authors: Konstantinos Maragos[1], George Lentaris[1], Kostas Siozios[1], Dimitrios Soudris[1] and Vasilis Pavlidis[2]
[1]National Technical University of Athens, GR; [2]The University of Manchester, GR

4.8 CV Fair DATE 2017

Exhibition Theatre 1700 - 1830

Organiser: Marisa Lopez-Vallejo, UPM, ES
Moderator: Marisa Lopez-Vallejo, UPM, ES

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WEDNESDAY 29 MARCH, 2017

5.1 IoT Day: IoT Perspectives

5BC 0830 - 1000

Organisers: Marilyn Wolf, Georgia Tech, US
Andreas Herkersdorf, TU Muenchen, DE
Chair: Marilyn Wolf, Georgia Tech, US
Co-Chair: Andreas Herkersdorf, TU Muenchen, DE

The DATE 2017 Special Day on IoT will be kicked-off by perspective talks from academia and industry sharing their views and experience from backgrounds of large distributed sensor networks and cognitive computing. The entire spectrum of IoT devices and computing, storage and communication infrastructure, from smallest form factor sensors to Cloud backbone systems will be considered

0830 **Design for IoT**

Speaker and Author: Lothar Thiele, Swiss Federal Institute of Technology Zurich, CH

0915 **The Internet of Things in the Cognitive Era**

Speaker and Author: Alesandro Curioni, IBM Zurich Research, CH

1000 Coffee Break in Exhibition Area

5.2 Emerging Computer Paradigms

4BC 0830 - 1000

Chair: Jim Harkin, Ulster University, GB

This session presents recent advances in emerging computing strategies including Reversible Computing and Stochastic Computing with improvements in energy efficiency and reductions in computational complexity. An acceleration platform for the design exploration of Quantum Computers is also presented.

0830 **Make It Reversible: Efficient Embedding of Non-reversible Functions**

Speaker: Alwin Zulehner, Johannes Kepler University, Linz, AT
Authors: Alwin Zulehner[1] and Robert Wille[2]
[1]Johannes Kepler University, AT; [2]Johannes Kepler University Linz, AT

0900 **QX: A High-Performance Quantum Computer Simulation Platform**

Speaker: Nader Khammassi, QuTech, Computer Engineering Lab, Delft University of Technology, NL
Authors: Nader Khammassi, Imran Ashraf, Xiang Fu, Carmina Garcia Almudever and Koen Bertels, QuTech, Computer Engineering Lab, Delft University of Technology, NL

0930 **Design Automation and Design Space Exploration for Quantum Computers**

Speaker: Mathias Soeken, EPFL, CH
Authors: Mathias Soeken[1], Martin Roetteler[2], Nathan Wiebe[2] and Giovanni De Micheli[1]
[1]EPFL, CH; [2]Microsoft Research, US

IPs **IP2-13, IP2-14**

1000 Coffee Break in Exhibition Area

5.3 Hot Topic Session: I'm Gonna Make an Approximation IoT Can't Refuse - Approximate Computing for Improving Power Efficiency of IoT and HPC

2BC 0830 - 1000

Organiser: Vincent Camus, EPFL, CH
Chair: Christian Enz, EPFL, CH
Co-Chair: Anca Molnos, CEA Leti, FR

Power efficiency is the primary concern of IoT-related applications, both at the sensor node and on its cloud-computing counterpart. Unfortunately, achieving high efficiency and robustness requires complex and conflicting design constraints. Fortunately, the inherent error resiliency of many IoT applications allows the use of Approximate Computing techniques at both hardware and software levels, leading to great benefits on power efficiency while having a minimal impact on the applications.

0830 **Introduction**
Christian Enz, EPFL, CH

0845 **Pushing the limits of voltage over-scaling for error-resilient applications**
Speaker: Olivier Sentieys, INRIA, FR
Authors: Rengerajan Ragavan[1], Benjamin Barrois[2], Cedric Killian[1] and Olivier Sentieys[1]
[1]INRIA, FR; [2]University of Rennes - INRIA, FR

0900 **Combining Structural and Timing Errors in Overclocked Inexact Speculative Adders**
Speaker: Vincent Camus, EPFL, CH
Authors: Xun Jiao[1], Vincent Camus[2], Mattia Cacciotti[2], Yu Jiang[3], Christian Enz[2] and Rajesh Gupta[1]
[1]UC San Diego, US; [2]EPFL, CH; [3]Tsinghua University, CN

0915 **DVAFS: Trading Computational Accuracy for Energy Through Dynamic-Voltage-Accuracy-Frequency-Scaling**
Speaker: Bert Moons, KU Leuven, BE
Authors: Bert Moons, Roel Uytterhoeven, Wim Dehaene and Marian Verhelst, KU Leuven, BE

0930 **Exploiting computation skip to reduce energy consumption by approximate computing, an HEVC encoder case study**
Speaker: Daniel Menard, INSA Rennes, FR
Authors: Alexandre Mercat[1], Justine Bonnot[1], Maxime Pelcat[2], Wassim Hamidouche[1] and Daniel Menard[1]
[1]INSA Rennes, FR; [2]IETR-INSA, FR

0945 **Location Detection for Navigation Using IMUs with a Map Through Coarse-Grained Machine Learning**
Speaker: Anshumali Shrivastava, Rice University, US
Authors: J. Jose Gonzales E.[1], Chen Luo[1], Anshumali Shrivastava[1], Krishna Palem[1], Moon Yongshik[2], Soonhyun Noh[2], Daedong Park[3] and Seongsoo Hong[2]
[1]Rice University, US; [2]Seoul National University, KR; [3]Dept. of Electrical and Computer Engineering, Seoul National University, KR

1000 Coffee Break in Exhibition Area

5.4 Solutions for efficient simulation and validation

3A 0830 - 1000

Chair: Daniel Grosse, University of Bremen, DE
Co-Chair: Alper Sen, Bogazici University, TR

The section introduces system-level frameworks for addressing memory tracing, timing estimation, real-time verification, and reliability degradation.

WEDNESDAY 29 MARCH, 2017

0830 **Performance Impacts and Limitations of Hardware Memory-Access Trace-Collection**

Speaker: Graham Holland, Simon Fraser University, CA
Authors: Nicholas C. Doyle[1], Eric Matthews[1], Graham Holland[1], Alexandra Fedorova[2] and Lesley Shannon[1]
[1]Simon Fraser University, CA; [2]University of British Columbia, CA

0900 **Context-Sensitive Timing Automata for Fast Source Level Simulation**

Speaker: Sebastian Ottlik, FZI Research Center for Information Technology, DE
Authors: Sebastian Ottlik[1], Christoph Gerum[2], Alexander Viehl[3], Wolfgang Rosenstiel[4] and Oliver Bringmann[4]
[1]FZI Research Center for Information Technology, DE; [2]University of Tuebingen, DE; [3]FZI Forschungszentrum Informatik, DE; [4]University of Tuebingen / FZI, DE

0930 **MARS: A Flexible Real-time Streaming Platform for Testing Automation Systems**

Speaker: Alexandru Moga, ABB Research, CH
Authors: Raphael Eidenbenz, Alexandru Moga, Thanikesavan Sivanthi and Carsten Franke, ABB Corporate Research, CH

0945 **SERD: A Simulation Framework for Estimation of System Level Reliability Degradation**

Speaker: Saurav Ghosh, IIT Kharagpur, IN
Authors: Saurav Kumar Ghosh[1] and Dey Soumyajit[2]
[1]Dept. of CSE, IIT Kharagpur, IN; [2]IIT Kharagpur, IN

IPs **IP2-15, IP2-16, IP2-19**

1000 Coffee Break in Exhibition Area

5.5 Hot Topic Session: Spintronics-based Computing

3C 0830 - 1000

Organisers: Lionel Torres, LIRMM, CNRS/University of Montpellier, FR
Weisheng Zhao, Beihang University, CN
Chair: Lionel Torres, LIRMM, CNRS/University of Montpellier, FR
Co-Chair: Weisheng Zhao, Beihang University, CN

Numerous reports or industrial and academic works on emerging research devices identified magnetic tunnel junction (MTJ) (one of applications of Spintronics) as one of the most promising technologies to be part of the future of integrated systems. They provide non-volatility data, fast data access and low power operations. Indeed, MRAM or Magnetic memory based on the hybrid integration of MTJ have been commercialized since 2006 and used in a number of high-reliable applications. The aim of this session is to bring together the worldwide leading experts (from respectively USA, France, China, Japan and Germany) related to this hot topic to share the most recent results and discuss the future challenges. Different computing paradigms will be involved in this special session benefiting from interesting nature of spintronics devices. The invited speakers will talk about devices, design and compact modeling aspects, and applications, permitting a full development platform from devices to circuit & systems based on spintronics.

0830 **Magnetic Tunnel Junction Enabled All-Spin Stochastic Spiking Neural Network**

Speaker: Kaushik Roy, Purdue University, US
Authors: Gopalakrishnan Srinivasan, Abhronil Sengupta and Kaushik Roy, Purdue University, US

0848 **Embedded Systems to High Performance Computing using STT-MRAM**

Speaker: Sophiane Senni, LIRMM, FR
Authors: Sophiane Senni[1], Thibaud Delobelle[1], Odilia Coi[1], Pierre-Yves Péneau[2], Lionel Torres[3], Abdoulaye Gamatie[4], Pascal Benoit[3] and Gilles Sassatelli[5]
[1]LIRMM, FR; [2]LIRMM - CNRS, FR; [3]University of Montpellier, FR; [4]CNRS LIRMM / University of Montpellier, FR; [5]LIRMM CNRS / University of Montpellier, FR

0906 **Voltage-Controlled MRAM for Working Memory: Perspectives and Challenge**

Speaker: Wang Kang, Beihang University, CN
Authors: Wang Kang, Liang Chang, Youguang Zhang and Weisheng Zhao, Beihang University, CN

0924 **Three-Terminal MTJ-Based Nonvolatile Logic Circuits with Self-Terminated Writing Mechanism for Ultra-Low-Power VLSI Processor**

Speaker: Takahiro Hanyu, RIEC, Tohoku University, JP
Authors: Takahiro Hanyu, Daisuke Suzuki, Naoya Onizawa and Masanori Natsui, Tohoku University, JP

0942 **Opportunistic Write for Fast and Reliable STT-MRAM**

Speaker: Mehdi Tahoori, Karlsruhe Institute of Technology, DE
Authors: Nour Sayed[1], Mojtaba Ebrahimi[1], Rajendra Bishnoi[2] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]Karlsruhe Instituite of Technology, DE

1000 Coffee Break in Exhibition Area

5.6 Reuse and Integration of Test, Debug, and Reliability Infrastructure

5A 0830 - 1000

Chair: Paolo Bernardi, Politecnico di Torino, IT
Co-Chair: Alberto Bosio, LIRMM, FR

This session deals with 3D reliability and repair, integration of compression into standard test infrastructure, and reusing silicon debug infrastructure to enhance functional performance.

0830 **Fault Clustering Technique for 3D Memory BISR**

Speaker: Tianjian Li, Shanghai Jiao Tong University, CN
Authors: Tianjian Li[1], Yan Han[1], Xiaoyao Liang[1], Hsien-Hsin S. Lee[2] and Li Jiang[3]
[1]Shanghai Jiao Tong University, CN; [2]TSMC / Georgia Tech, TW; [3]Department of Computer Science and Engineering, Shanghai Jiao Tong University, CN

0900 **Architectural Evaluations on TSV Redundancy for Reliability Enhancement**

Speaker: Yen-Hao Chen, National Tsing Hua University, Taiwan, TW
Authors: YenHao Chen[1], Chien-Pang Chiu[1], Russell Barnes[2] and TingTing Hwang[1]
[1]National Tsing Hua University, R.O.C, TW; [2]University of California at Santa Barbara, US

0930 **Reusing Trace Buffers to Enhance Cache Performance**

Speaker: Neetu Jindal, PhD, IN
Authors: Neetu Jindal, Preeti Ranjan Panda and Smruti R. Sarangi, Indian Institute of Technology Delhi, IN

0945 **Optimization of Retargeting for IEEE 1149.1 TAP Controllers with Embedded Compression**

Speaker: Sebastian Huhn, University of Bremen, DE
Authors: Sebastian Huhn[1], Stephan Eggersglüß[1], Krishnendu Chakrabarty[2] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]Duke University, US; [3]University of Bremen/DFKI, DE

IPs **IP2-17**

1000 Coffee Break in Exhibition Area

5.7 Schedulability Analysis

3B 0830 - 1000

Chair: Rodolfo Pellizzoni, University of Waterloo, CA
Co-Chair: Petru Eles, Linköpings universitet, SE

The papers in this session introduce new schedulability analyses for real-time systems, including systems with precedence constraints, real-time networks-on-chip, and mixed-critical systems.

0830 **Bounding Deadline Misses in Weakly-hard Real-Time Systems with Task Dependencies**
Speaker: Zain A. H. Hammadeh, TU Braunschweig, DE
Authors: Zain A. H. Hammadeh[1], Sophie Quinton[2], Rolf Ernst[1], Rafik Henia[3] and Laurent Rioux[3]
[1]TU Braunschweig, DE; [2]Inria, FR; [3]Thales Research & Technology, FR

0900 **Real-Time Communication Analysis for Networks-on-Chip with Backpressure**
Speaker: Sebastian Tobuschat, TU Braunschweig, DE
Authors: Sebastian Tobuschat and Rolf Ernst, TU Braunschweig, DE

0930 **Probabilistic Schedulability Analysis for Fixed Priority Mixed Criticality Real-Time Systems**
Speaker: Yasmina Abdeddaïm, Université Paris-Est, LIGM, ESIEE Paris, FR
Authors: Yasmina ABDEDDAÏM[1] and Dorin Maxim[2]
[1]Université Paris-Est, LIGM, ESIEE-Paris, FR; [2]University of Lorraine - Loria - Inria Nancy Grand Est, FR

1000 Coffee Break in Exhibition Area

IP2 Interactive Presentations

IP sessions (in front of rooms 4A and 5A) 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. At the end of each afternoon Interactive Presentations session the award 'Best IP of the Day' is given.

IP2-1 **Compact Modeling and Circuit-Level Simulation of Silicon Nanophotonic Interconnects**
Speaker: Yuyang Wang, UC Santa Barbara, US
Authors: Rui Wu[1], Yuyang Wang[2], Zeyu Zhang[2], Chong Zhang[2], Clint Schow[2], John Bowers[2] and Kwang-Ting Cheng[2]
[1]UC Santa Barbara, US; [2]UCSB, US

IP2-2 **A True Random Number Generator based on Parallel STT-MTJs**
Speaker: Yuanzhuo Qu, University of Alberta, CA
Authors: Yuanzhuo Qu[1], Jie Han[1], Bruce Cockburn[1], Yue Zhang[2], Weisheng Zhao[2] and Witold Pedrycz[1]
[1]University of Alberta, CA; [2]Beihang University, CN

IP2-3 **Enabling Area Efficient RF ICs through Monolithic 3D Integration**
Speaker: Panagiotis Chaourani, KTH, Royal Institute of Technology, Stockholm, SE
Authors: Panagiotis Chaourani, Per-Erik Hellström, Saul Rodriguez, Raul Onet and Ana Rusu, KTH, Royal Institute of Technology, SE

IP2-4 **Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors**
Speaker: Baris Taskin, Drexel University, US
Authors: Ragh Kuttappa, Lunal Khuon, Bahram Nabet and Baris Taskin, Drexel University, US

IP2-5 **i-BEP: A Non-Redundant and High-Concurrency Memory Persistency Model**
Speaker: Yuanchao Xu, Capital Normal University, CN
Authors: Yuanchao Xu, Zeyi Hou, Junfeng Yan, Lu Yang and Hu Wan, Capital Normal University, CN

IP2-6 **SPMS: Strand based Persistent Memory System**
Speaker: Shuo Li, National University of Defense Technology, CN
Authors: Shuo Li[1], Peng Wang[2], Nong Xiao[1], Guangyu Sun[2] and Fang Liu[1]
[1]National University of Defense Technology, CN; [2]Peking University, CN

IP2-7 **Architecting High-Speed Command Schedulers for Open-Row Real-Time SDRAM Controllers**
Speaker: Leonardo Ecco, TU Braunschweig, DE
Authors: Leonardo Ecco[1] and Rolf Ernst[2]
[1]Institute of Computer and Network Engineering, TU Braunschweig, DE; [2]TU Braunschweig, DE

IP2-8 **Automatic Equivalence Checking for SystemC-TLM 2.0 Models Against their Formal Specifications**
Speaker: Mehran Goli, University of Bremen, DE
Authors: Mehran Goli, Jannis Stoppe and Rolf Drechsler, University of Bremen, DE

IP2-9 **Head-Mounted Sensors and Wearable Computing for Automatic Tunnel Vision Assessment**
Speaker: Josue Ortiz, Complutense University of Madrid, ES
Authors: Yuchao Ma and Hassan Ghasemzadeh, Washington State University, US

IP2-10 **RetroDMR: Troubleshooting Non-Deterministic Faults with Retrospective DMR**
Speaker: Ting Wang, The Chinese University of Hong Kong, HK
Authors: Ting Wang[1], Yannan Liu[1], Qiang Xu[1], Zhaobo Zhang[2], Zhiyuan Wang[2] and Xinli Gu[2]
[1]The Chinese University of Hong Kong, HK; [2]Huawei Technologies, Inc., US

IP2-11 **Critical Path - Oriented Thermal Aware X-Filling for High Un-modeled Defect Coverage**
Speaker: Fotios Vartziotis, Computer Engineering, T.E.I. of Epirus, Greece, GR
Authors: Fotios Vartziotis[1] and Chrysovalantis Kavousianos[2]
[1]TEI of Epirus, University of Ioannina, GR; [2]Department of Computer Science and Engineering, University of Ioannina, GR

IP2-12 **A Comprehensive Methodology for Stress Procedures Evaluation and Comparison for Burn-In of Automotive SoC**
Speaker: Paolo Bernardi, Politecnico di Torino, IT
Authors: Paolo Bernardi[1], Davide Appello[2], Giampaolo Giacopelli[2], Alessandro Motta[2], Alberto Pagani[2], Giorgio Pollaccia[3], Christian Rabbi[2], Marco Restifo[1], Priit Ruberg[4], Ernesto Sanchez[1], Claudio Maria Villa[2] and Federico Venini[1]
[1]Politecnico di Torino, IT; [2]STMicroelectronics, IT; [3]STMicroelectonics, IT; [4]Tallinn University of Technology, EE

IP2-13 **Energy Efficient Stochastic Computing with Sobol Sequences**
Speaker: Siting Liu, University of Alberta, CA
Authors: Siting Liu and Jie Han, University of Alberta, CA

IP2-14 **Logic Analysis and Verification of n-input Genetic Logic Circuits**
Speaker: Hasan Baig, Technical University of Denmark, DK
Authors: Hasan Baig and Jan Madsen, Technical University of Denmark, DK

IP2-15 **A novel way to efficiently simulate complex full systems incorporating hardware accelerators**
Speaker: Nikolaos Tampouratzis, Technical University of Crete, GR
Authors: Nikolaos Tampouratzis[1], Konstantinos Georgopoulos[2] and Ioannis Papaefstathiou[3]
[1]Technical University of Crete, GR; [2]Telecommunication Systems Institute, Technical University of Crete, GR; [3]Technical university of Crete, GR

IP2-16 **Automatic Abstraction of Multi-Discipline Analog Models for Efficient Functional Simulation**
Speaker: Franco Fummi, Università degli Studi di Verona, IT
Authors: Enrico Fraccaroli[1], Michele Lora[1] and Franco Fummi[2]
[1]University of Verona, IT; [2]Universita' di Verona, IT

IP2-17 **Novel Magnetic Burn-In for Retention Testing of STTRAM**
Speaker: Swaroop Ghosh, Pennsylvania State University, US
Authors: Mohammad Nasim Imtiaz Khan, Anirudh Iyengar and Swaroop Ghosh, Pennsylvania State University, US

IP2-19 **Automatic Construction of Models for Analytic System-Level Design Space Exploration Problems**
Speaker: Seyed-Hosein Attarzadeh-Niaki, Shahid Beheshti University (SBU), IR
Authors: Seyed-Hosein Attarzadeh-Niaki[1] and Ingo Sander[2]
[1]Shahid Beheshti University (SBU), IR; [2]KTH Royal Institute of Technology, SE

1100 Session 6

WEDNESDAY 29 MARCH, 2017

6.1 IoT Day Hot Topic Session: IoT Enabling Technologies

5BC 1100 - 1230

Organisers: Marilyn Wolf, Georgia Tech, US
Andreas Herkersdorf, TU Muenchen, DE
Chair: Andreas Herkersdorf, TU Muenchen, DE
Co-Chair: Marilyn Wolf, Georgia Tech, US

The introduction and broad scale rollout of IoT applications puts pressing demands on semiconductor base technologies for computation, communication and sensing in terms of lowest cost, power dissipation, dependability, security and the ability to integrate heterogeneous devices and technologies. This session presents three research-oriented perspectives on the challenging aspects of IoT enabling technologies

1100 **Ultra-low-power circuits for IoT applications**
Speaker and Author: Georges Gielen, KU Leuven, BE

1130 **Structural Health Monitoring for Smart Cities: a HW/SW Codesign Perspective**
Speaker and Author: Jiang Xu, Hong Kong University of Science and Technology, HK

1200 **Security in the Internet of Things: A Challenge of Scale**
Speaker and Author: Patrick Schaumont, Virginia Tech, US

1230 Lunch Break in Garden Foyer

6.2 IT&A Session: Panel: Ultra-Low-Power (ULP) Autonomously Powered Systems

4BC 1100 - 1230

Chair: Jamil Kawa, Synopsys, US

In this executive session, we will discuss the prominent features and requirements of today's autonomously powered systems and deliberate over various visions of what needs to happen next to take autonomously powered systems from their embryonic state to an advanced efficient state that is well thought through and efficiently architectured.

Moderator:

Jamil Kawa, Synopsys, US

Panelists:

Christopher Van Hoof, IMEC, BE
Christoph Heer, Intel, DE
Krisztian Flautner, ARM, US
Yankin Tanurhan, Synopsys, US
Ali Keshavarzi, Cypress Semiconductor, US

1230 Lunch Break in Garden Foyer

6.3 Security Primitives

2BC 1100 - 1230

Chair: Berndt Gammel, Infineon, DE
Co-Chair: Tim Güneysu, University of Bremen & DFKI, DE

This session discusses the implementation of basic primitives that are necessary building blocks for the secure systems: Physical unclonable functions (PUFs) are used for creating secret values which then are used as keys in cryptographic algorithms. Logical and physical security of these systems fundamentally relies on the presence of high quality random numbers.

1100 **Sensitized Path PUF: A Lightweight Embedded Physical Unclonable Function**

Speaker: Matthias Sauer, University of Freiburg, DE
Authors: Matthias Sauer[1], Pascal Raiola[1], Linus Feiten[1], Bernd Becker[1], Ulrich Rührmair[2] and Ilia Polian[3]
[1]University of Freiburg, DE; [2]TU München, DE; [3]University of Passau, DE

1130 **Temperature Aware Phase/Frequency Detector-based RO-PUFs Exploiting Bulk-Controlled Oscillators**

Speaker: Sha Tao, Royal Institute of Technology (KTH), SE
Authors: Sha Tao and Elena Dubrova, Royal Institute of Technology (KTH), SE

1200 **ChaCha20-Poly1305 Authenticated Encryption for High-Speed Embedded IoT Applications**

Speaker: Fabrizio De Santis, Technische Universität München, DE
Authors: Fabrizio De Santis, Andreas Schauer and Georg Sigl, Technische Universität München, DE

1215 **Towards Post-Quantum Security for IoT Endpoints with NTRU**

Speaker: Johanna Sepulveda, TU Munich, DE
Authors: Oscar M. Guillen[1], Thomas Pöppelmann[2], Jose M. Bermudo Mera[1], Elena Fuentes Bongenaar[3], Georg Sigl[1] and Johanna Sepulveda[1]
[1]TU München, DE; [2]Infineon Technologies AG, DE; [3]Radboud University, NL

IPs **IP3-1, IP3-2**

1230 Lunch Break in Garden Foyer

6.4 High-performance Reconfigurable Computing

3A 1100 - 1230

Chair: Philip Brisk, University of California, Riverside, US
Co-Chair: Mirjana Stojilovic, EPFL, CH

Reconfigurable architectures are seeing increased usage in high performance and scientific applications. This session addresses challenges in this space, which include optimizes arithmetic data paths, developing an in-memory architecture for optimizing database processing, and a case study on developing a high throughput Smith-Waterman accelerator.

1100 **Automating the pipeline of arithmetic datapaths**

Speaker: Florent de Dinechin, INSA-Lyon, FR
Authors: Matei Istoan[1] and Florent de Dinechin[2]
[1]INRIA, FR; [2]INSA-Lyon, FR

1130 **Operand Size Reconfiguration for Big Data Processing in Memory**

Speaker: Luigi Carro, UFRGS, BR
Authors: Paulo Cesar Santos[1], Geraldo Francisco de Oliveira Junior[2], Diego Gomes Tomé[3], Marco Antonio Zanata Alves[3], Eduardo Cunha de Almeida[3] and Luigi Carro[4]
[1]UFRGS - Universidade Federal do Rio Grande do Sul, BR; [2]Universidade Federal do Rio Grande do Sul, BR; [3]UFPR, BR; [4]UFRGS, BR

1200 **Architectural Optimizations for High Performance and Energy Efficient Smith-Waterman Implementation on FPGAs using OpenCL**

Speaker: Lorenzo Di Tucci, Politecnico di Milano, IT
Authors: Lorenzo Di Tucci[1], Kenneth O'Brien[2], Michaela Blott[2] and Marco D. Santambrogio[1]
[1]Politecnico di Milano, IT; [2]Xilinx Inc, IE

IPs **IP3-3, IP3-4**

1230 Lunch Break in Garden Foyer

6.5 Hot Topic Session: Memristor for High Performance Computing: Myth or Reality?

3C 1100 - 1230

Organisers: Koen Bertels, Delft University of Technology, NL
Said Hamdioui, Delft University of Technology, NL
Chair: Henk Corporaal, Eindhoven University of Technology, NL
Co-Chair: Koen Bertels, Delft University of Technology, NL

Both today's technology and computer architectures are facing serious challenges/ walls making them incapable to deliver the right computing power at pre-defined constraints for emerging applications such as big-data. However, a solution may be at your fingertips. This session discusses the emerging memristor device in enabling new memory technologies and new logic design styles, as well as its potential in enabling new computing paradigms such as memory intensive architectures and neuromorphic computing, due to its unique properties like the tight integration with CMOS and the ability to learn and adapt

1100 **Memory-Intensive Architectures**
Speaker and Author: Shahar Kvatinsky, Technion/Israel Institute of Technology, IL

1130 **Memristor for Computation-in-Memory**
Speaker and Author: Said Hamdioui, Delft University of Technology, NL

1200 **Nanoscale Neuromorphic Silicon Learning Machines**
Speaker and Author: Gert Cauwenberghs, UC San Diego, US

1230 Lunch Break in Garden Foyer

6.6 Industrial Experiences & EU Projects

5A 1100 - 1230

Chair: Mario Diaz Nava, ST Microelectronics, FR
Co-Chair: Eugenio Villar, University of Cantabria, ES

This session adresses industrial research and practice on architecture, design, timing analysis techniques and analogue circuit sizing. The session will be rounded off by presentations of two European projects about to start, addressing cross-layer design of reconfigurable CPS and IoT for smart wearable applications.

1100 **An Asynchronous NoC Router in a 14nm FinFET Library: Comparison to an Industrial Synchronous Counterpart**
Speaker: Wayne Burleson, Advanced Micro Devices, Inc., US
Authors: Weiwei Jiang[1], Davide Bertozzi[2], Gabriele Miorandi[2], Steven M. Nowick[1], Wayne Burleson[3] and Greg Sadowski[3]
[1]Columbia University, US; [2]University of Ferrara, IT; [3]Advanced Micro Devices, US

1115 **An Advanced Embedded Architecture for Connected Component Analysis in Industrial Applications**
Speaker: Menbere Tekleyohannes, University of Kaiserslautern, DE
Authors: Menbere Tekleyohannes[1], Mohammadsadegh Sadri[1], Martin Klein[2], Michael Siegrist[2], Christian Weis[1] and Norbert Wehn[1]
[1]University of Kaiserslautern, DE; [2]Wipotec GmbH, DE

1130 **Workload Dependent Reliability Timing Analysis Flow**
Speaker: Ajith Sivadasan, TIMA Labs, IN
Authors: Ajith Sivadasan[1], Armelle Notin[2], Vincent Huard[2], Etienne Maurin[3], Florian Cacho[3], Sidi Ahmed Benhassain[4] and Lorena Anghel[5]
[1]TIMA Labs, FR; [2]ST Microelectronics, FR; [3]St Microelectronics, FR; [4]TIMA, FR; [5]Grenoble-Alpes University, FR

1145 **Probabilistic Timing Analysis on Time-Randomized Platforms for the Space Domain**

Speaker: Francisco J. Cazorla, Barcelona Supercomputing Center and Spanish National Research Council (IIIA-CSIC), ES
Authors: Mikel Fernandez[1], David Morales[2], Leonidas Kosmidis[3], Alen Bardizbanyan[4], Ian Broster[5], Carles Hernandez[1], Eduardo Quinones[1], Jaume Abella[6], Francisco Cazorla[7], Paulo Machado[8] and Luca Fossati[8]
[1]Barcelona Supercomputing Center, ES; [2]BSC, ES; [3]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [4]Chalmers University of Technology, SE; [5]Rapita Systems LTD, GB; [6]Barcelona Supercomputing Center (BSC-CNS), ES; [7]Barcelona Supercomputing Center and IIIA-CSIC, ES; [8]ESA, IT

1200 **Cross-layer Design of Reconfigurable Cyber-Physical Systems**

Speaker and Author: Michael Masin, IBM Research, IL

1215 **INSPEX: design and integration of a portable/wearable smart spatial exploration system**

Speaker and Author: Suzanne Lesecq, CEA-LETI, FR

IPs **IP3-5**

1230 Lunch Break in Garden Foyer

6.7 Model-Based Design and Verification of Real-Time Systems

3B 1100 - 1230

Chair: Alain Girault, INRIA, FR
Co-Chair: Amir Aminifar, IPFL Lausanne, CH

This session provides an overview of recent advances in model based design of embedded real-time systems. The first paper proposes an optimal deployment for data-flow applications on many-core chips. The second paper addresses the issue of simulation-based verification of embedded systems. It considers aspects of model based design of control systems in the context of event based real-time simulation. Last, but not least, the third paper discusses the workload monitoring of real-time systems by relying on a run-time feedback instead of offline assumptions.

1100 **Near-optimal Deployment of Dataflow Applications on Many-core Platforms with Real-time Guarantees**

Speaker: Stefanos Skalistis, École Polytechnique Fédérale de Lausanne (EPFL), GR
Authors: Stefanos Skalistis and Alena Simalatsar, EPFL, CH

1130 **Simulating Preemptive Scheduling with Timing-aware Blocks in Simulink**

Speaker and Author: Andreas Naderlinger, University of Salzburg, AT

1200 **Online Workload Monitoring with the Feedback of Actual Execution Time for Real-Time Systems**

Speaker: Biao Hu, Tech. Univ. Muenchen TUM, DE
Authors: Biao Hu[1], Kai Huang[2], Gang Chen[1], Long Cheng[1] and Alois Knoll[1]
[1]Tech. Univ. Muenchen TUM, DE; [2]Sun Yat-Sen University, CN

IPs **IP3-6**

1230 Lunch Break in Garden Foyer

6.8 HiPEAC: European Network on High Performance and Embedded Architecture and Compilation

Exhibition Theatre 1100 - 1230

Organiser: Catherine Roderick, Barcelona Supercomputing Center, ES
Moderator: Luca Fanucci, University of Pisa, IT

See Page 109

1230 Lunch Break in Garden Foyer

7.0 LUNCH TIME KEYNOTE SESSION

Garden Foyer 1350 - 1420

Chair: David Atienza, EPFL, CH

See Page 9

1350 **Internet of Everything is our Opportunity**

Speaker and Author: Keith Willett, Director of Software Engineering for Merck Serono, CH

1430 Session 7

7.1 IoT Day Hot Topic Session: IoT Deployment

5BC 1430 - 1600

Organisers: Marilyn Wolf, Georgia Tech, US
Andreas Herkersdorf, TU Muenchen, DE
Chair: Marilyn Wolf, Georgia Tech, US
Co-Chair: Andreas Herkersdorf, TU Muenchen, DE

IoT technologies have the potential to be a disruptive game changer for existing applications and services as well as an enabler for new businesses. This session provides viewpoints from industry as well as a startup company on the deployment and evolution of IoT-oriented services and products.

1430 **Designing and launching great IoT products**

Speaker and Author: Adrian Caceres, Ayla Networks, US

1500 **How ASIC development will change for future IoT MEMS sensors**

Speaker and Author: Dirk Droste, Bosch, DE

1530 **Distributed Wayside Architecture - IoT for Railway Infrastructure**

Speaker: Peter Hefti, Siemens, CH
Author: Olivier Kaiser, Siemens, CH

IP7.1.1 **A low-power IoT processor integrating voltage-scalable fully digital memories**

Speaker and Author: Hidetoshi Ondotera, Kyoto University, JP

IP7.1.2 **A simple, stateless, cost effective symmetric encryption strategy for energy-harvesting IoT devices**

Speaker and Author: Jan Madsen, Technical University of Denmark, DK

IP7.1.3 **Reconfigurable microcontroller for end nodes in Internet of Things**

Speaker and Author: Wai-Chung Matthew Tang, Queen Mary University of London, GB

IP7.1.4 **Further simplification of approximate adders using input data ranges in IoT**

Speaker and Author: Jeong-A Lee, Chosun University, KR

1600 Coffee Break in Exhibition Area

7.2 In-memory Computing and Security for Non-volatile Memory Technologies

4BC 1430 - 1600

Chair: Luca Amaru, Synopsys, US
Co-Chair: Pierre-Emmanuel Gaillardon, University of Utah, US

Non-volatile memories (NVMs) are playing an increasingly dominant role in the construction of energy-efficient systems thanks to reduced static power consumption. NVMs raise new opportunities and challenges in terms of enhancing computational efficiency and ensuring security, respectively. This session explores in-memory computing applied to emerging NVM technologies and goes on to investigate security and encryption strategies.

1430 **Automated Synthesis of Compact Crossbars for Sneak-Path based In-Memory Computing**

Speaker: Sumit Kumar Jha, University of Central Florida, US
Authors: Dwaipayan Chakraborty and Sumit Kumar Jha, University of Central Florida, US

1500 **Hybrid Spiking-based Multi-layered Self-learning Neuromorphic System Based On Memristor Crossbar Arrays**

Speaker: Yiran Chen, Professor, US
Authors: Amr Hassan, Chaofei Yang, Chenchen Liu, Hai (Helen) Li and Yiran Chen, University of Pittsburgh, US

1530 **ReVAMP : ReRAM based VLIW Architecture for in-Memory comPuting**

Speaker: Anupam Chattopadhyay, School of Computer Science and Engineering, Nanyang Technological University, SG
Authors: Debjyoti Bhattacharjee, Rajeswari Devadoss and Anupam Chattopadhyay, Nanyang Technological University, SG

IPs **IP3-7, IP3-8, IP3-9**

1600 Coffee Break in Exhibition Area

7.3 Optimizing performance, energy and predictability via hardware/software codesign

2BC 1430 - 1600

Chair: Sasan Avesta, George Mason University, US
Co-Chair: Ramon Canal, UPC, ES

This session presents a variety of architectural solutions to improve performance/energy/predictability covering several hardware blocks: processor pipeline, caches, memory and on-chip I/O. The first paper proposes a hardware/software mechanism to classify accesses as private or shared. The second paper, introduces a low-power asynchronous microprocessor design. The third paper proposes a coordinated approach to improve performance by partitioning multilevel caches. And the last paper proposes a hardware approach to increase the timing accuracy of I/O operations.

1430 **Accurate Private/Shared Classification of Memory Accesses: a Run-time Analysis System for the LEON3 Multi-core Processor**

Speaker: Nam Ho, Department of Computer Science, University of Paderborn, DE
Authors: Nam Ho, Ishraq Ibne Ashraf, Paul Kaufmann and Marco Platzner, Department of Computer Science, University of Paderborn, DE

1500 **Design of a Low Power, Relative Timing based Asynchronous MSP430 Microprocessor**

Speaker: Dipanjan Bhadra, University of Utah, US
Authors: Dipanjan Bhadra and Kenneth Stevens, University of Utah, US

1530 **A Coordinated Multi-Agent Reinforcement Learning Approach to Multi-Level Cache Co-partitioning**

Speaker: Preeti Ranjan Panda, Indian Institute of Technology Delhi, IN
Authors: Rahul Jain[1], Preeti Ranjan Panda[2] and Sreenivas Subramoney[3]
[1]Indian Institute of Technology, Delhi, IN; [2]IIT Delhi, IN; [3]Microarchitecture Research Lab, Intel, IN

1545 **GPIOCP: Timing-Accurate General Purpose I/O Controllerfor Many-core Real-time Systems**

Speaker: Zhe Jiang, University of York, CN
Authors: Zhe Jiang and Neil Audsley, University of York, GB

IPs **IP3-10, IP3-11, IP3-12**

1600 Coffee Break in Exhibition Area

7.4 Advances in Logic Synthesis

3A 1430 - 1600

Chair: Paolo Ienne, EPFL, CH
Co-Chair: Tsutomu Sasao, Meiji University, JP

This session focuses on new results in logic synthesis. The first two papers present specialized synthesis algorithms for index generating functions and encoder circuits. The last two papers discuss efficient encoding with SAT of short-circuit detection and combinational delay optimization.

1430 **An algorithm to find optimum support-reducing decompositions for index generation functions.**

Speaker: Tsutomu Sasao, Meiji University, JP
Authors: Tsutomu Sasao, Kyu Matsuura and Yukihiro Iguchi, Meiji University, JP

1500 **Taking One-to-one Mappings for Granted: Advanced Logic Design of Encoder Circuits**

Speaker: Robert Wille, Johannes Kepler University, Linz, AT
Authors: Alwin Zulehner[1] and Robert Wille[2]
[1]Johannes Kepler University, AT; [2]Johannes Kepler University Linz, AT

1530 **Analysis of Short-Circuit Conditions in Logic Circuits**

Speaker: João Afonso, INESC-ID, PT
Authors: João Pedro[1] and Jose Monteiro[2]
[1]INESC-ID, PT; [2]INESC-ID, IST, U Lisboa, PT

1545 **Busy Man's Synthesis: Combinational Delay Optimization with SAT**

Speaker: Mathias Soeken, EPFL, CH
Authors: Mathias Soeken[1], Giovanni De Micheli[1] and Alan Mishchenko[2]
[1]EPFL, CH; [2]UC Berkeley, US

IPs **IP3-13, IP3-14**

1600 Coffee Break in Exhibition Area

7.5 Hot Topic Session: The Engineering Challenges for Quantum Computing

3C 1430 - 1600

Organisers: Koen Bertels, QuTech & Computer Engineering Lab, NL
Carmen G. Almudéver, QuTech & Computer Engineering Lab, NL
Chair: Edoardo Charbon, Delft University of Technology, NL
Co-Chair: Said Hamdioui, Delft University of Technology, NL

Quantum computers may revolutionize the field of computation by solving some complex problems that are intractable even for the most powerful current supercomputers. This session will explain the basic concepts of quantum computing and describe what the required layers are for building a quantum sys-

tem. The different speakers in the session will then address the engineering challenges when building a quantum computer ranging from the core qubit technology, the control electronics, to the microarchitecture for the execution of quantum circuits and efficient quantum error correction and what compiler and system tools are needed in that context.

1430 **What is quantum computing all about?**
Speaker: Carmen G. Almudever, Delft University of Technology, NL
Authors: Carmen G. Almudever and Koen Bertels, Delft University of Technology, NL

1500 **Quantum processor**
Speaker and Author: Andreas Wallraff, ETH Zurich, CH

1530 **Control electronics for quantum computer**
Speaker and Author: Hendrik Bluhm, RWTH Aachen, DE

1600 Coffee Break in Exhibition Area

7.6 Memory Reliability: Modeling and Mitigation

5A 1430 - 1600

Chair: Jose Pineda De Gyvez, NXP, NL
Co-Chair: Vikas Chandra, ARM, US

This session discusses new trends and solutions to model and mitigate resiliency challenges for advanced memory technologies. The first paper discusses unequal protection for more efficient memory resiliency. The second paper analyzes the aging impact on different memory components. Finally, the third paper proposes mitigation schemes for memory peripheral circuitry.

1430 **MVP ECC : Manufacturing process Variation aware unequal Protection ECC for memory reliability**
Speaker: Joon-Sung Yang, Sungkyunkwan University, KR
Authors: Seungyeob Lee and Joon-Sung Yang, Sungkyunkwan University, KR

1500 **Analyzing the Effects of Peripheral Circuit Aging of Embedded SRAM Architectures**
Speaker: Josef Kinseher, Intel Deutschland, DE
Authors: Josef Kinseher[1], Leonhard Heiß[1] and Ilia Polian[2]
[1]Intel Deutschland, DE; [2]University of Passau, DE

1530 **Mitigation of Sense Amplifier Degradation Using Input Switching**
Speaker: Daniel Kraak, Delft University of Technology, NL
Authors: Daniel Kraak[1], Innocent Agbo[1], Mottaqiallah Taouil[1], Said Hamdioui[1], Pieter Weckx[2], Stefan Cosemans[2], Francky Catthoor[2] and Wim Dehaene[3]
[1]Delft University of Technology, NL; [2]imec, BE; [3]KU Leuven, ESAT, BE

IPs **IP3-15**

1600 Coffee Break in Exhibition Area

7.7 Resource management and analysis for embedded architectures

3B 1430 - 1600

Chair: Akash Kumar, Technische Universitaet Dresden, DE
Co-Chair: Orlando Moreira, Intel, NL

Embedded architectures have to often provide application performance guarantees despite stringent resource constraints. The talks in this session provide solutions to managing the limited resources of such platforms and analysing the impact of resource allocation - both from the power and performance perspective.

1430 **Scalable Probabilistic Power Budgeting for Many-Cores**

Speaker: Anuj Pathania, Karlsruhe Institute of Technology, IN
Authors: Anuj Pathania[1], Heba Khdr[2], Muhammad Shafique[3], Tulika Mitra[4] and Joerg Henkel[5]
[1]Karlsruhe Institute of Technology, DE; [2]Karlsruhe Institute of Technology (KIT), DE; [3]Vienna University of Technology (TU Wien), AT; [4]National University of Singapore, SG; [5]KIT, DE

1500 **Exploiting Sporadic Servers to provide Budget Scheduling for ARINC653 based Real-Time Virtualization Environments**

Speaker: Matthias Beckert, Institute of Computer and Network Engineering, TU Braunschweig, DE
Authors: Matthias Beckert[1], Kai Björn Gemlau[1] and Rolf Ernst[2]
[1]Institut für Datentechnik und Kommunikationsnetze - TU Braunschweig, DE; [2]TU Braunschweig, DE

1530 **Programming and Analysing Scenario-Aware Dataflow on a Multi-Processor Platform**

Speaker: Reinier van Kampenhout, Eindhoven University of Technology, NL
Authors: Reinier van Kampenhout, Sander Stuijk and Kees Goossens, Eindhoven University of Technology, NL

IPs **IP3-16, IP3-17, IP3-18**

1600 Coffee Break in Exhibition Area

7.8 Smart Energy and Self-Powered Devices

Exhibition Theatre 1430 - 1530

Organiser: Patrick Mayor, EPFL, CH

See Page 110

1600 Coffee Break in Exhibition Area

IP3 Interactive Presentations

IP sessions (in front of rooms 4A and 5A) 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. At the end of each afternoon Interactive Presentations session the award 'Best IP of the Day' is given.

IP3-1 **Leveraging Aging Effect to Improve SRAM-based True Random Number Generators**

Speaker: Mehdi Tahoori, Karlsruhe Institute of Technology (KIT), DE
Authors: Saman Kiamehr[1], Mohammad Saber Golanbari[2] and Mehdi Tahoori[2]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Karlsruhe Institute of Technology, DE

IP3-2 **Design Automation for Obfuscated Circuits with Multiple Viable Functions**

Speaker: Shahrzad Keshavarz, University of Massachusetts Amherst, US
Authors: Shahrzad Keshavarz[1], Christof Paar[2] and Daniel Holcomb[1]
[1]University of Massachusetts Amherst, US; [2]Horst Gortz Institut for IT-Security, Ruhr-Universitat Bochum, DE

IP3-3 **Double MAC: Doubling the Performance of Convolutional Neural Networks on Modern FPGAs**

Speaker: Jongeun Lee, UNIST, KR
Authors: Dong Nguyen[1], Daewoo Kim[1] and Jongeun Lee[2]
[1]UNIST, KR; [2]Ulsan National Institute of Science and Technology (UNIST), KR

IP3-4 **BITMAN: a Tool and API for FPGA Bitstream Manipulations**

Speaker: Dirk Koch, University of Manchester, GB
Authors: Khoa Pham, Edson Horta and Dirk Koch, University of Manchester, GB

IP3-5 **A Generic Topology Selection Method for Analog Circuits with Embedded Circuit Sizing Demonstrated on the OTA Example**
Speaker: Andreas Gerlach, Robert Bosch Centre for Power Electronics, DE
Authors: Andreas Gerlach[1], Thoralf Rosahl[2], Frank-Thomas Eitrich[2] and Jürgen Scheible[1]
[1]Robert Bosch Centre for Power Electronics, DE; [2]Robert Bosch GmbH, DE

IP3-6 **Latency Analysis of Homogeneous Synchronous Dataflow Graphs Using Timed Automata**
Speaker: Guus Kuiper, University of Twente, NL
Authors: Guus Kuiper[1] and Marco Bekooij[2]
[1]University of Twente, NL; [2]University of Twente + NXP semiconductors, NL

IP3-7 **COVERT: Counter OVErflow ReducTion for Efficient Encryption of Non-Volatile Memories**
Speaker: Kartik Mohanram, ECE Dept, University of Pittsburgh, US
Authors: Shivam Swami and Kartik Mohanram, University of Pittsburgh, US

IP3-8 **A Wear-Leveling-Aware Counter Mode for Data Encryption in Non-Volatile Memories**
Speaker: Fangting Huang, Huazhong University of Science and Technology, CN
Authors: Fangting Huang[1], Dan Feng[2], Yu Hua[2] and Wen Zhou[2]
[1]Huazhong University of Science and Technology, CN; [2]Wuhan National Lab for Optoelectronics, School of Computer Science and Technology, Huazhong University of Science and Technology, China, CN

IP3-9 **Tunnel FET Based Refresh-Free-DRAM**
Speaker: Navneet Gupta, ISEP-Paris, FR
Authors: Navneet Gupta[1], Adam Makosiej[2], Andrei Vladimirescu[3], Amara Amara[3] and Costin Anghel[3]
[1]Institut supérieur d'électronique de Paris, France; LETI, Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA-LETI) France;, FR; [2]LETI, Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA-LETI), FR; [3]Institut Superieur d'Electronique de Paris (ISEP), FR

IP3-10 **A Hardware Implementation of the MCAS Synchronization Primitive**
Speaker: Smruti Sarangi, IIT Delhi, IN
Authors: Srishty Patel, Rajshekar Kalayappan, Ishani Mahajan and Smruti R. Sarangi, IIT Delhi, IN

IP3-11 **BandiTS: Dynamic Timing Speculation Using Multi-Armed Bandit Based Optimization**
Speaker: Jeff Zhang, New York University, US
Authors: Jeff Zhang and Siddharth Garg, New York University, US

IP3-12 **Design and Implementation of a Fair Credit-Based Bandwidth Sharing Scheme for Buses**
Speaker: Carles Hernandez, Barcelona Supercomputing Center (BSC), ES
Authors: Mladen Slijepcevic[1], Carles Hernandez[2], Jaume Abella[3] and Francisco Cazorla[4]
[1]Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, ES; [2]Barcelona Supercomputing Center, ES; [3]Barcelona Supercomputing Center (BSC-CNS), ES; [4]Barcelona Supercomputing Center and IIIA-CSIC, ES

IP3-13 **Technology Mapping with All Spin Logic**
Speaker: Azadeh Davoodi, University of Wisconsin - Madison, US
Authors: Boyu Zhang[1] and Azadeh Davoodi[2]
[1]University of Wisconsin-Madison, US; [2]University of Wisconsin - Madison, US

IP3-14 **A new method to identify threshold logic functions**
Speaker: Spyros Tragoudas, Southern Illinois University Carbondale, US
Authors: Seyed Nima Mozaffari, Spyros Tragoudas and Themistoklis Haniotakis, Southern Illinois University, US

IP3-15 **A Bridging Fault Model for Line Coverage in the Presence of Undetected Transition Faults**
Speaker and Author: Irith Pomeranz, Purdue University, US

IP3-16 **CHRT: a Criticality- and Heterogeneity-Aware Runtime System for Task-Parallel Applications**
Speaker: Myeonggyun Han, UNIST, KR
Authors: Myeonggyun Han, Jinsu Park and Woongki Baek, UNIST, KR

IP3-17 **MobiXen: Porting Xen on Android Devices for Mobile Virtualization**
Speaker: Jianguo Yao, Shanghai Jiao Tong University, CN
Authors: Yaozu Dong[1], Jianguo Yao[2], Haibing Guan[2], Ananth. Krishna R[1] and Yunhong Jiang[1]
[1]Intel, US; [2]Shanghai Jiao Tong University, CN

IP3-18 **Optimisation Opportunities and Evaluation for GPGPU applications on Low-End Mobile GPUs**
Speaker: Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES
Authors: Matina Maria Trompouki[1] and Leonidas Kosmidis[2]
[1]Universitat Politècnica de Catalunya, ES; [2]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

1700 Session 8

8.1 IoT Day Hot Topic Session: Challenges and Potentials for IoT Rollout

5BC 1700 - 1830

Organisers: Marilyn Wolf, Georgia Tech, US
Andreas Herkersdorf, TU Muenchen, DE
Chair: Andreas Herkersdorf, TU Muenchen, DE
Co-Chair: Marilyn Wolf, Georgia Tech, US

Realizing the potential of IoT will require coordinated advances in multiple markets: applications, software systems, and VLSI. Understanding the requirements on IoT devices requires understanding the stack in which they operate. This session pulls together several points of view on the big picture of IoT rollout and their implications for device and system design

1700 **Ultra-Low Power and Dependability for IoT Devices**
Speaker: Joerg Henkel, KIT Karlsruhe, DE
Authors: Joerg Henkel[1], Santiago Pagani[2], Hussam Amrouch[3], Lars Bauer[3] and Farzad Samie[3]
[1]KIT, DE; [2]Karlsruhe Institute of Technology (KIT), DE; [3]Karlsruhe Institute of Technology, DE

1730 **Smarter Spaces through local(ized) object interactions**
Speaker: Jean-Marie Bonnin, Telecom Bretagne, FR
Authors: Jean-Marie Bonnin and Frédéric Weis, Telecom Bretagne, FR

1800 **Deploying IoT for Instrumentation and Analysis of Manufacturing Systems**
Speaker: Sujit Rokka Chhetri, University of California Irvine, US
Author: Mohammad Al Faruque, University of California Irvine, US

8.2 Hot Topic Session: No Power? No Problem! Exploiting Non-Volatility in Energy Constrained Environments

4BC 1700 - 1830

Organisers: Xiaobo Sharon Hu, University of Notre Dame, US
Michael Niemier, University of Notre Dame, US
Chair: Michael Niemier, University of Notre Dame, US
Co-Chair: Pierre-Emmanuel Gaillardon, The University of Utah at Salt Lake City, US

With the rapid growth of the internet of things (IoT), demands for battery-less systems are ever increasing. Systems that can be powered by ambient energy sources would offer new opportunities and capabilities for personal entertainment, self-powered, computational systems have obvious societal benefits when deployed for medical monitoring, environmental sensing, etc. This hot topic session considers the current landscape of energy harvesting computing systems and highlights the need for power neutral systems. Subsequent presentations showcase emerging non-volatile memory and logic technologies that could enable battery-less computing systems.

1700 **Energy-Driven Computing: Rethinking the Design of Energy Harvesting Systems**

Speaker: Geoff Merrett, University of Southampton, GB
Authors: Geoff Merrett and Bashir Al-Hashimi, University of Southampton, GB

1730 **Nonvolatile Processors: Why is it Trending?**

Speaker: Vijaykrishnan Narayanan, Penn State University, US
Authors: Fang Su[1], Kaisheng Ma[2], Xueqing Li[2], Tongda Wu[1], Yongpan Liu[1] and Vijaykrishnan Narayanan[2]
[1]Tsinghua University, CN; [2]Penn State University, US

1800 **Advanced Spintronic Memory and Logic For Non-Volatile Processors**

Speaker: X. Sharon Hu, University of Notre Dame, US
Authors: Robert Perricone[1], Ibrahim Ahmed[2], Zhaoxin Liang[3], Meghna Mankalale[4], X. Sharon Hu[1], Chris H. Kim[2], Michael Niemier[1], Sachin Sapatnekar[3] and Jian-Ping Wang[2]
[1]University of Notre Dame, US; [2]University of Minnesota, US; [3]University of Minnesota, ; [4]University Of Minnesota, US

8.3 Secure Processor Components

2BC 1700 - 1830

Chair: Patrick Schaumont, Virginia Tech, US
Co-Chair: Nele Mentens, KU Leuven, BE

Security concerns have put significant demands on hardware design of processors. In this session, papers will be presented that describe processor components designed to improve their performance, protect them more efficiently against side channel attacks and thereby improve the overall performance of processors used in secure applications.

1700 **Automatic Generation of Formally-Proven Tamper-Resistant Galois-Field Multipliers Based on Generalized Masking Scheme**

Speaker: Rei Ueno, Tohoku University, JP
Authors: Rei Ueno[1], Naofumi Homma[1], Sumio Morioka[2] and Takafumi Aoki[1]
[1]Tohoku University, JP; [2]Interstellar Technologies Inc., JP

1730 **SCAM: Secured Content Addressable Memory Based on Homomorphic Encryption**

Speaker: Song Bian, Kyoto University, JP
Authors: Song Bian, Masayuki Hiromoto and Takashi Sato, Kyoto University, JP

1800 **SPARX - A Side-Channel Protected Processor for ARX-based Cryptography**

Speaker: Florian Bache, University of Bremen, DE
Authors: Florian Bache[1], Tobias Schneider[2], Amir Moradi[2] and Tim Güneysu[3]
[1]University of Bremen, DE; [2]Ruhr University Bochum, DE; [3]University of Bremen & DFKI, DE

8.4 Advanced systems for healthcare and assistive technologies

3A 1700 - 1830

Chair: Ruben Braojos, EPFL, CH
Co-Chair: Luca Fanucci, University of Pisa, IT

This session focuses on embedded systems for human activity recognition and control. These systems combine flexible and dynamic hardware architectures with advanced novel signal processing techniques for activity recognition, myoelectric prosthesis control, motor intention decoding and brain computer interface. Finally, we will have two interactive presentations focused on embedded systems for diagnosis.

1700 **Adaptive Compressed Sensing at the Fingertip of Internet-of-Things Sensors: An Ultra-Low Power Activity Recognition**

Speaker: Hassan Ghasemzadeh, Washington State University, US
Authors: Ramin Fallahzadeh[1], Josué Pagán[2] and Hassan Ghasemzadeh[3]
[1]School of Electrical Engineering and Computer Science, Washington State University, US; [2]Complutense University of Madrid, ES; [3]Washington State University, US

1730 **A Zynq-based dynamically reconfigurable high density myoelectric prosthesis controller**

Speaker: Linus Witschen, Paderborn University, DE
Authors: Alexander Boschmann[1], Georg Thombansen[1], Linus Witschen[1], Alex Wiens[1] and Marco Platzner[2]
[1]Paderborn University, DE; [2]University of Paderborn, DE

1800 **Microwatt End-to-End Digital Neural Signal Processing Systems for Motor Intention Decoding**

Speaker: Zhewei Jiang, Columbia University, US
Authors: Zhewei Jiang[1], Chisung Bae[2], Joonseong Kang[2], Sang Joon Kim[2] and Mingoo Seok[1]
[1]Columbia University, US; [2]Samsung Electronics, KR

1815 **An Embedded System Remotely Driving Mechanical Devices by P300 Brain Activity**

Speaker: Daniela De Venuto, Politecnico di Bari, IT
Authors: Valerio F. Annese[1], Giovanni Mezzina[2] and Daniela De Venuto[2]
[1]Politecnico di Bari, IT; [2]Dept. of Electrical and Information Engineering, Politecnico di Bari, IT

IPs **IP4-1**

8.5 Learning and Resilience Techniques for Green Computing

3C 1700 - 1830

Chair: Muhammed Shafique, Vienna University of Technology (TU-Wien), AT
Co-Chair: Andreas Burg, EPFL, CH

The papers in this session discuss the use of learning as well as energy efficient circuit level implementation techniques for Neural Networks and for Green Computing in general.

1700 **Revamping Timing Error Resilience to Tackle Choke Points at NTC Systems**

Speaker: Aatreyi Bal, USU Bridge Lab, Utah State University, US
Authors: Aatreyi Bal, Shamik Saha, Sanghamitra Roy and Koushik Chakraborty Utah State University, US

1730 **Efficient Neural Network Acceleration on GPGPU using Content Addressable Memory**

Speaker: Tajana Rosing, University of California at San Diego, US
Authors: Mohsen Imani[1], Daniel Peroni[1], Yeseong Kim[1], Abbas Rahimi[2] and Tajana Rosing[3]
[1]University of California San Diego, US; [2]University of California Berkeley, US; [3]UCSD, US

1800 **Chain-NN: An Energy-Efficient 1D Chain Architecture for Accelerating Deep Convolutional Neural Networks**

Speaker: Shihao Wang, Waseda University, JP
Authors: Shihao Wang, Dajiang Zhou, Xushen Han and Yoshimura Takeshi, Waseda University, JP

1815 **Continuous Learning of HPC Infrastructure Models using Big Data Analytics and In-Memory processing Tools**

Speaker: Andrea Bartolini, ETH Zurich/University of Bologna, IT
Authors: Francesco Beneventi[1], Andrea Bartolini[2], Carlo Cavazzoni[3] and Luca Benini[4]
[1]DEI - University of Bologna, IT; [2]University of Bologna, IT; [3]Cineca, IT; [4]Università di Bologna, IT

IPs **IP4-2, IP4-3**

8.6 Hot Topic Session: Self-aware Systems: Concepts and Applications

5A 1700 - 1830

Organisers: Nikil Dutt, UC Irvine, US
Axel Jantsch, TU Wien, AT
Chair: Nikil Dutt, UC Irvine, US
Co-Chair: Amir Rahmani, TU Wien, AT

This special hot topic session addresses concepts and applications of self-awareness for engineered systems. Interest in self-awareness continues to grow with applications in diverse domains such as automotive, space, military, consumer electronics, industrial control, health care, etc. The first talk outlines the concepts of self-awareness in psychology, and its applicability in computing, as well as in the engineering of adaptive systems. The second talk reviews the role of self-awareness in autonomous driving systems and explains how system self-awareness has become an important foundation for reliable and flexible platform management of autonomous cars. The third talk presents a remote health monitoring and diagnostic system for holistic perception of a patient's situation, and demonstrates how self-awareness is leveraged through the use of wearable sensors, contextual knowledge of the patient's health situation, and automated reasoning of the patient's health situation.

1700 **Self-aware Computing Systems: From Psychology to Engineering**

Speaker and Author: Peter Lewis, Aston University, GB

1730 **Self-awareness in autonomous systems: Self-driving cars**

Speaker: Rolf Ernst, TU Braunschweig, DE
Authors: Johannes Schlatow[1], Mischa Möstl[2], Rolf Ernst[2], Marcus Nolte[2], Inga Jatzkowski[2], Markus Maurer[2], Christian Herber[3] and Andreas Herkersdorf[3]
[1]TU Braunschweig, Institute of Computer and Network Engineering, DE; [2]TU Braunschweig, DE; [3]Technische Universität München, DE

1800 **Self-awareness in Remote Health Monitoring Systems through Wearable Electronics**

Speaker: Axel Jantsch, TU Wien, AT
Authors: Arman Anzanour[1], Iman Azimi[1], Maximilian Götzinger[1], Amir M. Rahmani[2], Nima Taherinejad[3], Pasi Liljeberg[1], Axel Jantsch[3] and Nikil Dutt[4]
[1]University of Turku, FI; [2]University of California Irvine & TU Wien, US; [3]Vienna University of Technology, AT; [4]UC Irvine, US

8.7 Instruction-level and thread-level parallelism in embedded systems

3B 1700 - 1830

Chair: Oliver Bringmann, Universität Tübingen, DE
Co-Chair: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

The first paper in this session presents a novel open-source hardware/software infrastructure for dynamic binary translation. The second paper presents a mechanism to improve the floating point to fixed point conversion by exploiting word-level parallelism. The third paper presents a WCET analysis for multiple tasks on single-core systems.

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1700 **Hardware-Accelerated Dynamic Binary Translation**

Speaker: Simon Rokicki, Université de Rennes [1] / IRISA, FR
Authors: Simon Rokicki[1], Erven Rohou[2] and Steven Derrien[1]
[1]Irisa, FR; [2]Inria, FR

1730 **Superword Level Parallelism aware Word Length Optimization**

Speaker: Ali Hassan El Moussawi, INRIA, FR
Authors: Ali Hassan EL Moussawi[1] and Steven Derrien[2]
[1]INRIA, FR; [2]sderrien, FR

1800 **Schedulability-Aware SPM Allocation for Preemptive Hard Real-Time Systems with Arbitrary Activation Patterns**

Speaker: Arno Luppold, Hamburg University of Technology, DE
Authors: Arno Luppold[1] and Heiko Falk[2]
[1]Hamburg University of Technology, DE; [2]Hamburg University of Technology (TUHH), DE

IPs **IP4-4, IP4-5, IP4-6**

8.8 Panel: Technology startups. Vision from Academia and Industry

Exhibition Theatre 1700 - 1830

Organiser: Marisa Lopez-Vallejo, UPM, ES
Moderator: Marisa Lopez-Vallejo, UPM, ES

See Page 110

PARTY DATE Party | Networking Event

The Olympic Museum 1900 - 2300

See Page 13

9.1 Wearable and Smart Medical Devices Day: New tools and devices for chronic and acute care

5BC 0830 - 1000

Organisers: José L. Ayala, Universidad Complutense de Madrid, ES
Chris Van Hoof, IMEC, BE
Chair: Jose L. Ayala, Complutense University of Madrid, ES
Co-Chair: Nick Van Helleputte, imec, BE

This session will present the recent advances in medical devices for the clinical practice. We will attend how Industry and Academia work on designing novel wearable, ASICs and computational systems that help on promoting the novel healthcare paradigms in the treatment of chronic and acute diseases.

0830 **Wearable Robotics in clinical practice: prospects**
Speaker and Author: José Luis Pons, CSIC, ES

0900 **Overcoming hearing loss through new implant technologies**
Speaker and Author: Carl Van Himbeeck, Cochlear Technology Centre, BE

0930 **Circuits and systems as enablers for novel healthcare paradigms**
Speaker and Author: Mario Konijnenburg, imec, BE

1000 Coffee Break in Exhibition Area

9.2 Emerging Schemes for Memory Management

4BC 0830 - 1000

Chair: Arne Heittman, RWTH, DE
Co-Chair: Costin Anghel, ISEP, FR

This topic covers aspects of emerging memory architectures and functional blocks with respect to performance and endurance enhancement. In particular caches, FTL, logic-in-memory and error correction schemes covering strategies like error correction wear leveling and cache replacement are covered. NVMs like PCM, Flash and RRAms are considered in this track.

0830 **A Log-aware Synergized Scheme for Page-level FTL Design**
Speaker: Chu Li, Huazhong University of Science & Technology, CN
Authors: Chu Li[1], Dan Feng[1], Yu Hua[1], Fang Wang[1], Chuntao Jiang[2] and Wei Zhou[1]
[1]Huazhong University of Science and Technology, CN; [2]Illinois Institute of Technology, US

0900 **MALRU: Miss-penalty Aware LRU-based Cache Replacement for Hybrid Memory Systems**
Speaker: Chen Di, Huazhong University of Science and Technology, CN
Authors: Di Chen, Hai Jin, Xiaofei Liao, Haikun Liu, Rentong Guo and Dong Liu, Huazhong University of Science and Technology, CN

0930 **Endurance Management for Resistive Logic-In-Memory Computing Architectures**
Speaker: Saeideh Shirinzadeh, University of Bremen, DE
Authors: Saeideh Shirinzadeh[1], Mathias Soeken[2], Pierre-Emmanuel Gaillardon[3], Giovanni De Micheli[4] and Rolf Drechsler[5]
[1]Group of Computer Architecture, University of Bremen, DE; [2]EPFL, CH; [3]University of Utah, US; [4]Integrated Systems Laboratory, EPFL, Lausanne, Switzerland, CH; [5]Group of Computer Architecture, University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, DE

0945 **Live Together or Die Alone: Block Cooperation to Extend Lifetime of Resistive Memories**
Speaker: David Kaeli, Northeastern University, US
Authors: Mohammad Khavari Tavana, Amir Kavyan Ziabari and David Kaeli, Northeastern University, US

IPs **IP4-7, IP4-8, IP4-9**

1000 Coffee Break in Exhibition Area

9.3 Hot Topic Session: Security in Cyber-Physical Systems: Attacks All The Way

2BC 0830 - 1000

Organisers: Anupam Chattopadhyay, Nanyang Technological University, SG
Muhammad Shafique, CARE-Tech, TU Wien, AT
Chair: Ahmad Sadeghi, TU Darmstadt, DE
Co-Chair: Muhammad Shafique, CARE-Tech, TU Wien, AT

The goal of this special session is to revisit the depth and breadth of CPS security, with focus on practical system and design automation aspects. In a practical system, the possible sources of security vulnerabilities and recent attacks are discussed, and it is argued that there are significant varieties of attacks that need to be accounted for in a holistic manner.

0830 **Secure Cyber-Physical Systems: Current Trends, Tools and Open Research Problems**

Speaker: Anupam Chattopadhyay, Nanyang Technological University, SG
Authors: Anupam Chattopadhyay[1], Alok Prakash[1] and Muhammad Shafique[2]
[1]Nanyang Technological University, SG; [2]Vienna University of Technology (TU Wien), AT

0845 **Don't Fall into a Trap: Physical Side-Channel Analysis of ChaCha20-Poly1305**

Speaker: Bernhard Jungk, Temasek Laboratories @ Nanyang Technological University, SG
Authors: Bernhard Jungk[1] and Shivam Bhasin[2]
[1]Temasek Laboratories @ Nanyang Technological University, SG; [2]TL@NTU, SG

0900 **The RowHammer Problem and Other Issues We May Face as Memory Becomes Denser**

Onur Mutlu, ETH Zurich, CH

0915 **Compromising FPGA SoCs using Malicious Hardware Blocks**

Speaker: Nisha Jacob, Fraunhofer AISEC, DE
Authors: Nisha Jacob[1], Carsten Rolfes[1], Andreas Zankl[1], Johann Heyszl[1] and Georg Sigl[2]
[1]Fraunhofer Institute for Applied and Integrated Security (AISEC), DE; [2]Technische Universität München, DE

0930 **Inspiring Trust in Outsourced Integrated Circuit Fabrication**

Speaker and Author: Siddharth Garg, New York University, US

0945 **Analyzing Security Breaches of Countermeasures Throughout the Refinement Process in Hardware Design Flow**

Speaker: Jean-Luc Danger, Secure-IC, FR
Authors: Sylvain Guilley, Jean-Luc Danger, Philippe Nguyen, Robert Nguyen and Youssef Souissi, Secure-IC S.A.S., FR

1000 Coffee Break in Exhibition Area

9.4 Design Space Exploration

3A 0830 - 1000

Chair: Lars Bauer, KIT Karlsruhe, DE
Co-Chair: Alberto Del Barrio, Universidad Computense de Madrid, ES

This session features methods that extract desired implementation options from the huge design space of digital systems. The first talk presents a method to pick valuable operating points from a Pareto optimal set of task mappings for an efficient online resource management. The second presentation presents a rapid estimation framework to evaluate performance/area metrics of various accelerator options for an application at an early design phase. A design space exploration for implementing convolutional layers of neural networks is presented in the third talk in order to maximize the performance. The fourth talk presents an HLS scheduling method that is optimized for incorpo-

rating Radix 8 Booth multipliers. The session concludes with two short introductions of interactive presentations.

0830 **Automatic Operating Point Distillation for Hybrid Mapping Methodologies**

Speaker: Behnaz Pourmohseni, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE
Authors: Behnaz Pourmohseni[1], Michael Glaß[2] and Jürgen Teich[3]
[1]Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE; [2]Ulm University, DE; [3]University of Erlangen-Nuremberg, DE

0900 **Design Space Exploration of FPGA-based Accelerators with Multi-level Parallelism**

Speaker: Guanwen Zhong, National University of Singapore, SG
Authors: Guanwen Zhong[1], Alok Prakash[2], Siqi Wang[1], Yun (Eric) Liang[3], Tulika Mitra[1] and Smail Niar[4]
[1]National University of Singapore, SG; [2]Nanyang Technological University, SG; [3]Peking University, CN; [4]LAMIH-University of Valenciennes, FR

0930 **Design Space Exploration of FPGA Accelerators for Convolutional Neural Networks**

Speaker: Jongeun Lee, UNIST, KR
Authors: Atul Rahman[1], Sangyun Oh[2], Jongeun Lee[3] and Kiyoung Choi[4]
[1]Samsung Electronics, KR; [2]UNIST, KR; [3]Ulsan National Institute of Science and Technology (UNIST), KR; [4]Seoul National University, KR

0945 **A Slack-based Approach to Efficiently Deploy Radix 8 Booth Multipliers**

Speaker: Alberto Antonio Del Barrio, Universidad Complutense de Madrid, ES
Authors: Alberto Antonio Del Barrio Garcia and Hermida Roman, Complutense University of Madrid, ES

IPs **IP4-10**

1000 Coffee Break in Exhibition Area

9.5 Modeling and optimization of Internet-of-things (IoT) devices

3C 0830 - 1000

Chair: William Fornaciari, Politecnico di Milano, IT
Co-Chair: Shusuke Yoshimoto, Osaka University, JP

Modeling and optimization of Internet-of-things (IoT) devices from energy sources to computing components including battery, energy harvesting system, power converter, and microprocessor

0830 **Measurement and Validation of Energy Harvesting IoT Devices**

Speaker: Lukas Sigrist, ETH Zurich, CH
Authors: Lukas Sigrist[1], Andres Gomez[1], Roman Lim[1], Stefan Lippuner[1], Matthias Leubin[1] and Lothar Thiele[2]
[1]ETH Zurich, CH; [2]Swiss Federal Institute of Technology Zurich, CH

0900 **A Methodology for the Design of Dynamic Accuracy Operators by Runtime Back Bias**

Speaker: Daniele Jahier Pagliari, Politecnico di Torino, IT
Authors: Daniele Jahier Pagliari[1], Yves Durand[2], David Coriat[2], Anca Molnos[2], Edith Beigne[2], Enrico Macii[1] and Massimo Poncino[1]
[1]Politecnico di Torino, IT; [2]CEA-LETI, FR

0930 **A Scan-Chain Based State Retention Methodology for IoT Processors Operating on Intermittent Energy**

Speaker: Pascal Alexander Hager, ETH Zürich, CH
Authors: Pascal Alexander Hager[1], Hamed Fatemi[2], Jose Pineda[2] and Luca Benini[3]
[1]ETH Zurich, CH; [2]NXP Semiconductors, NL; [3]Università di Bologna, IT

0945 **A Circuit-Equivalent Battery Model Accounting for the Dependency on Load Frequency**

Speaker: Enrico Macii, Politecnico di Torino, IT
Authors: Yukai Chen, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT

IPs **IP4-11, IP4-12**

1000 Coffee Break in Exhibition Area

9.6 Reliability and Optimization Techniques for Analog Circuits

5A 0830 - 1000

Chair: Manuel Barragan, TIMA, FR
Co-Chair: Said Hamdioui, TU Delft, NL

The first two papers discuss optimizations for yield and performances of analog circuits. The third paper proposes methods for flip-flop soft error protection in sequential circuits wile the last paper discusses methods based on machine learning for timing error detection.

0830 **SLoT: A Supervised Learning Model to Predict Dynamic Timing Errors of Functional Units**

Speaker: Xun Jiao, University of California San Diego, US
Authors: Xun Jiao[1], Yu Jiang[2], Abbas Rahimi[3] and Rajesh Gupta[1]
[1]University of California, San Diego, US; [2]Tsinghua University, CN; [3]University of California, Berkeley, US

0900 **Exploiting Data-Dependence and Flip-Flop Asymmetry for Zero-Overhead System Soft Error Mitigation**

Speaker: Liangzhen Lai, ARM Inc., US
Authors: Liangzhen Lai and Vikas Chandra, ARM, US

0915 **Subgradient Based Multiple-Starting-Point Algorithm for Non-Smooth Optimization of Analog Circuits**

Speaker: Wenlong Lv, Fudan University, CN
Authors: Wenlong Lv[1], Fan Yang[1], Changhao Yan[1], Dian Zhou[2] and Xuan Zeng[1]
[1]Fudan University, CN; [2]University of Texas at Dallas, US

0930 **Efficient Yield Optimization Method using a Variable K-Means Algorithm for Analog IC Sizing**

Speaker: António Canelas, Instituto de Telecomunicações/Instituto Superior Técnico – ULisbon, PT
Authors: António Canelas[1], Ricardo Martins[1], Ricardo Povoa[2], Nuno Lourenço[1] and Nuno Horta[1]
[1]Instituto de Telecomunicações/Instituto Superior Técnico – ULisbon, PT; [2]Instituto de Telecomunicações/Instituto Superior Técnico - ULisbon, PT

IPs **IP4-13, IP4-14, IP4-15, IP4-16**

1000 Coffee Break in Exhibition Area

9.7 Front-row seats for Temperature and Variability

3B 0830 - 1000

Chair: Marina Zapater Sancho, EPFL, CH
Co-Chair: Giovanni Ansaloni, USI, CH

This session sets highlights on the impact of temperature and variability sources at the overall system level. Firstly, an approach that incorporates leakage in thermal simulations is presented and a thermal simulation framework is devised. After that, temperature is not only estimated but also minimized in the context of global interconnects by means of an analytic methodology. Finally, timing variability plays its role in the session and its effects in variable-latency designs.

0830 **An Efficient Leakage-Aware Thermal Simulation Approach for 3D-ICs Using Corrected Linearized Model and Algebraic Multigrid**

Speaker: Chao Yan, Microelectronics Dept., Fudan University, CN
Authors: Chao Yan[1], Hengliang Zhu[1], Dian Zhou[2] and Xuan Zeng[1]
[1]Fudan University, CN; [2]University of Texas at Dallas, US

0900 **A Thermally-Aware Energy Minimization Methodology for Global Interconnects**

Speaker: Massoud Pedram, University of Southern California, US
Authors: Soheil Nazar Shahsavani[1], Alireza Shafaei Bejestan[1], Shahin Nazarian[1] and Massoud Pedram[2]
[1]University of Southern California, US; [2]USC, US

0930 **Analysis and Optimization of Variable-Latency Designs in the Presence of Timing Variability**

Speaker: Kai-Chiang Wu, Department of Computer Science, National Chiao Tung University, Hsinchu, Taiwan, TW
Authors: Chang-Lin Tsai, Chao-Wei Cheng, Ning-Chi Huang and Kai-Chiang Wu, National Chiao Tung University, TW

IPs **IP4-17, IP4-18**

1000 Coffee Break in Exhibition Area

9.8 The Internet of INSECURE Things

Exhibition Theatre 0830 - 1000

Organiser: Marcello Coppola, STMicroelectronics, FR

See Page 111

1000 Coffee Break in Exhibition Area

IP4 Interactive Presentations

IP sessions (in front of rooms 4A and 5A) 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. At the end of each afternoon Interactive Presentations session the award 'Best IP of the Day' is given.

IP4-1 **1024-Channel 3D Ultrasound Digital Beamformer in a Single 5W FPGA**

Speaker: Aya Ibrahim, EPFL, CH
Authors: Federico Angiolini[1], Aya Ibrahim[1], William Simon[1], Ahmet Caner Yüzügüler[1], Marcel Arditi[1], Jean-Philippe Thiran[1] and Giovanni De Micheli[2]
[1]EPFL, CH; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

IP4-2 **LAANT: A Library to Automatically Optimize EDP for OpenMP Applications**

Speaker: Arthur Francisco Lorenzon, Federal University of Rio Grande do Sul, BR
Authors: Arthur Lorenzon, Jeckson Dellagostin Souza and Antonio Carlos Schneider Beck Filho, Universidade Federal do Rio Grande do Sul, BR

IP4-3 **Improving the Accuracy of the Leakage Power Estimation of Embedded CPUs**

Speaker: Shiao-Li Tsao, National Chiao Tung University, TW
Authors: Ting-Wu Chin, Shiao-Li Tsao, Kuo-Wei Hung and Pei-Shu Huang, National Chiao Tung University, TW

IP4-4 **Schedule-Aware Loop Parallelization for Embedded MPSoCs by Exploiting Parallel Slack**

Speaker: Miguel Angel Aguilar, RWTH Aachen University, DE
Authors: Miguel Angel Aguilar[1], Rainer Leupers[1], Gerd Ascheid[1], Nikolaos Kavvadias[2] and Liam Fitzpatrick[2]
[1]RWTH Aachen University, DE; [2]Silexica Software Solutions GmbH, DE

IP4-5 **Reducing Code Management Overhead in Software-Managed Multicores**
Speaker: Aviral Shrivastava, Arizona State University, US
Authors: Jian Cai[1], Yooseong Kim[1], Youngbin Kim[2], Aviral Shrivastava[1] and Kyoungwoo Lee[2]
[1]Arizona State University, US; [2]Yonsei University, KR

IP4-6 **Performance Evaluation and Optimization of HBM-Enabled GPU for Data-intensive Applications**
Speaker: Yuan Xie, University of California, Santa Barbara, US
Authors: Maohua Zhu[1], Youwei Zhuo[2], Chao Wang[3], Wenguang Chen[4] and Yuan Xie[1]
[1]University of California, Santa Barbara, US; [2]University of Southern California, US; [3]University of Science and Technology of China, CN; [4]Tsinghua University, CN

IP4-7 **DAC: Dedup-Assisted Compression Scheme for Improving Lifetime of NAND storage systems**
Speaker: Jisung Park, Seoul National University, KR
Authors: Jisung Park[1], Sungjin Lee[2] and Jihong Kim[1]
[1]Seoul National University, KR; [2]Inha University, KR

IP4-8 **Lifetime Adaptive ECC in NAND Flash Page Management**
Speaker: Shunzhuo Wang, Huazhong University of Science and Technology, CN
Authors: Shunzhuo Wang[1], Fei Wu[1], Zhonghai Lu[2], You Zhou[1], Qin Xiong[1], Meng Zhang[1] and Changsheng Xie[1]
[1]Huazhong University of Science and Technology, CN; [2]KTH Royal Institute of Technology, SE

IP4-9 **3D-DPE: A 3D High-Bandwidth Dot-Product Engine for High-Performance Neuromorphic Computing**
Speaker: Miguel Lastras-Montaño, University of California, Santa Barbara, US
Authors: Miguel Angel Lastras-Montaño[1], Bhaswar Chakrabarti[1], Dmitri B. Strukov[1] and Kwang-Ting Cheng[2]
[1]UCSB, US; [2]HKUST, HK

IP4-10 **A Schedulability Test for Software Migration on Multicore Systems**
Speaker: Jung-Eun Kim, Department of Computer Science at the University of Illinois at Urbana-Champaign, US
Authors: Jung-Eun Kim[1], Richard Bradford[2], Tarek Abdelzaher[3] and Lui Sha[3]
[1]Department of Computer Science, University of Illinois at Urbana-Champaign, US; [2]Rockwell Collins, Cedar Rapids, IA, US; [3]University of Illinois, US

IP4-11 **Adaptive Power Delivery System Management for Many-Core Processors with On/Off-Chip Voltage Regulators**
Speaker: Haoran Li, The Hong Kong University of Science and Technology, HK
Authors: Haoran Li, Jiang Xu, Zhe Wang, Peng Yang, Rafael Kioji Vivas Maeda and Zhongyuan Tian, The Hong Kong University of Science and Technology, HK

IP4-12 **Flying and Decoupling Capacitance Optimization for Area-Constrained On-Chip Switched-Capacitor Voltage Regulators**
Speaker: Xiaoyang Mi, Arizona State University, US
Authors: Xiaoyang Mi[1], Hesam Fathi Moghadam[2] and Jae-sun Seo[1]
[1]Arizona State University, US; [2]Oracle Corporation, US

IP4-13 **Enhancing Analog Yield Optimization for Variation-aware Circuits Sizing**
Speaker: Ons Lahiouel, Concordia University, CA
Authors: Ons Lahiouel, Mohamed H. Zaki and Sofiene Tahar, Concordia University, CA

IP4-14 **A New Sampling Technique for Monte Carlo-based Statistical Circuit Analysis**
Speaker: Hiwa Mahmoudi, Vienna University of Technology, AT
Authors: Hiwa Mahmoudi and Horst Zimmermann, Vienna University of Technology, AT

IP4-15 **Automatic Technology Migration of Analog IC Designs using Generic Cell Libraries**
Speaker: Nuno Horta, Instituto de Telecomunicações / Instituto Superior Técnico, PT
Authors: Jose Cachaco[1], Nuno Machado[1], Nuno Lourenco[1], Jorge Guilherme[2] and Nuno Horta[3]
[1]Instituto de Telecomunicacoes/Instituto Superior Tecnico, PT; [2]Instituto de Telecomunicacoes/Instituto Politecnico de Tomar, PT; [3]Instituto de Telecomunicações/Instituto Superior Técnico, PT

IP4-16 **Noise-Sensitive Feedback Loop Identification in Linear Time-Varying Analog Circuits**
Speaker: Peng Li, Texas A&M University, US
Authors: Ang Li[1], Peng Li[1], Tingwen Huang[2] and Edgar Sánchez-Sinencio[1]
[1]Texas A&M University, US; [2]Texas A&M University at Qatar, QA

IP4-17 **CAnDy-TM: Comparative Analysis of Dynamic Thermal Management in Many-Cores using Model Checking**
Speaker: Muhammad Shafique, Institute of Computer Engineering, Vienna University of Technology (TU Wien), AT
Authors: Syed Ali Asadullah Bukhari[1], Faiq Khalid Lodhi[2], Osman Hasan[2], Muhammad Shafique[3] and Joerg Henkel[4]
[1]National University of Sciences and Technology - School of Electrical Engineering and Computer Science, PK; [2]School of Electrical Engineering and Computer Science National University of Sciences and Technology (NUST), PK; [3]Vienna University of Technology (TU Wien), AT; [4]KIT, DE

IP4-18 **Power pre-characterized meshing algorithm for finite element thermal analysis of integrated circuits**
Speaker: Shohdy Abdelkader, Software Developer, EG
Authors: Shohdy Abdelkader[1], Alaa ElRouby[2] and Mohamed Dessouky[1]
[1]Mentor Graphics, EG; [2]Electric and Electronic Department, Faculty of Engineering and Natural Science, Yildirim Beyazit University, TR

1100 Session 10

10.1 Wearable and Smart Medical Devices Day: Diagnosis and prevention systems

5BC 1100 - 1230

Organisers: José L. Ayala, Universidad Complutense de Madrid, ES
Chris Van Hoof, IMEC, BE
Chair: Olivier Romain, Université de Cergy-Pontoise, FR
Co-Chair: Nick Van Helleputte, imec, BE

This session will present novel approaches, techniques and devices for the improvement of diagnosis and prevention systems. Improved bioanalytics-on-chip designs, wearables in the prevention of elderly, computational mechanisms for prevention of symptoms, and bioelectronics medicines will be covered.

1100 **Enabling technologies for next generation bioanalytics on chip**
Speaker and Author: Carlota Guiducci, EPFL, CH

1120 **Bioelectronics Medicines - Bridging Biology with Technology**
Speaker and Author: Firat Yazicioglu, GSK, BE

1145 **An Optimal Approach for Low-Power Migraine Prediction Models in the State-of-the-Art Wireless Monitoring Devices**
Speaker: Josué Pagán, Universidad Complutense de Madrid, ES
Authors: Josué Pagán[1], Ramin Fallahzadeh[2], Hassan Ghasemzadeh[3], Jose Manuel Moya[4], José Luis Risco Martín[1] and Jose L. Ayala[1]
[1]Complutense University of Madrid, ES; [2]School of Electrical Engineering and Computer Science, Washington State University, US; [3]Washington State University, US; [4]Universidad Politécnica de Madrid, ES

1205 **Wearable electronics – what is it good for – and what is missing to support the quality of life of elderly people?**
Speaker and Author: Ralf Brederlow, Kilby Labs at Texas Instruments, DE

1230 Lunch Break in Garden Foyer

10.2 Hot Topic Session: EDA as an Emerging Technology Enabler

4BC 1100 - 1230

Organisers: Pierre-Emmanuel Gaillardon,, The University of Utah at Salt Lake City, US
Mathias Soeken, EPFL, CH
Chair: Mathias Soeken, EPFL, CH
Co-Chair: Ian O'Connor, Ecole Centrale de Lyon, FR

In this hot topic session, we demonstrate how design automation enables emerging technologies. Four talks will be provided. The first talk will review how logic synthesis has and is still enabling today's technologies and will also outline the requirements of design automation for the technologies of tomorrow. The other three talks present several emerging technologies, such as carbon nanotubes, spin wave devices, quantum-dot cellular automata, nanomagnetic logic and quantum computing, and illustrate how design automation plays a central role in their development.

1100 **Logic Optimization and Synthesis: Trends and Directions in Industry**

Speaker: Luca Amaru, Synopsys Inc., US
Authors: Luca Amaru, Patrick Vuillod, Jiong Luo and Janet Olson, Synopsys, US

1122 **Carbon Nanotubes Enable Major Energy Efficiency Benefits for Sub-10nm Digital Systems**

Speaker: Gage Hills, Stanford University, US
Authors: Gage Hills[1], Max Shulaker[2], Chi-Shuen Lee[3], Peter Debacker[4], Marie Garcia Bardon[5], Dmitry Yakimets[5], Romain Ritzenthaler[5], Iuliana Radu[5], Francky Catthoor[5], Praveen Raghavan[6], Aaron Thean[7], H.-S. Philip Wong[3] and Subhasish Mitra[3]
[1]Department of Electrical Engineering, Stanford University, US; [2]MIT, US; [3]Stanford University, US; [4]imec vzw, BE; [5]IMEC, BE; [6]imec, BE; [7]NU Singapore, SG

1145 **Wave Pipelining for Majority-based Beyond-CMOS Technologies**

Speaker: Odysseas Zografos, imec, BE
Authors: Odysseas Zografos[1], Anton De Meester[1], Eleonora Testa[2], Mathias Soeken[2], Pierre-Emmanuel Gaillardon[3], Giovanni De Micheli[4], Luca Amaru[5], Praveen Raghavan[6], Francky Catthoor[1] and Rudy Lauwereins[1]
[1]IMEC, BE; [2]EPFL, CH; [3]University of Utah, US; [4]École Polytechnique Fédérale de Lausanne (EPFL), CH; [5]Synopsys, US; [6]imec, BE

1207 **Design Automation for Quantum Architectures**

Speaker: Martin Roetteler, Microsoft Research, US
Authors: Martin Roetteler, Krysta M. Svore, Dave Wecker and Nathan Wiebe, Microsoft, US

1230 Lunch Break in Garden Foyer

10.3 Side-Channel Attacks

2BC 1100 - 1230

Chair: Oscar Reparaz, KU Leuven, BE
Co-Chair: Wieland Fischer, Infineon, DE

This session introduces new side-channel attacks techniques against cryptographic primitives, namely leakage resilient protocols and storage encryption based on AES. Also a power measurement setup specifically targeting static power consumption is presented and evaluated from the side-channel attack viewpoint.

1100 **Side-Channel Plaintext-Recovery Attacks on Leakage-Resilient Encryption**

Speaker: Thomas Unterluggauer, Graz University of Technology, AT
Authors: Thomas Unterluggauer, Mario Werner and Stefan Mangard, Graz University of Technology, AT

1130 **Static Power Side-Channel Analysis of a Threshold Implementation Prototype Chip**

Speaker: Thorben Moos, Horst Görtz Institute for IT-Security, Ruhr-Universität Bochum, DE
Authors: Thorben Moos[1], Amir Moradi[2] and Bastian Richter[1]
[1]Ruhr-Universität Bochum, DE; [2]Ruhr University Bochum, DE

1200 **Side-Channel Power Analysis of XTS-AES**

Speaker: Chao Luo, Northeastern Univeristy, CN
Authors: Chao Luo, Yunsi Fei and A. Adam Ding, Northeastern University, US

IPs **IP5-1**

1230 Lunch Break in Garden Foyer

10.4 Emerging Architectures for Reconfigurable Computing

3A 1100 - 1230

Chair: Alessandro Cilardo, University of Naples Federico II, IT
Co-Chair: Florent de Dinechin, ENS-Lyon, FR

This session presents a view of future reconfigurable architectures. These include a field programmable transistor array, a programmable methodology for power gating FPGA routing network, and a dynamic instruction issue technique for coarse grain reconfigurable architectures.

1100 **A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration**

Speaker: Carl Sechen, The University of Texas at Dallas, US
Authors: Jingxiang Tian, Gaurav Rajavendra Reddy, Jiajia Wang, William Swartz Jr., Yiorgos Makris and Carl Sechen, The University of Texas at Dallas, US

1130 **A Power Gating Switch Box Architecture in Routing Network of SRAM-Based FPGAs in Dark Silicon Era**

Speaker: Hossein Asadi, Sharif University of Technology, IR
Authors: Zeinab Seifoori, Behnam Khaleghi and Hossein Asadi, Sharif University of Technology, IR

1200 **A static-placement, dynamic-issue framework for CGRA loop accelerator**

Speaker: Zhongyuan Zhao, Department of NaNo/Micro Electronics, CN
Authors: Zhongyuan Zhao[1], Weiguang Sheng[1], Weifeng He[1], Zhigang Mao[1] and Zhaoshi Li[2]
[1]Shanghai JiaoTong University, CN; [2]Tsinghua University, Beijing, CN

1230 Lunch Break in Garden Foyer

10.5 Emerging NoC Directions

3C 1100 - 1230

Chair: Jiang Xu, Hong Kong University of Science and Technology, HK
Co-Chair: Tushar Krishna, GeorgiaTech, US

This session presents papers on emerging directions in NoC design. The first paper uses machine learning for effective power management in NoCs. The next three papers use emerging technologies - wireless, 3D, and Optical - for efficient on-chip communications.

1100 **Machine Learning Enabled Power-Aware Network-on-Chip Design**

Speaker: Avinash Kodi, Ohio University, US
Authors: Dominic DiTomaso[1], Ashif Sikder[1], Avinash Kodi[1] and Ahmed Louri[2]
[1]Ohio University, US; [2]George Washington University, US

1130 **Performance Evaluation and Design Trade-offs for Wireless-enabled SMART NoC**

Speaker: Karthi Duraisamy, Washington State University, US
Authors: Karthi Duraisamy and Partha Pande, Washington State University, US

1200 **Robust TSV-based 3D NoC Design to Counteract Electromigration and Crosstalk Noise**

Speaker: Partha Pande, Washington State University, US
Authors: Sourav Das[1], Janardhan Rao Doppa[1], Partha Pande[1] and Krishnendu Chakrabarty[2]
[1]Washington State University, US; [2]Duke University, US

1215 **Performance and energy aware wavelength allocation on ring-based WDM 3D optical NoC**

Speaker: Jiating Luo, INRIA/IRISA, FR
Authors: Jiating Luo[1], Ashraf Elantably[1], Pham Van-Dung[1], Cedric Killian[1], Daniel Chillet[1], Sébastien Le Beux[2], Olivier Sentieys[3] and Ian O'Connor[2]
[1]INRIA/IRISA, FR; [2]Lyon Institute of Nanotechnology, FR; [3]INRIA, FR

1230 Lunch Break in Garden Foyer

10.6 Approximate computing and neural networks for novel communication and multimedia systems

5A 1100 - 1230

Chair: Norbert Wehn, Technical University Kaiserslautern, DE
Co-Chair: Gerogios Keramidas, Think Silicon, GR

In this session ideas related to approximate computing and neural networks are presented, which can be applied in novel communication and multimedia systems.

1100 **Exploiting Special-Purpose Function Approximation For Hardware-Efficient QR-Decomposition**

Speaker: Jochen Rust, University of Bremen, DE
Authors: Jochen Rust[1] and Steffen Paul[2]
[1]University of Bremen, DE; [2]University Bremen, DE

1130 **Embracing Approximate Computing for Energy-Efficient Motion Estimation in High Efficiency Video Coding**

Speaker: Muhammad Shafique, Vienna University of Technology (TU Wien), AT
Authors: Walaa El-Harouni[1], Semeen Rehman[2], Bharath Srinivas Prabakaran[2], Akash Kumar[3], Rehan Hafiz[4] and Muhammad Shafique[5]
[1]Private Researcher, DE; [2]TU Dresden, DE; [3]Technische Universitaet Dresden, DE; [4]ITU, PK; [5]Vienna University of Technology (TU Wien), AT

1200 **Hardware Architecture of Bidirectional Long Short-Term Memory Neural Network for Optical Character Recognition**

Speaker: Vladimir Rybalkin, TU Kaiserslautern, DE
Authors: Vladimir Rybalkin[1], Mohammad Reza Yousefi[2], Norbert Wehn[1] and Didier Stricker[3]
[1]University of Kaiserslautern, DE; [2]Augmented Vision Department, German Research Center for Artificial Intelligence (DFKI), DE; [3]German Research Center for Artificial Intelligence (DFKI), DE

IPs **IP5-2**

1230 Lunch Break in Garden Foyer

10.7 Adaptive and Resilient Cyber-Physical Systems

3B 1100 - 1230

Chair: Rolf Ernst, TU Braunschweig, DE
Co-Chair: Paul PoP, Technical University of Denmark, DK

The session contains four regular papers and four IP papers addressing different aspects of adaptivity and resilience for Cyber-Physical Systems. The topic of the first paper is distributed architectures for deep neural networks executing on a set of mobile nodes. The second paper considers scheduling of imprecise computation tasks on MPSoC systems taking the uncertainty of harvested energy into account. The final two papers both considers resilience of CPS. The first presents a scheme for preventing GPS-based hijacking of drones and the last considers how to avoid adversaries from learning what is printed using a 3D

printer. The four IP papers considers control and scheduling co-design, contract-based design, medical CPS, utility-driven data transmission strategies for CPS.

1100 **MoDNN: Local Distributed Mobile Computing System for Deep Neural Network**

Speaker: Yiran Chen, University of Pittsburgh, US
Authors: Jiachen Mao[1], Xiang Chen[2], Kent W. Nixon[1], Christopher Krieger[3] and Yiran Chen[1]
[1]University of Pittsburgh, US; [2]George Mason University, US; [3]University of Maryland, Baltimore County, US

1130 **Energy-Adaptive Scheduling of Imprecise Computation Tasks for QoS Optimization in Real-Time MPSoC Systems**

Speaker: Tongquan Wei, East China Normal University, CN
Authors: Junlong Zhou[1], Jianming Yan[1], Tongquan Wei[1], Mingsong Chen[1] and X, Sharon Hu[2]
[1]East China Normal University, CN; [2]University of Notre Dame, US

1200 **Fix the Leak! An Information Leakage Aware Secured Cyber-Physical Manufacturing System**

Speaker: Mohammad Al Faruque, UCI, US
Authors: Sujit Rokka Chhetri[1], Sina Faezi[1] and Mohammad Al Faruque[2]
[1]University of California, Irvine, US; [2]University of California Irvine, US

1215 **Efficient Drone Hijacking Detection using Onboard Motion Sensors**

Speaker: Zhiwei Feng, Northeastern University, China, CN
Authors: Zhiwei Feng[1], Nan Guan[2], Mingsong Lv[1], Weichen Liu[3], Qingxu Deng[1], Xue Liu[4] and Wang Yi[1]
[1]Northeastern University, CN; [2]Hong Kong Polytechnic University, HK; [3]Chongqing University, CN; [4]McGill University, CA

IPs **IP5-3, IP5-4, IP5-5, IP5-6**

10.8a Smart and Wearable Sensors for Health

Exhibition Theatre 1100 - 1200
Organiser: Patrick Mayor, EPFL, CH
See Page 111

10.8b IoT Edge Devices

Exhibition Theatre 1200 - 1230
See Page 111

1230 Lunch Break in Garden Foyer

11.0 LUNCH TIME KEYNOTE SESSION

Garden Foyer 1320 - 1350
Chair: David Atienza, EPFL, CH
See Page 10

1320 **The Engineering to Medicine Metamorphosis**

Speaker and Author: Sani R. Nassif, Radyalis LLC, US

1400 Session 11

11.1 Wearable and Smart Medical Devices Day: HW and SW design constraints in medical devices

5BC 1400 - 1530

Organisers: José L. Ayala, Universidad Complutense de Madrid, ES
Chris Van Hoof, IMEC, BE
Chair: Maurizio Rossi, University of Trento, IT
Co-Chair: José L. Ayala, Universidad Complutense de Madrid, ES

This session will present the current efforts on making optimal electronic designs for biomedical devices. Therefore, the issues of low power consumption, reconfigurability and design challenges will be analysed in a broad range of medical applications.

1400 **Reconfigurable Embedded Systems Applications for Versatile Biomedical Measurements**

Speaker: Luca Cerina, Politecnico di Milano, IT
Authors: Luca Cerina[1] and Marco D. Santambrogio[2]
[1]politecnico di milano, IT; [2]Politecnico di Milano, IT

1430 **Ultra low power microelectronics for wearable and medical devices**

Speaker: Pierre-François Rüedi, CSEM, CH
Authors: Pierre-François Rüedi, André Bischof, Marcin Kamil Augustyniak, Pascal Persechini, Jean-Luc Nagel, Marc Pons, Stephane Emery and Olivier Chételat, CSEM S.A., CH

1500 **Design Challenges for Wearable EMG Applications**

Speaker: Elisabetta Farella, Fondazione Bruno Kessler - ICT Center, IT
Authors: Bojan Milosevic[1], Simone Benatti[2] and Elisabetta Farella[1]
[1]Fondazione Bruno Kessler (FBK), IT; [2]Università di Bologna, IT

1530 Coffee Break in Exhibition Area

11.2 Emerging Technologies for Future Memory Design

4BC 1400 - 1530

Chair: Weisheng Zhao, Beihang University, CN
Co-Chair: Jean-Michel Portal, Aix-Marseille Université, FR

Memory design based on emerging technologies is critical for the future VLSI design targeting low power and high performance. This session involves novel design method and evaluation tool for emerging technologies (i.e. STT-MRAM, Racetrack memory, Phase Change Memory and Ferroelectric memory etc.) including variation aware design, novel architecture implementation and reliability concern.

1400 **Hybrid VC-MTJ/CMOS Non-volatile Stochastic Logic for Efficient Computing**

Speaker: Shaodi Wang, University of California, Los Angeles, US
Authors: Shaodi Wang[1], Saptadeep Pal[1], Tianmu Li[2], Andrew Pan[2], Cecile Grezes[2], Pedram Khalili-Amiri[2], Kang L. Wang[2] and Puneet Gupta[2]
[1]University of California, Los Angeles, US; [2]UCLA, US

1430 **Design and Benchmarking of Ferroelectric FET based TCAM**

Speaker: Xunzhao Yin, University of Notre Dame, US
Authors: Xunzhao Yin, Michael Niemier and X. Sharon Hu, University of Notre Dame, US

1500 **Leveraging Access Port Positions to Accelerate Page Table Walk in DWM Main Memory**

Speaker: Chengmo Yang, University of Delaware, US
Authors: Hoda Aghaei Khouzani[1], Pouya Fotouhi[2], Chengmo Yang[1] and Guang R. Gao[2]
[1]University of Delaware, US; [2]Department of Electrical and Computer Engineering, University of Delaware, US

1515 **VAET-STT: A Variation Aware Estimator Tool for STT-MRAM based Memories**

Speaker: Sarath Mohanachandran Nair, KIT, Germany, DE
Authors: Sarath Mohanachandran Nair[1], Rajendra Bishnoi[2], Mohammad Saber Golanbari[1], Fabian Oboril[1] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]Karlsruhe Instituite of Technology, DE

IPs **IP5-7, IP5-8**

1530 Coffee Break in Exhibition Area

11.3 Exploiting Heterogeneity for Big Data Computing

2BC 1400 - 1530

Chair: Georgios Keramidas, Think Silicon S.A./Technological Educational Institute of Western Greece, GR
Co-Chair: Houman Homayoun, George Mason University, US

This session introduces new approaches for building reconfigurable accelerators and heterogeneous architectures integrating big-little cores, FPGA hardware, and coarse grain reconfigurable array architectures targeting emerging applications such as Hadoop map reduce framework and neural networks.

1400 **A Novel Zero Weight/Activation-Aware Hardware Architecture of Convolutional Neural Network**

Speaker: Dongyoung Kim, Seoul National University, KR
Authors: Dongyoung Kim, Junwhan Ahn and Sungjoo Yoo, Seoul National University, KR

1430 **A Mechanism for Energy-efficient Reuse of Decoding and Scheduling of x86 Instruction Streams**

Speaker: Antonio Carlos S. Beck, Universidade Federal do Rio Grande do Sul, BR
Authors: Marcelo Brandalero and Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul, BR

1500 **Understanding the Impact of Precision Quantization on the Accuracy and Energy of Neural Networks**

Speaker: Sherief Reda, Brown University, US
Authors: Soheil Hashemi, Nicholas Anthony, Hokchhay Tann, Iris Bahar and Sherief Reda, Brown University, US

1515 **Big vs Little Core for Energy-Efficient Hadoop Computing**

Speaker: Houman Homayoun, George Mason University, US
Authors: Maria Malik[1], Katayoun Neshatpour[1], Tinoosh Mohsenin[2], Avesta Sasan[1] and Houman Homayoun[1]
[1]George Mason University, US; [2]University of Maryland Baltimore County, US

IPs **IP5-9, IP5-10**

1530 Coffee Break in Exhibition Area

11.4 Advances in Timing and Layout

3A 1400 - 1530

Chair: Mark Po-Hung Lin, National Chung Cheng University, TW
Co-Chair: Ibrahim Elfadel, Masdar Institute of Technology, AE

This session focuses on issues related to timing and layout in the presence of manufacturing variability and photolithographic limitations. The first paper reduces pessimism in timing analysis by estimating path sensitization while accounting for delay variations. The second paper enables patterning with reduced wirelength and overlay violation through placement refinement. The third paper improves manufacturability with an optimization algorithm for cut locations in line-end process. The last paper discusses clock tree synthesis to reduce delay sensitivity mismatch with gate delay circuitry.

1400 **Quantifying Error: Extending Static Timing Analysis with Probabilistic Transitions**

Speaker: Kevin Murray, University of Toronto, CA
Authors: Kevin E. Murray[1], Andrea Suardi[2], Vaughn Betz[1] and George Constantinides[2]
[1]University of Toronto, CA; [2]Imperial College, GB

1430 **On Refining Standard Cell Placement for Self-aligned Double Patterning**

Speaker: Ting-Chi Wang, National Tsing Hua University, TW
Authors: Ye-Hong Chen, Sheng-He Wang and Ting-Chi Wang, National Tsing Hua University, TW

1500 **Cut Mask Optimization for Multi-Patterning Directed Self-Assembly Lithography**

Speaker: Wachirawit Ponghiran, School of Electrical Engineering, KAIST, KR
Authors: Wachirawit Ponghiran[1], Seongbo Shim[2] and Youngsoo Shin[3]
[1]School of Electrical Engineering, KAIST, KR; [2]Dept. of Electrical Engineering, KAIST, KR; [3]KAIST, KR

1515 **Clock Data Compensation Aware Clock Tree Synthesis in Digital Circuits with Adaptive Clock Generation**

Speaker: Saibal Mukhopadhyay, Georgia Institute of Technology, US
Authors: Taesik Na, Jong Hwan Ko and Saibal Mukhopadhyay, Georgia Institute of Technology, US

IPs **IP5-11**

1530 Coffee Break in Exhibition Area

11.5 Smart Energy and Automotive Systems

3C 1400 - 1530

Chair: Geoff Merrett, University of Southampton, GB
Co-Chair: Michele Magno, ETHZ, CH

This session presents the state of the art in efficient automotive software, smart battery systems and the latest strives toward energy neutral wireless communications systems.

1400 **On Reducing Busy Waiting in AUTOSAR via Task-Release-Delta-based Runnable Reordering**

Speaker: Robert Höttger, Dortmund University of Applied Sciences and Arts, DE
Authors: Robert Höttger[1], Olaf Spinczyk[2] and Burkhard Igel[1]
[1]FH-Dortmund, DE; [2]TU-Dortmund, DE

1430 **Power Neutral Performance Scaling for Energy Harvesting MP-SoCs**

Speaker: Benjamin Fletcher, University of Southampton, GB
Authors: Benjamin Fletcher, Domenico Balsamo and Geoff Merrett, University of Southampton, GB

1500 **Efficient Decentralized Active Balancing Strategy for Smart Battery Cells**

Speaker: Nitin Shivaraman, Nanyang Technological University, SG
Authors: Nitin Shivaraman[1], Arvind Easwaran[1] and Sebastian Steinhorst[2]
[1]Nanyang Technological University, SG; [2]Technical University of Munich, DE

1515 **WULoRa: An Energy Efficient IoT End-Node for Energy Harvesting and Heterogeneous Communication**

Speaker: Michele Magno, ETH Zurich, CH
Authors: Michele Magno[1], Fayçal Ait Aoudia[2], Matthieu Gautier[3], Olivier Berder[4] and Luca Benini[5]
[1]ETH Zurich, CH; [2]Irisa - University of Rennes, FR; [3]University of Rennes [1], IRISA, INRIA, FR; [4]Irisa -University of Rennes, FR; [5]Università di Bologna, IT

IPs **IP5-12, IP5-13, IP5-14, IP5-15**

1530 Coffee Break in Exhibition Area

11.6 Dependable microprocessors and systems

5A 1400 - 1530

Chair: Maksim Jenihhin, Tallinn University f Technology, EE
Co-Chair: Antonio Miele, Politecnico di Milano, IT

The section presents two papers investigating the effects of soft errors on critical registers and hardware methods to detect intrusion attacks in microprocessors. A third paper provides a solution for estimating multiprocessor expected lifetime.

1400 **Characterization of stack behavior under soft errors**

Speaker: Junchi Ma, School of Computer Science and Engineering, Southeast University, CN
Authors: Junchi Ma and Yun Wang, School of Computer Science and Engineering, Southeast University, CN

1430 **Multi-Armed Bandits for Efficient Lifetime Estimation in MPSoC design**

Speaker: Brett Meyer, McGill University, CA
Authors: Calvin Ma, Aditya Mahajan and Brett Meyer, McGill University, CA

1500 **Hardware-based On-line Intrusion Detection via System Call Routine Fingerprinting**

Speaker: Yiorgos Makris, The University of Texas at Dallas, US
Authors: Liwei Zhou and Yiorgos Makris, The University of Texas at Dallas, US

IPs **IP5-16, IP5-17**

1530 Coffee Break in Exhibition Area

11.7 Formal Methods and Verification: Core Technologies and Applications

3B 1400 - 1530

Chair: Barbara Jobstmann, EPFL / Cadence, CH
Co-Chair: Christoph Scholl, University of Freiburg, DE

The session consists of three papers on formal verification and its applications. The first paper presents the use of grammar-based techniques for the analysis of high-end processor designs at the netlist level. The second paper considers a computer algebra-based technique to reverse engineer the irreducible polynomial used in the implementation of multipliers in finite fields. The third paper applies probabilistic model checking in a case study analyzing the dependability of optical communication networks with double-ring topologies (which have been proposed for multicast traffic in metropolitan areas).

1400 **Static Netlist Verification for IBM High-Frequency Processors using a Tree-Grammar**

Speaker: Christoph Jaeschke, IBM Deutschland Research & Development GmbH, DE
Authors: Christoph Jaeschke, Ulla Herter, Claudia Wolkober, Carsten Schmitt and Christian Zoellin, IBM Deutschland Research & Development GmbH, DE

1430 **Reverse Engineering of Irreducible Polynomials in GF(2^m) Arithmetic**

Speaker: Cunxi Yu, University of Massachusetts, Amherst, US
Authors: Cunxi Yu[1], Daniel Holcomb[1] and Maciej Ciesielski[2]
[1]University of Massachusetts, Amherst, US; [2]University of Massachusetts Amherst, US

1500 **Formal Specification and Dependability Analysis of Optical Communication Networks**

Speaker: Khaza Anuarul Hoque, University of Oxford, GB
Authors: Umair Siddique[1], Khaza Anuarul Hoque[2] and Taylor T Johnson[3]
[1]McMaster University, CA; [2]University of Oxford, GB; [3]University of Texas at Arlington, US

1530 Coffee Break in Exhibition Area

11.8 Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs

Exhibition Theatre 1400 - 1530

Organisers: Andy M. Tyrrell, University of York, GB
Lukas Sekanina, Brno University of Technology, CZ
Chair: Andy M. Tyrrell, University of York, GB
Co-Chair: Lukas Sekanina, Brno University of Technology, CZ

See Page 112

1530 Coffee Break in Exhibition Area

IP5 Interactive Presentations

IP sessions (in front of rooms 4A and 5A) 1530 - 1600

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. At the end of each afternoon Interactive Presentations session the award 'Best IP of the Day' is given.

IP5-1 Formal Model for System-Level Power Management Design

Speaker: Mirela Simonovic, Aggios, RS
Authors: Mirela Simonovic[1], Vojin Zivojnovic[2] and Lazar Saranovac[3]
[1]University of Belgrade, RS; [2]AGGIOS Inc., US; [3]University of Belgrade, School of Electrical Engineering, RS

IP5-2 Extending Memory Capacity of Neural Associative Memory based on Recursive Synaptic Bit Reuse

Speaker: Tianchan Guan, Columbia University, US
Authors: Tianchan Guan[1], Xiaoyang Zeng[1] and Mingoo Seok[2]
[1]Fudan University, CN; [2]Columbia University, US

IP5-3 Anomalies in Scheduling Control Applications and Design Complexity

Speaker: Amir Aminifar, Swiss Federal Institute of Technology in Lausanne, CH
Authors: Amir Aminifar[1] and Enrico Bini[2]
[1]Swiss Federal Institute of Technology in Lausanne (EPFL), CH; [2]University of Turin, IT

IP5-4 Contract-Based Integration of Automotive Control Software

Speaker: Tobias Sehnke, IAV GmbH, DE
Authors: Tobias Sehnke[1], Matthias Schultalbers[2] and Rolf Ernst[3]
[1]Control Engineering Excellence Cluster of IAV GmbH, DE; [2]Gasoline Engines, IAV GmbH, DE; [3]Inst. of Comput. & Network Eng, Tech. Univ. Braunschweig, DE

IP5-5 Modeling and Integrating Physical Environment Assumptions in Medical Cyber-Physical System Design

Speaker: Chunhui Guo, Illinois Institute of Technology, US
Authors: Zhicheng Fu[1], Chunhui Guo[1], Shangping Ren[1], Yu Jiang[2] and Lui Sha[3]
[1]Illinois Institute of Technology, US; [2]Tsinghua University, CN; [3]University of Illinois at Urbana-Champaign, US

IP5-6 A Utility-Driven Data Transmission Optimization Strategy in Large Scale Cyber-Physical Systems

Speaker: Bei Yu, The Chinese University of Hong Kong, HK
Authors: Soumi Chattopadhyay[1], Ansuman Banerjee[1] and Bei Yu[2]
[1]Indian Statistical Institute, IN; [2]The Chinese University of Hong Kong, HK

IP5-7 Protect Non-volatile Memory from Wear-out Attack based on Timing Difference of Row Buffer Hit/Miss

Speaker: Haiyu Mao, Tsinghua University, CN
Authors: Haiyu Mao[1], Xian Zhang[2], Guangyu Sun[2] and Jiwu Shu[1]
[1]Tsinghua University, CN; [2]Peking University, CN

IP5-8 Effects of Cell Shapes on the Routability of Digital Microfluidic Biochips

Speaker: Oliver Keszöcze, University of Bremen, DE
Authors: Kevin Leonard Schneider[1], Oliver Keszocze[1], Jannis Stoppe[1] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen/DFKI, DE

IP5-9 **LESS: Big Data Sketching and Encryption on Low Power Platform**
Speaker: Amey Kulkarni, University of Maryland Baltimore County, US
Authors: Amey Kulkarni[1], Colin Shea[2], Houman Homayoun[3] and Tinoosh Mohsenin[2]
[1]University of Maryland, Baltimore County, US; [2]University of Maryland Baltimore County, US; [3]George Mason University, US

IP5-10 **TruncApp: A Truncation-based Approximate Divider for Energy Efficient DSP Applications**
Speaker: Ali Afzali-Kusha, University of Tehran, IR
Authors: Shaghayegh Vahdat[1], Mehdi Kamal[1], Ali Afzali-Kusha[1], Zainalabedin Navabi[1] and Massoud Pedram[2]
[1]University of Tehran, IR; [2]University of Southern California, US

IP5-11 **Timing-Aware Wire Width Optimization for SADP Process**
Speaker: Youngsoo Song, KAIST, KR
Authors: Youngsoo Song, Sangmin Kim and Youngsoo Shin, School of Electrical Engineering, KAIST, KR

IP5-12 **Formal Timing Analysis of Non-Scheduled Traffic in Automotive Scheduled TSN Networks**
Speaker: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE
Authors: Fedor Smirnov[1], Michael Glaß[2], Felix Reimann[3] and Jürgen Teich[4]
[1]Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE; [2]Ulm University, DE; [3]Audi Electronics Venture GmbH, DE; [4]University of Erlangen-Nuremberg, DE

IP5-13 **Ultra Low-Power Visual Odometry for Nano-Scale Unmanned Aerial Vehicles**
Speaker: Daniele Palossi, ETH Zurich, CH
Authors: Daniele Palossi[1], Andrea Marongiu[2] and Luca Benini[3]
[1]ETH - Zurich, CH; [2]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [3]Università di Bologna, IT

IP5-14 **Long range wireless sensing powered by plant-microbial fuel cell**
Speaker: Maurizio Rossi, University of Trento, IT
Authors: Maurizio Rossi, Pietro Tosato, Luca Gemma, Luca Torquati, Cristian Catania, Sergio Camalò and Davide Brunelli, University of Trento, IT

IP5-15 **On the Cooperative Automatic Lane Change: Speed Synchronization and Automatic "Courtesy"**
Speaker: Alexandre Lombard, UTBM, FR
Authors: Alexandre Lombard[1], Florent Perronet[1], Abdeljalil ABBAS-TURKI[2] and Abdellah El-Moudni[1]
[1]UTBM, FR; [2]Université de Technologie de Belfort-Montbéliard, FR

IP5-16 **Evaluating Matrix Representations for Error-Tolerant Computing**
Speaker: Pareesa Golnari, Princeton University, US
Authors: Pareesa Ameneh Golnari and Sharad Malik, Princeton University, US

IP5-17 **Simulation-Based Design Procedure for sub 1 V CMOS Current Reference**
Speaker: Dmitry Osipov, University of Bremen, DE
Authors: Dmitry Osipov and Steffen Paul, University of Bremen, DE

1600 Session 12

12.1 Wearable and Smart Medical Devices Day: Industry panel: Industrial challenges for tomorrow's medical devices and tools

5BC 1600 - 1730

Organisers: José L. Ayala, Universidad Complutense de Madrid, ES
Chris Van Hoof, IMEC, BE
Chair: Nick Van Helleputte, imec, BE
Co-Chair: José L. Ayala, Universidad Complutense de Madrid, ES

This panel will analyze the Industrial challenges for tomorrow's medical devices and tools. We expect the invited industries to provide their view in how technology, market and users will drive the evolution of medical devices.

Panelists:

Adrian Ionescu, Xsensio, CH
David Bailey, Sensimed, CH
Kamiar Aminian, GaitUp, CH
Carl Van Himbeeck, Cochlear, BE

12.2 Advances in Microfluidics and Neuromorphic Architectures

4BC 1600 - 1730

Chair: Tsung-Yi Ho, National Tsing Hua University, TW
Co-Chair: Li Jiang, Shanghai Jiao Tong University, CN

This session consists of four presentations from emerging applications in EDA such as mircrofluidics and neural networks. The first presentation proposes a progressive optimization procedure for the synthesis of fault-tolerant flow-based microfluidics. The second presentation presents a hybrid microfluidic platform that enables single-cell analysis on a heterogeneous cells. Next presentation discusses automatic verification on networked labs-on-chip architecture. The final presentation proposes synthesis method for parallel convolutional layers of convolutional neural network.

1600 **Fast Architecture-Level Synthesis of Fault-Tolerant Flow-Based Microfluidic Biochips**

Speaker: Tsung-Yi Ho, National Tsing Hua University, TW
Authors: Wei-Lun Huang[1], Ankur Gupta[2], Sudip Roy[2], Tsung-Yi Ho[1] and Paul Pop[3]
[1]National Tsing Hua University, TW; [2]Indian Institute of Technology Roorkee, IN; [3]Technical University of Denmark, DK

1630 **CoSyn: Efficient Single-Cell Analysis Using a Hybrid Microfluidic Platform**

Speaker: Mohamed Ibrahim, Duke University, US
Authors: Mohamed Ibrahim[1], Krishnendu Chakrabarty[1] and Ulf Schlichtmann[2]
[1]Duke University, US; [2]TU München, DE

1700 **Verification of Networked Labs-on-Chip Architectures**

Speaker: Andreas Grimmer, Johannes Kepler University of Linz, AT
Authors: Andreas Grimmer[1], Werner Haselmayr[1], Andreas Springer[1] and Robert Wille[2]
[1]Johannes Kepler University, AT; [2]Johannes Kepler University Linz, AT

1715 **Synthesis of Activation-Parallel Convolution Structures for Neuromorphic Architectures**

Speaker: Seban Kim, Incheon National University, KR
Authors: Seban Kim and Jaeyong Chung, Incheon National University, KR

12.3 Security Tools

2BC 1600 - 1730

Chair: Francesco Regazzoni, AlaRI/USI, CH
Co-Chair: Georg Sigl, TU Munich, DE

Security tools provide support to build secure systems. Such techniques have made great progress in past years with improvements in SAT solvers, theorem provers and available computing power. This session includes papers that perform information flow checks on hardware designs, to check for information leaks either directly through analysis of the design or indirectly through timing channels.

1600 **Register Transfer Level Information Flow Tracking for Provably Secure Hardware Design**

Speaker: Armaiti Ardeshiricham, University of California, San Diego, US
Authors: Armaiti Ardeshiricham[1], Wei Hu[2], Joshua Marxen[2] and Ryan Kastner[3]
[1]University of California San Diego, US; [2]University of California, San Diego, US; [3]UCSD, US

1630 **Dude, is my code constant time?**

Speaker: Oscar Reparaz, KU Leuven/COSIC, BE
Authors: Oscar Reparaz[1], Josep Balasch[1] and Ingrid Verbauwhede[2]
[1]KU Leuven, BE; [2]KU Leuven - COSIC, BE

1700 **Information Flow Tracking in Analog/Mixed-Signal Designs through Proof-Carrying Hardware IP**

Speaker: Yiorgos Makris, The University of Texas at Dallas, US
Authors: Mohammad-Mahdi Bidmeshki, Angelos Antonopoulos and Yiorgos Makris, The University of Texas at Dallas, US

12.4 Formal and Predictive Models for System Design

3A 1600 - 1730

Chair: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair: Michael Huebner, Ruhr-University Bochum, DE

The first paper presents a predictive approach to measure the impact of platform changes on the application perfomance. The second paper introduces a unifying approach for expressing multiple models of computations. The final paper compares two alternative implementations to realize faithfully the logical execution time model of computation.

1600 **Sampling-Based Binary-Level Cross-Platform Performance Estimation**

Speaker: Xinnian Zheng, University of Texas at Austin, US
Authors: Xinnian Zheng, Haris Vikalo, Shuang Song, Lizy K. John and Andreas Gerstlauer, The University of Texas at Austin, US

1630 **A Layered Formal Framework for Modeling of Cyber-Physical Systems**

Speaker: George Ungureanu, KTH Royal Institute of Technology, SE
Authors: George Ungureanu and Ingo Sander, KTH Royal Institute of Technology, SE

1700 **Efficient Synchronization Methods for LET-based Applications on a Multi-Processor System on Chip**

Speaker: Gabriela Breaban, Technical University of Eindhoven, NL
Authors: Gabriela Breaban, Sander Stuijk and Kees Goossens, Technical University of Eindhoven, NL

12.5 Power Modeling, Estimation and Verification

3C 1600 - 1730

Chair: Pascal Vivet, CEA-LETI, FR
Co-Chair: Hiroshi Nakamura, University of Tokyo, JP

This session covers a wide scope on power modeling and estimation in circuit design. The first paper presents a new model for modeling electromigration in power grid network, taking into account transient effects. The second paper introduces a fast and accurate thermal simulator for 3D circuits, taking into acccount thermal leakage dependency. The third paper proposes a new identification technique of fine grain power sources for multi-core without the knowledge of the thermal model. The last paper presents rule based checking for quick verification at implementation level of the power intent defined in UPF.

1600 **Physics-based Electromigration Modeling and Assessment for Multi-Segment Interconnects in Power Grid Networks**

Speaker: Xiaoyi Wang, Beijing University of Technology, CN
Authors: Xiaoyi Wang[1], Hongyu Wang[2], Jian He[1], Sheldon X.-D. Tan[3], Yici Cai[4] and Shengqi Yang[2]
[1]Beijing Advanced Innovation Center for Future Internet Technology, Beijing Engineering Research Center for IoT Software and Systems, Beijing University of Technology, CN; [2]Beijing University of Technology, CN; [3]University of California, Riverside, US; [4]TsingHua University, CN

1630 **A Fast Leakage Aware Thermal Simulator for 3D Chips**

Speaker: Hameedah Sultan, IIT Delhi, IN
Authors: Hameedah Sultan and Smruti R. Sarangi
IIT Delhi, IN

1700 **Blind Identification of Power Sources in Processors**

Speaker: Sherief Reda, Brown University, US
Authors: Sherief Reda[1] and Adel Belouchrani[2]
[1]Brown University, US; [2]ENP, Algeria, DZ

1715 **Fast Low Power Rule Checking for Multiple Power Domain Design**

Speaker: Iris Hui-Ru Jiang, National Chiao Tung University, TW
Authors: Chien-Pang Lu[1] and Iris Hui-Ru Jiang[2]
[1]MediaTek, TW; [2]National Chiao Tung University, TW

12.6 Efficient design methodologies for high-performance analog circuits and systems.

5A 1600 - 1730

Chair: Nuno Horta, Instituto de Telecomunicacoes, PT
Co-Chair: Deuk Heo, Washington State University, US

This session presents area- and energy-efficient design methodologies for high-performance analog circuits and systems. These papers include an energy-efficient asynchronous digital design method for digitally-assisted analog circuits, a design method of high-density energy storage components, and a robust communication link design for communication systems.

1600 **Benefits of Asynchronous Control for Analog Electronics: Multiphase Buck Case Study**

Speaker: Danil Sokolov, Newcastle University, GB
Authors: Danil Sokolov[1], Vladimir Dubikhin[1], Victor Khomenko[1], David Lloyd[2], Andrey Mokhov[1] and Alex Yakovlev[1]
[1]Newcastle University, GB; [2]Dialog Semiconductor, GB

1630 **High-Density MOM Capacitor Array with Novel Mortise-Tenon Structure for Low-Power SAR ADC**

Speaker: Pang-Yen Chou, Technical University of Munich, DE
Authors: Nai-Chen Chen[1], Pang-Yen Chou[2], Helmut Graeb[3] and Mark Po-Hung Lin[1]
[1]National Chung Cheng University, TW; [2]Technische Universität München, DE; [3]TU Muenchen, DE

1700 **Adaptive Interference Rejection in Human Body Communication using Variable Duty Cycle Integrating DDR Receiver**

Speaker: Shreyas Sen, Purdue University, US
Authors: Shovan Maity[1], Debayan Das[1] and Shreyas Sen[2]
[1]Purdue University, US; [2]ECE, Purdue University, US

12.7 Software optimization for emerging memory architectures and technologies

3B 1600 - 1730

Chair: Amit Singh, University of Southampton, GB
Co-Chair: Semeen Rehman, Technische Universitaet Dresden, DE

The papers in this session propose optimization techniques to improve the lifetime and performance of emerging technologies like persistent memory and scalable many-cores. Architectural optimizations are also presented to improve energy and performance of applications executing on GPU-based platforms.

1600 **Efficient Storage Management for Aged File Systems on Persistent Memory**

Speaker: Kaisheng Zeng, Tsinghua University, CN
Authors: Kaisheng Zeng[1], Youyou Lu[1], Hu Wan[2] and Jiwu Shu[1]
[1]Tsinghua University, CN; [2]Capital Normal University, CN

1630 **LookNN: Neural Network with No Multiplication**

Speaker: Tajana Rosing, UCSD, US
Authors: Mohammad Samragh Razlighi[1], Mohsen Imani[1], Farinaz Koushanfar[2] and Tajana Rosing[2]
[1]University of California San Diego, US; [2]UCSD, US

1700 **Pegasus: Efficient Data Transfers for PGAS Languages on Non-Cache-Coherent Many-Cores**

Speaker: Manuel Mohr, Karlsruhe Institute of Technology, DE
Authors: Manuel Mohr and Carsten Tradowsky, Karlsruhe Institute of Technology, DE

12.8 Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology

Exhibition Theatre 1600 - 1730

Organisers: Paul Pop, Technical University of Denmark, DK
Seetal Potluri, Technical University of Denmark, DK
Chair: Jan Madsen, Technical University of Denmark, DK
Co-Chair: Seetal Potluri, Technical University of Denmark, DK

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W01 VLSI for IoT

3B 0830 - 1730

Organisers: Marilyn Wolf, Georgia Institute of Technology, US
Saibal Mukhopadhyay, Georgia Institute of Technology, US
Jörg Henkel, Karlsruhe Institute of Technology, DE

This workshop focuses on the intersection between IoT and the VLSI systems required to build IoT systems. Internet-of-Things technology is being applied to a huge range of application areas. IoT systems make use of wireless networking to build physically distributed soft real-time systems. To fully deliver on the promise of IoT, we need to develop a new generation of VLSI devices for IoT nodes and hubs. IoT pushes VLSI system design in an entirely new direction - rather than concentrate on building the biggest, most complex chips, we need to develop a new generation of small, extremely inexpensive chips. This new generation of IoT devices will require advances in packaging, circuit design, low-power design, security, and system architectures.The workshop features both invited speakers and submitted contributions from workshop participants. Interested participants can submit a 1-page summary of their proposed contribution by Friday, February 17, 2017 at: easychair.org/conferences/?conf=vlsiiot17. Results will be announced by March 1, 2017.

0830 - 1015 **Devices and Systems**

VLSI design - low power sensing and computation, wireless communication - defines the properties of IoT node devices. This session sets the stage for the day's discussion of VLSI for IoT. The first talk outlines how low power and low cost devices will influence the network architectures of IoT systems. The second talk proposes a fog-based paradigm for the IoT systems.

0830 Small Is Beautiful: The New VLSI Landscape
Speaker: Marilyn Wolf, Georgia Tech, US

0930 Towards a Fog Computing Paradigm for Industrial Internet of Things
Speaker: Paul Pop, Technical University of Denmark, DK

1030 - 1200 **Architectures and Applications**

This session looks at the architecture of IoT nodes and the characteristics of IoT applications. Hardware/software co-design techniques are well-suited to the design of low-power IoT nodes. Energy-oriented applications---smart grids and electric vehicles---offer key applications for IoT systems.

1030 Customizable Processor Acceleration of Time Series Similarity Search for the Internet of Things
Speaker: Philip Brisk, University of California, Riverside, US

1115 Deploying IoT for Energy Efficient Applications - Smart Grid and Electric Vehicles
Speaker: Mohammad al Faruque, UC Irvine, US

1415 - 1500 **Circuits and Systems**

Novel circuits enable new IoT applications. This session looks at two system designs for novel applications: personal health monitoring and neural-inspired image processing.

1330 Ultra-Low Power Neural Image Processing
Speaker: Saibal Mukhopadhyay, Georgia Institute of Technology, US

1415 Toward Smart Wearable Systems for Personal Health Monitoring
Speaker: Yu Cao, Arizona State University, US

1500 - 1630 **SoC Design around ARM Cortex-M0 for Energy-efficient IoT Applications**
Organisers: Xabier Iturbe, ARM Research, GB
Victor Nelson, Auburn University, US

This talk explores various areas of IoT in the context of existing technologies and discusses features of the ARM Cortex-M family of CPUs suitable for applications interesting to IoT. The talk will be followed by a demo on prototyping an IoT application built on the framework of the SoC Design Education Kit from ARM University Program using the energy-efficient ARM Cortex-M0 DesignStart IP core.

1500 SoC Design around ARM Cortex-M0 for Energy-efficient IoT Applications: Techniqwues
Speaker: Victor Nelson, Auburn University, US

1530 SoC Design around ARM Cortex-M0 for Energy-efficient IoT Applications: Demonstrations
Speaker: Victor Nelson, Auburn University, US

1645 - 1730 **Participant Presentations and Discussions**

Presentations from workshop participants and group discussion of workshop topics.

W02 Emerging Memory Solutions - Technology, Manufacturing, Architectures, Design and Test

2A 0830 - 1700

General Chair: Christian Weis, University of Kaiserslautern, DE
Programme Chair: Bastien Giraud, CEA-LETI, Minatec, FR
Panel Chair: Ian O'Connor, Ecole Centrale de Lyon, FR
Publicity Chair: Matthias Jung, University of Kaiserslautern, DE
Proceedings Chair: Jean-Philippe Noel, CEA-Leti, FR
Steering Committee Member: Erik Jan Marinissen, IMEC, BE

Scope

Memory manufacturing, architectures, design and test were deeply investigated in-depth to address issues linked to technology scaling such as increasing static power, maximum operating frequency and the gap between logic and memory minimum voltages. Various emerging memories solutions have appeared in recent years with the aim to replace either partially or completely already existing memories in order to overcome both technology and design related limitations while giving answers to the aggressive requirements of many different applications. The goal of this Workshop is to bring together researchers, practitioners, designers and other people interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss the future challenges and trends.

Subjects of interest

You are invited to participate and submit your contributions to DATE 2017 Friday Workshop on Emerging Memory Solutions. The areas of interest include (but are not limited to) the following topics:

- Volatile memory design (SRAM, DRAM, CAM, etc.)
- Non-Volatile memory design (ReRAM, Flash, PCM, MRAM, etc.)
- Applications of emerging devices in memories (TFETs, CNTs, nanowires, etc.)
- 3D memories (volatile and non-volatile)
- In-Memory and Near-Memory Processing
- Memory Application for emerging markets
- Memory test, BIST and debug techniques
- Applications, products and prototypes of new memories

Panel

The panel of the workshop will be about the topic "Can We Jump over the Memory Wall with In-Memory Computing?". We looking forward to a very lively discussion moderated by our panel chair Ian O'Connor.

0830 - 0915 **Opening and 1st Keynote**
Chair: Christian Weis, University of Kaiserslautern, DE

0830 Welcome Addresss
Speaker: Christian Weis, University of Kaiserslautern, DE

0835 Keynote: "Tomorrow's Memory Systems"
Speaker: Bruce Jacob, University of Maryland, US

FRIDAY 31 MARCH, 2017

0915 - 1000 **Special Session on Emerging Memory Applications**
Chair: Pascal Vivet, CEA-LETI, FR

0915 Narrower-purpose Computing for Efficient Near-Memory Processing
Speaker: Stephan Diestelhorst, ARM, GB

0940 SMCSim: An Accurate Simulation Framework for the Smart Memory Cube
Speaker: Erfan Azarkhish, DEIS, University of Bologna, Bologna, IT

1000 - 1030 **Coffee Break and Poster Session I**
See for the Poster List below.

1030 - 1200 **Invited Talk and Panel**
Moderator: Ian O'Connor, Ecole Centrale de Lyon, FR

1030 Cortical Processors and Memories!
Speaker: Paul Franzon, NC State University, US

1100 Panel: "Can We Jump over the Memory Wall with In-Memory Computing?"
Panelists: Francky Catthoor[1], Ahmed Hemani[2], Jean-Francois Roy[3], Elisa Vianello[4] and Said Hamdioui[5]
[1]IMEC, BE; [2]Royal Institute of Technology, SE; [3]UPMEM, FR; [4]CEA-LETI, FR; [5]Delft University of Technology, NL

1200 - 1300 **Lunch Break**

1300 - 1430 **2nd Keynote and Special Session II**
Chair: Bastien Giraud, CEA-LETI, Minatec, FR

1300 Keynote: Energy-Efficient Processing and Why the Memory Matters
Speaker: Borivoje Nikolic, UC Berkeley, US

1330 Pushing the limits: challenges of low-voltage operation in ULL High Density (HD) SRAM
Speaker: Lorenzo Ciampolini, STM, FR

1350 Evaluation of ternary computing approaches with NVM technologies
Speaker: Dietmar Fey, FAU, DE

1410 Resistive RAM-Centric Computing: Design and Modeling Methodology
Speaker: Haitong Li, Stanford University, US

1430 - 1500 **Coffee Break and Poster Session II**
See for the Poster List below.

1500 - 1600 **Special Session on Emerging RRAMs and MRAMs**
Chair: Said Hamdioui, Delft University of Technology, NL

1500 SOT-MRAM : an energy efficient cache memory alternative
Speaker: Marc Drouard, Antaios, FR

1520 Majority-based Synthesis for RRAM-based in-memory computing
Speaker: Pierre-Emmanuel Gaillardon, University of Utah, US

1540 An overview of Normally-off MCU based on hybrid NVM/CMOS circuits
Speaker: Jean-Michel Portal, IM^{2}NP, FR

1600 - 1650 **Open Call Paper Session**
Chair: Matthias Jung, University of Kaiserslautern, DE

1600 Ultra-Low Power and Compact TFET Multibit Latch and its Applications for Low Voltage Applications
Speaker: Navneet Gupta, CEA-LETI, FR

1620 MAGPIE: System-level Evaluation of Manycore Systems with Emerging Memory Technologies
Speaker: Bruguier Florent, University of Montpellier, FR

Poster List:

A Non-Volatile Flip-Flop Using Memristive Voltage Divider
Author: Mehrdad Biglari, FAU, DE

In-Memory Computation of Transitive Closure
Author: Alvaro Velasquez, University of Central Florida, US

A Scalable Near-Data Processing Simulator
Author: Geraldo Francisco de Oliveira Junior, Universidade Federal do Rio Grande do Sul, BR

Disruptive 3D Technology: Recent Advances on COOLCUBE(TM)
Author: Mélanie Brocard, CEA-LETI, FR

300 MM & 200 MM ADVANCED MEMORY PLATFORM AND MPW SHUTTLE AT LETI
Author: Elisa Vianello, CEA-LETI, FR

4T SRAM Bitcell in 3D CoolCube Technology Exploiting Dynamic Back Biasing
Author: Réda Boumchedda, CEA-Leti, FR

1650 **Remarks**
Speakers: Christian Weis[1] and Bastien Giraud[2]
[1]University of Kaiserslautern, DE; [2]CEA-LETI, Minatec, FR

1650 - 1700 **Closing**

W03 4th Workshop on Design Automation for Understanding Hardware Designs DUHDe 2017

2B 0830 - 1700

Organisers: Ian Harris, University of Californa Irvine, US
Mathias Soeken, EPFL, CH

The design process is essentially a creative process which is reliant on the ability of designers to balance the interactions between a complex set of constraints to arrive at successful solutions. In order for designers to manage this task, they must collectively have a complete understanding of the behavior of the system, the mapping between behavior and structure, and the impact of each design feature on constraints such as power, performance, cost, and security. Design tasks require reasoning across multiple levels of abstraction in order to determine the impact of high-level design decisions, or to trace a design characteristic back to the feature which caused it. In a real design, cross-abstraction reasoning is difficult because the relationships between the different abstractions of a design are not captured. Designer time is expended discovering these cross-abstraction relationships in order to perform design, verification, and maintenance tasks. This workshop will present the state-of-the-art in Design Understanding, research in approaches to provide designers with the design information needed in a concise and straightforward way.

0830 - 0835 **Welcome**

0835 - 0935 **Invited Talk: Dr. Barbara Jobstmann EPFL, Lausanne, Switzerland**

0835 **Title: TBA**
Speaker: Barbara Jobstmann, EPFL, CH

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0935 - 1000 **Research Session 1**

0935 ELVE: An Interactive and Extensible Visualisation Tool for Logic Circuits
Authors: Gregoire Hirt[1], Ana Petkovska[1] and Paolo Ienne[2]
[1]EPFL, CH; [2]EPFL I&C LAP, CH

1000 - 1030 **Coffee Break**

1030 - 1130 **Invited Talk: Dr. Martin Monperrus University of Lille & INRIA, France**

1030 **Title: TBA**
Speaker: Martin Montperrus, University of Lille & INRIA, FR

1130 - 1155 **Research Session 2**

1130 Mining Latency Guarantees for RT-level Designs
Authors: Jan Malburg[1], Heinz Riener[2] and Goerschwin Fey[3]
[1]German Aerospace Center, DE; [2]DLR, DE; [3]Univ. of Bremen, DE

1200 - 0100 **Lunch Break**

1300 - 1440 **Research Session 3**

1300 Verilog2GEXF Dynamic Large Scale Circuit Visualization
Authors: Kenneth Schmitz[1], Jannis Stoppe[2] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]Universität Bremen, DE; [3]Department of Mathematics and Computer Science, University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, DE

1325 Computing Exact Fault Candidates Incrementally
Authors: Heinz Riener[1] and Goerschwin Fey[2]
[1]DLR, DE; [2]Univ. of Bremen, DE

1350 A Human-Centered Approach to Routing for Digital Microfluidic Biochip
Authors: Oliver Keszöcze[1], Andre Pols[2] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]University of Bremen, AD; [3]Department of Mathematics and Computer Science, University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, DE

1415 Making Waveforms Great Again
Authors: Jannis Stoppe[1] and Rolf Drechsler[2]
[1]Universität Bremen, DE; [2]Department of Mathematics and Computer Science, University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, DE

1440 - 1500 **Coffee Break**

1500 - 1600 **Invited Talk: Shalini Ghosh, SRI International, USA**

1500 **Title: TBA**
Speaker: Shalini Ghosh, SRI International, US

1600 - 1650 **Research Session 4**

1600 A Natural Language Interface to Design Cyber-Physical Systems
Authors: Sophia Balkovski[1] and Ian Harris[2]
[1]University of California Irvine, US; [2]University of Californa Irvine, US

1625 On Identifying Functional Primitives in Hardware Description Language (HDL) Specifications
Authors: Christian Krieg[1], Martin Mosbeck[2], Clifford Wolf[2] and Axel Jantsch[3]
[1]Institute of Computer Technology, Vienna University of Technology, AT; [2]TU Wien, AT; [3]Technische Universität Wien, AT

1650 - 1700 **Closing Session**

W04 MOS-AK Workshop

2C 0830 - 1730

Organisers: Jean-Michel Sallese, EDLab, EPFL, CH
Wladek Grabinski, MOS-AK, CH

Arbeitskreis Modellierung von Systemen und Parameterextraktion
Modeling of Systems and Parameter Extraction Working Group

Synopsis:

HiTech forum to discuss the frontiers of electron device modeling with emphasis on simulation-aware compact/SPICE models.

The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

Topics to be covered include the following

- Advances in semiconductor technologies and processing
- Compact Modeling (CM) of the electron devices
- Verilog-A language for CM standardization
- New CM techniques and extraction software
- FOSS TCAD/EDA modeling and simulation
- CM of passive, active, sensors and actuators
- Emerging Devices, TFT CMOS and SOI-based memory cells
- Organic, Bio/Med devices/technology modeling
- Microwave, RF device modeling, HV/Power device modeling
- Nanoscale CMOS devices and circuits
- Technology R&D, DFY, DFT and IC Designs
- Foundry/Fabless Interface Strategies

Extended MOS-AK Committee:

- International MOS-AK Board of R&D Advisers
- Larry Nagel, Omega Enterprises Consulting (USA)
- Andrei Vladimirescu, UCB (USA); ISEP (FR)
- Technical Program Committee Chairs www.mos-ak.org//committee.html
- Pekka Ojala, Exar Corporation (USA)
- Gilson I Wirth, UFRGS (BR)
- Ehrenfried Seebacher, ams (A)
- Sadayuki Yoshitomi, Toshiba (J)

W05 Second International Workshop on Resiliency in Embedded Electronic Systems (REES 2017)

3C 0830 - 1700

Organisers: Wolfgang Müller, Universität Paderborn, DE
Daniel Müller-Gritschneder, Technische Universität München, DE
Subhasish Mitra, Stanford University, US

The REES workshop is a joint academic/industry forum considering multiple resiliency aspects from software to hardware and from embedded systems to chip level designs.REES 2017 features a range academic talks with poster presentations from internal research groups as well as exciting industrial presentations from ARM Limited, NXP, Bosch GmbH, Hewlett Packard Enterprise, ST Microelectronics, Infineon Technologies, and Mentor Graphics. More information is available at https://www.edacentrum.de/rees

0845 - 0900 **WELCOME Address**

0900 - 0930 **KEYNOTE Address**

0900 **Multi-Layer-Resilience: The Need for Discipline**
Speaker: Wolfgang Ecker, Infineon Technologies, DE

0930 - 1010 **Resilient Systems Designs I**

0930 **Introducing Fault Tolerance to the Regularity-Based Resource Partition Model**
Authors: Darrell Knape, Albert M. K. Cheng and Yu Li, University of Houston, Texas, US

0940 **Architecting Resilient IoT Systems**
Authors: Kemal A. Delic and David M. Penkler, Hewlett Packard Enterprise, FR

0950 **Utilization of Memristor Variability Towards Brain-Inspired Resilient Computing**
Authors: Rawan Naous[1] and Khaled Nabil Salama[2]
[1]King Abdullah University of Science and Technology, SA; [2]KAUST, SA

1000 **flexMEDiC: flexible Memory Error Detection by Combined Data Encoding and Duplication**
Authors: Norman A. Rink[1] and Jeronimo Castrillon[2]
[1]Technische Universität Dresden, DE; [2]TU Dresden, Germany, DE

1010 - 1045 **Poster Discussions (Session I) & Refreshments**

1045 - 1145 **Invited Industrial Talks - Resilient Systems in Practise**

1045 **Novel ISO26262 Compliant Architecture for Advanced Driver Assistance Systems**
Speaker: Luc van Dijk, NXP Semiconductors, NL

1115 **Design-for-Resiliency in Dynamically Power Managed Systems**
Speaker: Liangzehn Lai, ARM Ltd., GB

1145 - 1145 **Resilient Systems Design II**

1145 **Correction of Transient Faults by Rollback with Low Overhead for Microcontrollers**
Authors: Felix Mühlbauer[1] and Mario Schölzel[2]
[1]Universität Potsdam, DE; [2]IHP Frankfurt Oder, DE

1155 **Prototyping Resilient Processing Cores in Workcraft**
Authors: Georgy Lukyanov[1], Alessandro de Gennaro[2], Andrey Mokhov[3], Paulius Stankaitis[2] and Maxim Rykunov[4]
[1]Southern Federal University, Rostov-on-Don, RU; [2]Newcastle University, GB; [3]Newcastle upon Tyne U, GB; [4]imec, BE

1205 **Increasing the Robustness of Digital Circuits with Ring Oscillator Clocks**
Authors: Lucas Machado[1], Jordi Cortadella[2] and Antoni Roca Perez[1]
[1]Universitat Politècnica de Catalunya, ES; [2]Universitat Politecnica de Catalunya, ES

1315 - 1415 **Invited Industrial Talks - Resilient Design Tools and Methods**

1315 **Simultaneous Measurement of Defect Coverage and Tolerance in AMS ICs for ISO26262**
Speaker: Stephen Sunter, Mentor Graphics, CA

1345 **Error Effect Simulation for Automotive using SystemC Virtual Prototypes**
Speaker: Andreas Mauderer, Robert Bosch GmbH, DE

1415 - 1455 **Fault Injection Automation**

1415 **An Automatic Injection Framework for Safety Assessements of Embedded Software Binaries**
Authors: Peer Adelt[1], Bastian Koppelmann[2], Bernd Kleinjohann[1] and Christoph Scheytt[2]
[1]C-LAB, DE; [2]Heinz Nixdorf Institute, DE

1425 **Revisiting Symbolic Software-implemented Fault Injection**
Authors: Hoang Minh Le[1], Vladimir Herdt[1], Daniel Grosse[2] and Rolf Drechsler[3]
[1]Universität Bremen, DE; [2]University of Bremen, DE; [3]University of Bremen/DFKI, DE

1435 **Constraining Graph-based Test Case Generation by Fitness Landscaping**
Authors: Stefan Mueller[1], Jo Laufenberg[1], Joachim Gerlach[2], Thomas Kropf[1] and Oliver Bringmann[3]
[1]University of Tuebingen, DE; [2]Hochschule Albstadt-Sigmaringen, DE; [3]Universität Tübingen, DE

1455 **Closing the Gap Between FMEDA, FTA and Simulation Based Fault Injection at System Level**
Authors: Adam Himmelsbach[1], Sebastian Reiter[1], Alexander Viehl[2], Oliver Bringmann[3] and Wolfgang Rosenstiel[4]
[1]FZI, DE; [2]FZI Forschungszentrum Informatik, DE; [3]Universität Tübingen, DE; [4]University of Tübingen, DE

1455 - 1530 **Poster Discussions (Session III+V) & Refreshments**

1530 - 1610 **Resilient Circuit Analysis**

1530 **Fault Injection Campaigns in Multi-Domain Virtual Prototypes**
Authors: Raghavendra Koppak[1], Oliver Bringmann[2] and Andreas von Schwerin[3]
[1]University of Tübingen / Siemens AG, DE; [2]Universität Tübingen, DE; [3]Siemens AG, DE

1540 **Workload Dependent Aged Circuit Reliability Analysis**
Authors: Ajith Sivadasan[1], Armelle Notin[1], Vincent Huard[2], Etienne Maurin[3], Florian Cacho[2] and Lorena Anghel[4]
[1]ST Microelectronics, FR; [2]STMicroelectronics, FR; [3]St Microelectronics, FR; [4]TIMA Laboratory, FR

1550 **SPICE-Level Fault Injection with Likelihood Weighted Random Sampling - A Case Study**
Authors: Liang Wu[1], Saed Abughannam[1], Wolfgang Müller[2], Christoph Scheytt[1] and Wolfgang Ecker[3]
[1]Heinz Nixdorf Institute, DE; [2]Universität Paderborn, DE; [3]Infineon Technologies, DE

1600 **Resilient Large-Scale Physical Design**
Authors: Roman Bazylevych[1] and Lubov Bazylevych[2]
[1]Lviv Polytechnic National University, UA; [2]Institute of Applied Problems of Mechanics and Mathematics NASU, UA

1610 - 1645 **Poster Discussions (Session VI)**

1645 - 1700 **CLOSING**

W06 The 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)

4A 0830 - 1730

General Chairs: Jiang Xu, Hong Kong University of Science and Technology, CN
Sébastien Le Beux, Lyon Institute of Nanotechnology, FR
Programme Chair: Mahdi Nikdast, Polytechnique Montréal/McGill University, CA
Programme Committee Members: Akihiko Shinya, NTT Basic Research Lab., JP
Alan Mickelson, University of Colorado Boulder, US
Ayse Coskun, Boston University, US
Daniel Chillet, INRIA, FR
Davide Bertozzi, University of Ferrara, IT
Fabiano Hessel, PUCRS, BR
Ian O'Connor, Ecole Centrale de Lyon, FR
Isabella Cerutti, Scuola Superiore Sant'Anna, IT
John Ferguson, Mentor Graphics Corporation, US
Nikos Hardavellas, Northwestern University, US
Olivier Sentieys, INRIA - University of Rennes 1, FR
Sandro Bartolini, University of Siena, IT
Sebastien Rumley, University of Columbia, US
Yaoyao Ye, Shanghai Jiao Tong University, CN
Yvain Thonnart, CEA LETI, MINATEC, FR

Scope of the Workshop

Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering an alternative interconnect technology to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to address the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices and circuits are necessary to construct photonic interconnect networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects. OPTICS aims at discussing the most recent advances in photonic interconnects and silicon photonics for computing systems. Industry's and academia's views on the feasibility and recent progress of optical interconnects and silicon photonics will be discussed. The workshop is comprised of invited talks of the highest caliber in addition to refereed poster presentations.Topics to be discussed in the workshop include (but are not limited to) the following:Design Methodologies, Modeling and Tools: design space exploration, optimization, thermal-aware design, floor-planning, system level modeling and simulation, etc.Architectures/Micro-Architectures: hybrid optical-electronic interconnects, passive/active optical switched networks, communication protocols, etc.Applications: high-performance computing, photonics interconnects for memory, many-core systems, and datacenters, etc. Silicon Photonics Devices and Circuits: circuit demonstrators, on-chip lasers, photodetectors, electro-optic modulators, optical/photonic switches and routers, athermal devices, high-bandwidth I/O, packaging, etc.Paper SubmissionYou are invited to participate and submit your contributions to OPTICS. Please refer to the workshop webpage for more information (http://www.ece.ust.hk/~eexu/OPTICS.html).

0830 - 0835 **Introduction to OPTICS Workshop**
Chair: Jiang Xu, Hong Kong University of Science and Technology, CN
Co-Chair: Mahdi Nikdast, Polytechnique Montréal/McGill University, CA

0835 - 1030 **Morning Session I: What is New on the Technology Side?**
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR

0835 Electro-Optical Integration Technology for High-Bandwidth Optical Interconnects
Speaker: Bert Jan Offrein, IBM Zurich Research Lab., CH

0905 On the Way to Photonic Interposers, Building Blocks for Short-Distance Optical Communication
Speaker: Yvain Thonnart, CEA LETI, MINATEC, FR

0925 Germanium Receivers for Low Power Consumption Photonic Circuits
Speaker: Laurent Vivien, CNRS, FR

0945 Opportunities and Obstacles of Monolithic III-V Integration on Silicon
Speaker: Yoan Leger, CNRS – FOTON, FR

1005 Short Presentations of Accepted Poster Papers

1030 - 1100 **Coffee Break and Poster Session**

1100 - 1200 **Morning Session II: Applications of Silicon Photonics**
Chair: Mahdi Nikdast, Polytechnique Montréal/McGill University, CA

1100 Applications of CMOS-Compatible Integrated Photonics Beyond Interconnect and Telecom
Speaker: Xavier Rottenberg, IMEC, BE

1120 Optics in Data Center Disaggregation
Speaker: Alan Mickelson, University of Colorado Boulder, US

1140 An Optical Parallel Adder Towards Light Speed Data Processing
Speaker: Tohru Ishihara, Kyoto University, JP

1200 - 1300 **Lunch Break and Poster Session**

1300 - 1430 **Afternoon Session I: Opportunities and Challenges!**
Chair: Jiang Xu, Hong Kong University of Science and Technology, CN

1300 Scaling Up Silicon Photonic Circuits: Where Are the Challenges?
Speaker: Wim Bogaerts, Ghent University-IMEC, BE

1330 Impact of Planar Photonic Switch Architecture on Worse-Case Power Penalty
Speaker: Sebastien Rumley, University of Columbia, US

1350 Towards Accurate Silicon Photonics Platform Qualification for Static and Dynamic Purposes
Speaker: Jean-Francois Carpentier, STMicroelectronics, FR

1410 Temperature Sensitivity Analysis and Power Consumption Optimization of Optical Networks-on-Chip
Speaker: Yaoyao Ye, Shanghai Jiao Tong University, CN

1430 - 1500 **Coffee Break and Poster Session**

1500 - 1640 **Afternoon Session II: Design Automation and Methodologies!**
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR

1500 Towards Electronic-Photonic Design Automation for Optical Interconnect Networks
Speaker: Sergei F. Mingaleev, VPIphotonics, BY

1520 TBD
Speaker: Marcel van der Vliet, PhoeniX, NL

1540 From Circuit-Level to Component-Level Simulation and Back - PDK Driven Design Automation
Speaker: Jonas Flueckiger, Lumerical, CA

1600 Design Automation Beyond its Electronic Roots: Toward a Synthesis Methodology for Wavelength-Routed Optical Networks-on-Chip
Speaker: Davide Bertozzi, University of Ferrara, IT

1620 Silicon Photonics Scalable Design Framework: From Design Concept to Physical Verification
Speaker: Sarhan Hossam, Mentor Graphics, FR

1640 - 1720 **Panel Discussion**
Moderator: Jiang Xu, Hong Kong University of Science and Technology, CN

Panelists:
Wim Bogaerts, Ghent University-IMEC, BE
Jean-Francois Carpentier, STMicroelectronics, FR
Sergei F. Mingaleev, VPIphotonics, BY
Bert Jan Offrein, IBM Zurich Research Lab., CH
Laurent Vivien, CNRS, FR
Marcel van der Vliet, PhoeniX, NL

1720 - 1730 **Concluding Remarks and Closing Session**
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR
Co-Chairs: Jiang Xu, Hong Kong University of Science and Technology, CN
Mahdi Nikdast, Polytechnique Montréal/McGill University, CA

1930 - 2200 **OPTICS Networking Event (Dinner)**
Please check the OPTICS website (http://www.ece.ust.hk/~eexu/OPTICS.html) for more information. Send an email to mahdi.nikdast@mcgill.ca to register for the networking event.

W07 New Platforms for Future Cars: Safety and Security Challenges

3A 0830 - 1640

Organiser: Selma Saidi, Hamburg University of Technology, DE

The automotive industry is rapidly moving towards the adoption of new hardware solutions, such as multi- and many-core processors, in order to comply with the increasingly number of ECUs and the high computational power required by future autonomous cars and advanced vision processing. The automotive industry has focused for many years on safety to gain expertise and maturity in building robust and safe cars. Today, with the emerging trends in the automotive domain such as autonomous driving, V2X communication and Internet of Cars, security is also arising as a major concern for many automotive players. Therefore, new architecture solutions pose numerous challenges besides the burden of migrating legacy code. This involves data fusion and processing of a multitude of sensors piling into autonomous cars, mapping affecting processing power demands in new systems architectures, the verification and validation of timing safety and providing secure interfaces to connect the cars to each other and to the outside world. The purpose of this workshop is to present some of the current topics in the field of automotive and secure systems and to bring a detailed and technical discussion about the research challenges that can be tackled in that area by the DATE community, both at the software and the hardware level.The workshop will include only invited talks, with speakers from industry, namely Infineon, Bosch, Daimler, Chrona, NXP, Kalray and ESCRYPT, and distinguished speakers from academia with a long experience in the field. The workshop will be organized in the form of 3 main sessions:Session 1 presents a panel of existing new hardware solutions considered by the automotive domain.Session 2 presents the scientific problems related to the use of these new platforms and some of the proposed approaches to solve them.Session 3 is dedicated to cyber security aspects in future cars.

0830 - 0840 **Welcome and Opening**
Organiser: Selma Saidi, Hamburg University of Technology, DE

0840 - 1010 **Session 1: New Hardware Solution for Future Cars**
Chair: Muhammad Shafique, Vienna University of Technology (TU Wien), AT

0840 Engineering Dependable Platforms for Automated Driving
Speaker: Simon Burton, Robert Bosch GmbH, DE

0910 Why Multi-Core Microcontroller Architectures like AURIX will be ubiquitous in Autonomous Cars
Speaker: Albrecht Mayer, Infineon Technologies AG, DE

0940 Consolidating High-Performance and High-Integrity Autonomous Driving Functions on the MPPA Manycore Processor
Speaker: Benoît Dupont de Dinechin, Kalray S.A., FR

1010 - 1030 **Coffee break**

1030 - 1215 **Session 2: Predictability and Efficiency in Multicore Architectures**
Chair: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1030 Efficient Usage of Many-core Heterogeneous Processor Architectures in Critical Real-time Embedded Systems
Speaker: Eduardo Quinones, Barcelona Supercomputing Center, ES

1100 A Scalable Approach For Parallelizing Legacy Embedded Control Software
Speakers: Hermann von Hasseln[1] and Stefan Resmerita[2]
[1]Daimler AG, DE; [2]University of Salzburg/Chrona GmbH, AT, AT

1145 LET Based Communication for Heterogeneous Workloads in Multicore Systems
Speaker: Rolf Ernst, TU Braunschweig, DE

1215 - 1330 **Lunch break**

1330 - 1500 **Session3: Embedded Security in Cars**
Chair: Rolf Ernst, TU Braunschweig, DE

1330 Trends in Automotive Security
Speaker: Andre Osterhues, ESCRYPT GmbH., DE

1400 Securing the Connected Car
Speaker: Timo van Roermund, NXP Semiconductors, Hamburg, DE

1430 Automotive Microcontrollers - its not just all about safety and security.
Speaker: Glenn Farrall, Infineon Technologies AG, Bristol,, GB

1500 - 1530 **Coffee break**

1530 - 1630 **Panel Discussion**

1530 **Panel1: The Role of Hardware Design in Safety and Security**

1600 **Panel2: Automotive IoT: The Challenge of Communication and Software Integration**

1630 - 1640 **Closing Session**

W08 Engineering Multi-Scale Systems for Health, Energy and the Environment

5ABC 0830 - 1730

Organisers: Martin Rajman, EPFL, CH
Patrick Mayor, nano-tera.ch, CH

The main objective of this workshop is to provide an expert overview of the main scientific achievements produced in the framework of Nano-Tera.ch, a Swiss national program supporting research in multi-scale system engineering for health, security, energy and the environment.The broad objectives of the program are to improve quality of life and security of people and to create innovative products, technologies and manufacturing methods, thus resulting in job and revenue creation.Launched in 2008, Nano-Tera.ch is one of the larg-

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est federal programs funding research in engineering sciences. The research funded resulted in more than 1000 peer-reviewed publications and numerous prototypes and demonstrators, a tangible sign that the program focuses on concrete collaborative research leading to potentially exploitable results.The research carried out in the program explores various key thematic areas. Smart prosthetics and body repair covers topics ranging from image-guided micro surgery for hearing aid implantation, to tactile prosthetics as well as spinal cord neuroprosthesis for restoration of locomotion. Health monitoring addresses the use of smart textiles for monitoring long-term obesity, smart bandages, newborn care, and personalized therapeutic drug monitoring. Innovative medical platforms include flexible MRI detectors, cancer diagnostic using cantilever sensors, or high-performance portable 3D ultrasound platforms, among others. In addition to these health-related challenges, Nano-Tera.ch also tackles important issues in environmental monitoring, with technologies such as distributed sensor networks for air quality monitoring or natural hazard detection, multi-color lasers analyzing greenhouse gases or aquatic robots tracking water pollutants. Finally, Nano-Tera.ch has been focusing on the crucial theme of smart energy, with projects addressing ultra-high performance photovoltaic cells, economically viable renewable energy production through solar-hydrogen generators, or smart power grid monitoring and management.

0900 - 1300 **Nano-Tera.ch Final Event: morning session**

0900 Welcome

0910 Engineering Multi-Scale Systems for Health, Energy and the Environment
Speaker: Giovanni De Micheli, EPFL, CH

1000 Keynote speech: "The virtual personal health coach: Tools for prevention through behavior change and for management of chronic disease"
Speaker: Chris Van Hoof, IMEC, BE

1100 **Coffee break**

1130 Thematic Nano-Tera presentation: Health Monitoring
Speaker: Bradley Nelson, ETHZ, CH

1200 Thematic Nano-Tera presentation: Smart Prosthetics and Body Repair
Speaker: Stefan Weber, Uni Bern, CH

1230 Short PhD students presentations (part 1)

1300 **Lunch & Exhibition**

1400 - 1730 **Nano-Tera.ch Final Event: afternoon session**

1400 Keynote speech: "The bio-inspired artificial pancreas for treatment of diabetes"
Speaker: Pantelis Georgious, Imperial College London, GB

1500 Thematic Nano-Tera presentation: Medical Platforms
Speaker: Luca Benini, ETHZ, CH

1530 **Coffee break**

1600 Thematic Nano-Tera presentation: Environmental Monitoring
Speaker: Alcherio Martinoli, EPFL, CH

1630 Thematic Nano-Tera presentation: Smart Energy
Speaker: Christophe Moser, EPFL, CH

1700 Short PhD students presentations (part 2)

EXHIBITION THEATRE SESSIONS

Exhibition Theatre (2A) 1000 - 1700

Organisers: Jürgen Haase, edacentrum GmbH, DE
Marisa Lopez-Vallejo, UPM, ES

Exhibition Theatre 2017 feat. Internet of Things and Smart Devices, High Performance Computing and a Special Student´s Programme

In addition to the conference programme during DATE 17, there will be a presentation theatre as part of the exhibition from Tuesday 28 March to Thursday 30 March 2017. Attendees will profit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located in Room 1A close to the exhibition hall as well as to the rooms of the technical conference programme, thus affording easy access for exhibition visitors as well as for conference delegates.

The sessions of DATE 2017 Exhibition Theatre are open to conference delegates as well as to exhibition visitors.

Internet of Things and Smart Devices

The eleven Exhibition Theatre sessions will highlight technical presentations and panel discussions from leading companies, research projects and networks represented in the DATE 2017 Exhibition. A special emphasis will be on Internet of Things Applications, including Smart Medical Devices, Smart Energy and Self-Powered Devices, Smart Wearable Sensors. Special attention will also be given to security aspects in the upcoming internet of insecure things. Newest research results, technologies and solutions for cloud computing and for high performance computing also will be highlighted by DATE 2017 Exhibition Theatre programme and by DATE 2017 Exhibition.

Special Student's Programme

DATE 2017 for the first time will offer in the Exhibition Theatre a programme dedicated especially to students. It will include technical presentations from local industry, market leaders in EDA, semiconductors and application industries, a panel discussion and as special highlight a CV fair.

Please see presented below information on the Exhibition Theatre sessions. Extensions of this programme, list of contributing companies and institutes and further details of the exhibition sessions will be published on the DATE web portal and complemented regularly. Before your DATE attendance, please visit the web portal for an update.

EXHIBITION THEATRE SESSIONS Room 2A

2.8a	Smart Medical Devices	TUE 1130 - 1230
2.8b	Smart Medical Devices, Part 2	TUE 1230 - 1300
3.8	Addressing Challenges in Today's Datacenter Systems' Design	TUE 1430 - 1600
4.8	CV Fair DATE 2017	TUE 1700 - 1830
6.8	HiPEAC: European Network on High Performance and Embedded Architecture and Compilation	WED 1100 - 1230
7.8	Smart Energy and Self-Powered Devices	WED 1430 - 1530
8.8	Panel: Technology startups. Vision from Academia and Industry	WED 1700 - 1830
9.8	The Internet of INSECURE Things	THU 0830 - 1000
10.8a	Smart and Wearable Sensors for Health	THU 1100 - 1200
10.8b	IoT Edge Devices	THU 1200 - 1230
11.8	Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs	THU 1400 - 1530
12.8	Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology	THU 1600 - 1730

EXHIBITION THEATRE SESSIONS

2.8a Smart Medical Devices, Part 1

Exhibition Theatre 1130 - 1230

Organiser: Patrick Mayor, EPFL, CH

The goal of this session is to present concrete examples of smart medical devices, such as a novel surgical robot for hearing implant surgery, a measurement module for the identification of cancer cells through elastic properties, as well as a sensing pad for non-invasive wound monitoring.

2.8b Smart Medical Devices, Part 2

Exhibition Theatre 1230 - 1300

Organiser: John Zhao, MathWorks, US

1230 **Matlab and Simulink in the Smart Devices and Big Data Era**

Speaker: Stefano Olivieri, MathWorks Academia Group, US

Smart connected devices and Internet of Things (IoT) are emerging technologies that are impacting diverse industries, including automotive, energy, healthcare, retail, smart manufacturing, smart buildings and homes, smart transportation, etc. Combining internet-connected devices with cloud computing, machine learning, and other data analytics approaches is enabling products and solutions that are transforming the way we live and work. For example, Smart Medical Devices are key components of new products and solutions that may help healthcare professionals to improve health outcomes from anywhere, leading to increased value for the patient.

However, a system developer working on such products and services faces challenges in capturing, storing, and analyzing the Big Data generated from a multitude of devices. Also, integrating Smart Devices, IoT and Big Data raises specific challenges for data acquisition, reduction, and transmission, using increasingly sophisticated technologies such as RFID tags, Wireless Sensor Nodes and mobile devices.

Using the development of a Smart Medical Device based healthcare application as an example, this presentation will discuss how engineers and scientists creating smart devices and IoT systems can use MATLAB and Simulink to access and analyze huge data sets from devices, sensors, and databases; apply deep learning and other machine-learning techniques to develop predictive models; and design and test smart devices that wirelessly interact with cloud services like ThingSpeak™, an analytic IoT platform that can run MATLAB code on demand in the cloud.

3.8 Addressing Challenges in Today's Datacenter Systems' Design

Exhibition Theatre 1430 - 1600

Organiser: Ousmane Diallo, EPFL, CH

1430 **Server Benchmarking and Design with Cloudsuite 3.0**

Speaker: Javier Picorel, EPFL, CH

Since its inception, CloudSuite (cloudsuite.ch) has emerged as a popular suite of benchmarks both in industry and among academics for the performance evaluation of cloud services. The EuroCloud Server project blueprinted key optimizations in server SoCs based on the salient features of CloudSuite benchmarks that lead to an order of magnitude improvement in efficiency while preserving QoS. ARM-based server products (e.g., Cavium ThunderX) have now emerged following these guidelines and showcasing the improved efficiency. CloudSuite 3.0 is a major enhancement over prior releases both in benchmarks and infrastructure. It includes benchmarks that represent massive data manipulation with tight latency constraints such as in-memory data analytics using Apache Spark, a new real-time video streaming benchmark following today's most popular video-sharing website setups, and a new web serving benchmark mirroring today's multi-tier web server software stacks. To ease the deployment of CloudSuite into private and public cloud systems, the benchmarks are integrated into the Docker software container system and Google's PerfKit Benchmarker. Dock-

er wraps each benchmark into a self-contained software package, guaranteeing the same execution regardless of the environment, while PerfKit automates the process of benchmarking cloud server systems with CloudSuite. CloudSuite 3.0 is supported to run both on real hardware and on our QEMU-based computer architecture simulation framework.

1515 **Protecting Data in Farm and RDMA Networks with Catapult**

Speaker: Greg O'Shea, Microsoft, US

FaRM is an in-memory, transactional database that runs distributed across a cluster of Windows Servers that are connected by a high-speed Remote Direct Memory Access (RDMA) network. Data in FaRM are stored in DRAM and exposed directly to the L2 network by the server's RDMA network adapters, so that other members of the FaRM cluster can access the data with great efficiency. RDMA enables a network adapter to directly access the memory of another server in the same Ethernet network bypassing the operating system in both servers. This enables low-latency and high-bandwidth data access across the entire cluster. However, RDMA provides no security: the data are also accessible to every other server attached to the same Ethernet network, and message transfers are vulnerable to replay and modification. We present our work to protect data in FaRM using a bump-in-the-wire firewall for RDMA. Based upon the FPGA cards widely deployed in Windows Servers within Microsoft, the firewall exists as a barrier between a FaRM server's RDMA adapter and the local Ethernet switch. It prevents packets from outside the FaRM cluster from ever reaching the server's RDMA adapter, and it protects RDMA packets between members of the FaRM cluster by encapsulating them in DTLS tunnels. We show that implementing a similar level of protection in software can be prohibitively expensive.

4.8 CV Fair DATE 2017

Exhibition Theatre 1700 - 1830

Organiser: Marisa Lopez-Vallejo, UPM, ES

The Curriculum Vitae (also known as a vita or CV) is the first point of contact between employee and employer. It must provide a concise overview of academic background and achievements. Furthermore, it usually should catch the attention of the readers, get them to take a closer look at you and ultimately invite you for an interview. Philippe Ory, Head of the EPFL Career Center, will open this CV Fair with a talk on the key issues that must be addressed when writing a CV.

Afterwards, organizations participating in the CV Fair will give a brief presentation with basic information about the company, potential positions or internships, what types of students are being sought, etc. The CV fair is designed to allow for students to engage in individual conversations with the company or organization team and ask specific questions that may have arisen during the presentation.

6.8 HiPEAC: European Network on High Performance and Embedded Architecture and Compilation

Exhibition Theatre 1100 - 1230

Organiser: Catherine Roderick, Barcelona Supercomputing Center, ES

This session will showcase the activities of this network of research expertise. HiPEAC members come from both industry and academia and, together, form a community of expertise in Europe which reinforces and strengthens R&D activities. We offer funding for industrial PhD internships and short-term collaborations between early-career researchers and other research centres, as well as annual Tech Transfer Awards and communications and recruitment services. Annual HiPEAC activities include a high-profile conference, a researcher summer school and two Computing Systems Weeks, which are networking and knowledge-exchange gatherings. We also produce a biennial technology roadmap, the HiPEAC Vision, which recommends future actions and priorities for the European computing systems community and is a key source of reference for the European Commission. In this session, after a brief introduction to HiPEAC, we highlight some of our members' innovative and groundbreaking research and development activities.

EXHIBITION THEATRE SESSIONS

1100 **Accelerated Data Centers for Cloud Computing: The Vineyard Platform**
Speaker: Dimitrios Soudris, National Technical Univ. of Athens and ICCS, GR

1115 **High-Performance Parallelisation of Real-Time Applications with the Upscale SDK**
Speaker: Luis Miguel Pinho, Polytechnic of Porto, PT

1130 **Power-Aware Software Mapping of Parallel Applications Onto Heterogeneous MPSOCS**
Speaker: Gereon Onnebrink, RWTH Aachen University, DE

1145 **Overview of MANGO: Exploring Manycore Architectures for Next-Generation HPC Systems**
Speaker: José Flich, Technical University of Valencia, ES

1200 **AEGLE: An Interplay of High Performance an Cloud Computing for Big Bio-Data Analytics Supporting Integrated Health-Care Services**
Speaker: Dimitrios Soudris, National Technical Univ. of Athens and ICCS, GR

1215 **Eyes of Things**
Speaker: Matteo Sorci, nVISO, CH

7.8 Smart Energy and Self-Powered Devices

Exhibition Theatre 1430 - 1530

Organiser: Patrick Mayor, EPFL, CH

The goal of this session is to present concrete examples of novel designs for next-generation energy-efficient computing architectures and real-time monitoring and management of smart grids, as well as robust low-power networks of acoustic detectors for natural hazard warning systems.

8.8 Panel: Technology startups. Vision from Academia and Industry

Exhibition Theatre 1700 - 1830

Organiser: Marisa Lopez-Vallejo, UPM, ES

Technology entrepreneurship implicates taking a technology idea and finding a high-potential commercial opportunity, gathering resources such as talent and capital, considering how to market the idea, and managing rapid growth. It is a very high-potential path with a chance of both high earnings and large direct impact. However, it is also a really difficult path, and only small number of people are successful.

Success in this kind of business requires strong technical skills, capacity to deal with high risk of failure, and extremely hard work. In this panel we will discuss which are the challenges, opportunities and risks of creating technology startups.

Participants:

- Paul Andres, Legal Consultant, CH
- Karim Kanoun, Mobile and Embedded Development Manager at Gait Up S.A., CH
- Paul Keenan, Director of the IT Development Center Lausanne at Credit Suisse S.A., CH
- Gian Paolo Perrucci, Mobility and Apps Solution Manager at Nestlé, CH
- Amin Shokrollahi, Founder and CEO of Kandou Bus, CH

9.8 The Internet of INSECURE Things

Exhibition Theatre 0830 - 1000

Organiser: Marcello Coppola, STMicroelectronics, FR

Today everything from the door locks, a heating system or vehicle can be connected to internet opening the endless possibilities of future innovative technologies. As more low-power and internet-connected gadgets and sensors are integrated to our lives, an increase in demand for developing secure and trustworthy IoT-based systems is becoming the key element to make winning products.

Although, there has been a steady increase in improving the security, still proper authentication and encrypted communications are not common; making the overall Internet as a network of insecure things. This session proposes a journey through several speeches to show the advances in technologies that master the security aspects of IoT.

The session starts with an in-depth overview of security challenges and the trends in the IoT ecosystem against cyber-threats. Then, introduces the STM32 and the secure IoT platforms based on STM32 called SECube. Finally, the session provides some real use cases for smart vehicle, where IoT have a big impact on the type of applications and services that can be deployed using the association between vehicle and the homes of their owners. Last but not least, all the pre-registered attendees are eligible to get one of IoT platforms presented by the speakers via the www.secube.eu web site.

0830 **Setting the Stage**
Speaker: Marcello Coppola, STMicroelectronics, FR

0835 **Challenges for Secure IoT**
Speaker: Paolo Prinetto, Politecnico di Torino, IT

0850 **Mitigating the Risks in IoT with an Effective Security Offer**
Speaker: Michele Scarlatella, STMicroelectronics, FR

0905 **University Experiences Using a Secure IoT Platform Based on STM32**
Speaker: George Kornarors, Univ. of Applied Sciences of Crete, GR

0920 **SECUBE™: The Secure Commercial IoZ Platform**
Speaker: Antonio Varriale, Blu5 Labs Ltd, MT

0940 **Secure Communication in Automotive**
Speaker: Giovanni Gherardi, Energica Motor Company, IT

10.8a Smart and Wearable Sensors for Health

Exhibition Theatre 1100 - 1200

Organiser: Patrick Mayor, EPFL, CH

The goal of this session is to present three concrete examples of innovative wearable devices: a contactless monitoring system using dedicated imaging to accurately measure heart and respiratory rates of neonates, wearable devices integrated in smart textiles for the long-term monitoring of obese patients, as well as a miniature sensor for non-invasive restoration of tactile sensations.

10.8b IoT Edge Devices

Exhibition Theatre 1200 - 1230

1200 **Mentor's Custom/Analog Solutions for IoT Edge Devices**
Speaker: Jeff Miller, Mentor Graphics, US

11.8

Hot Topic Session: Biologically-inspired techniques for smart, secure and low power SoCs

Exhibition Theatre 1400 - 1530

Organisers: Andy M. Tyrrell, University of York, GB
Lukas Sekanina, Brno University of Technology, CZ

Chair: Andy M. Tyrrell, University of York, GB

Co-Chair: Lukas Sekanina, Brno University of Technology, CZ

While advanced well-tuned techniques are employed in current integrated circuits to increase the lifetime of cyber-physical, IoT and other systems, major concerns and important product differentiators such as power, security and variability continue to be major design factors. For many applications a sacrifice of performance or accuracy is acceptable in exchange for extremely low power consumption. However, even when this sacrifice is possible, other conflicting performance features must still be taken into account. Biologically-inspired techniques such as evolutionary algorithms and artificial neural networks have been used in the mainstream circuit design community infrequently. Recent years have witnessed a significant development and progress in these fields. The goal of this Special Session is to present latest research results from worldwide leading experts addressing state-of-the-art biologically-inspired techniques and devices that demonstrate the efficacy of such methods to designs focused on smart, low-power, and secure systems on chip.

1400 **An Evolutionary Approach to Runtime Variability Mapping and Mitigation on a Multi-Reconfigurable Architecture**

Speaker: Simon Bale, University of York, GB
Authors: Simon Bale, Pedro Campos, Martin Albrecht Trefzer, James Walker and Andy Tyrrell, University of York, GB

1418 **Towards Low Power Approximate DCT Architecture for HEVC Standard**

Speaker: Zdenek Vasicek, Brno University of Technology, CZ
Authors: Zdenek Vasicek, Vojtech Mrazek and Lukas Sekanina, Brno University of Technology, CZ

1436 **Semantic Driven Hierarchical Learning for Energy-Efficient Image Classification**

Speaker: Priyadarshini Panda, Purdue University, US
Authors: Priyadarshini Panda and Kaushik Roy, Purdue University, US

1454 **Machine Learning for Run-Time Energy Optimisation in Many-Core Systems**

Speaker: Geoff Merrett, University of Southampton, GB
Authors: Dwaipayan Biswas[1], Vibishna Balagopal[1], Rishad Shafik[2], Bashir Al-Hashimi[1] and Geoff Merrett[1]
[1]University of Southampton, GB; [2]Newcastle University, GB

1512 **An Evolutionary Approach to Hardware Encryption and Trojan-Horse Mitigation**

Speaker: Ernesto Sanchez, Politecnico di Torino, IT
Authors: Andrea Marcelli, Marco Restifo, Ernesto Sanchez and Giovanni Squillero, Politecnico di Torino, IT

12.8

Hot Topic Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap between Microfluidics and Microbiology

Exhibition Theatre 1600 - 1730

Organisers: Seetal Potluri, Technical University of Denmark, DK
Paul Pop, Technical University of Denmark, DK

Chair: Jan Madsen, Technical University of Denmark, DK

Co-Chair: Seetal Potluri, Technical University of Denmark, DK

Microfluidic biochips (also called lab-on-a-chip) are replacing the conventional biochemical analyzers by integrating all the necessary functions for biochemical analysis using microfluidics. The current trend is towards cyberphysical biochip platforms that integrate novel sensors and actuators, as well as on-chip control circuits. Motivated by the similarity to microelectronics, researchers have started to propose EDA tools for the synthesis of microfluidic biochips. However, we advocate for a paradigm shift, to bridge the formidable barrier that separates engineering (or chip design) from practical biochemistry and microbiology. The special session will serve as a "call to arms" for more focused and relevant research to increase the adoption of microfluidics in translational research.

1600 **Digital-Microfluidic Biochips for Quantitative Analysis: Bridging the Gap Between Microfluidics and Microbiology**

Speaker: Krishnendu Chakrabarty, Duke University, US
Authors: Mohamed Ibrahim and Krishnendu Chakrabarty, Duke University, US

1630 **The Case for Semi-Automated Design of MVLSI Biochips**

Speaker: Jeffrey McDaniel, University of California, Riverside, US
Authors: Jeffrey McDaniel, William H. Grover and Philip Brisk, University of California, Riverside, US

1700 **Synthesis of On-Chip Control Circuits for MVLSI Biochips**

Speaker: Seetal Potluri, Technical University of Denmark, DK
Authors: Seetal Potluri[1], Alexander Schneider[2], Martin Hørslev-Petersen[2], Paul Pop[2] and Jan Madsen[2]
[1]Xilinx Asia Pacific, SG; [2]Technical University of Denmark, DK

1715 **Scheduling and Optimization of Genetic Logic Circuits on Microfluidic Biochips**

Speaker: Tsung-Yi Ho, National Tsing Hua University, TW
Authors: Yu-Jhih Chen[1], Sumit Sharma[2], Sudip Roy[3] and Tsung-Yi Ho[1]
[1]National Tsing Hua University, TW; [2]Indian Institute of Technology Roorkee, IN; [3]IIT Roorkee, IN

UNIVERSITY BOOTH AT DATE 2017

The University Booth is organised during DATE and will be located in booth 1 of the exhibition area. All demonstrations will take place from Tuesday, March 28 to Thursday, March 30, 2017 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 39 demonstrations from 13 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Internet-of-Things Prototypes
- Wearable Electronics and Smart Medical Prototypes

The University Booth at DATE 2017 invites you to booth 1 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information is available online at
www.date-conference.com/exhibition/u-booth.
The following demonstrators will be presented at the University Booth.

A FRAMEWORK FOR VARIATION-AWARE ANALOG CIRCUITS SIZING

Presenter: Ons Lahiouel, Concordia University, CA
Authors: Mohamed H. Zaki and Sofiene Tahar, Concordia University, CA

Timeslots: UB10.1 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Today's analog design faces significant challenges due to circuit complexity and short time-to-market windows. The proposed demonstration presents new techniques for enhancing variation-aware circuits sizing. The sizing problem is encoded using nonlinear constraints. A new algorithm using Satisfiability Modulo Theory (SMT) solving techniques exhaustively explores the design space and computes a continuous set of feasible sizing solutions. Two methods for the computation of parametric yield are implemented. The first method combines the advantages of sparse regression and SMT solving techniques for reliable and accelerated yield estimation. The second approach employs a statistical classifier to reduce the number of simulations. An optimization process using a two-step exploration strategy is also integrated to find the feasible design point with the highest yield. Experimental results show that our approach locates higher quality of design point within less run time.

A TOOL FOR STATIC INSTRUCTION SET ARCHITECTURE ANALYSIS

Presenter: Peer Adelt, Paderborn University / C-LAB, DE
Authors: Bastian Koppelmann[1], Wolfgang Mueller[1], Bernd Kleinjohann[2] and Christoph Scheytt[1]
[1]Heinz-Nixdorf Institute, DE; [2]Paderborn University / C-LAB, DE

Timeslots: UB09.1 (Thursday, March 30, 2017 1000 - 1200)

Abstract: Mutation based testing, which is applied to assess testbenches by mutations of designs under test, is well established in the hardware and software domain. We demonstrate our tool, which analyses all 798 instructions of the TriCore™ microcontroller architecture for mutations of their binary representation. The tool provides an interactive graphical interface, which indicates general and detailed instruction set (ISA) specific statistics of 1-, 2- and 3-bitflip mutations in opcode, data and address sections of the instructions and their impact on the program execution. The ISA analysis tool is applied as a front-end for automatic mutation generations of TriCore™ binaries. In this context, we also show how the CPU emulator QEMU can be applied as a framework for mutation based analysis based on the static analysis of the TriCore™ ISA and the software binary.

A VOLTAGE-SCALABLE FULLY DIGITAL ON-CHIP MEMORY FOR ULTRA-LOW-POWER IOT PROCESSORS

Presenter: Jun Shiomi, Kyoto University, JP
Authors: Tohru Ishihara and Hidetoshi Onodera, Kyoto University, JP

Timeslots: UB01.5 (Tuesday, March 28, 2017 1030 - 1230)
UB02.5 (Tuesday, March 28, 2017 1230 - 1500)
UB03.5 (Tuesday, March 28, 2017 1500 - 1730)
UB04.5 (Tuesday, March 28, 2017 1730 - 1930)
UB11.5 (Thursday, March 30, 2017 1430 - 1630)

Abstract: A voltage-scalable RISC processor integrating standard-cell based memory (SCM) is demonstrated. Unlike conventional processors, the processor has Standard-Cell based Memories (SCMs) as an alternative to conventional SRAM macros, enabling it to operate at a 0.4 V single-supply voltage. The processor is implemented with the fully automated cell-based design, which leads to low design costs. By scaling the supply voltage and applying the back-gate biasing techniques, the power dissipation of the SCMs is less than 20 uW, enabling the SCMs to operate with ambient energy source only. In this demonstration, the SCMs of the processor operates with a lemon battery as the ambient energy source.

ACCELERATORS: RECONFIGURABLE SELF-TIMED DATAFLOW ACCELERATOR & FAST NETWORK ANALYSIS IN SILICON

Presenter: Alessandro de Gennaro, Newcastle University, GB
Authors: Danil Sokolov and Andrey Mokhov, Newcastle University, GB

Timeslots: UB02.7 (Tuesday, March 28, 2017 1230 - 1500)
UB03.7 (Tuesday, March 28, 2017 1500 - 1730)
UB04.7 (Tuesday, March 28, 2017 1730 - 1930)

Abstract: Many real-life applications require dynamically reconfigurable pipelines to handle incoming data items differently depending on their values or current operating mode. A demo will show the benefits of an asynchronous accelerator for ordinal pattern encoding with reconfigurable pipeline depth. This was designed, simulated and verified using dataflow structure formalism in Workcraft toolset. The self-timed chip, fabricated in TSMC 90nm, shows high resilience to voltage variation and configurable accuracy of the results. Applications with underlying graph models foster the importance of a fast and flexible approach to graph analysis. To support

medicine discovery biological systems are modelled by graphs, and drugs can disconnect some of the connections. A demo will show how graphs can be automatically converted into VHDL designs, which are synthesised into a FPGA for the analysis: thousand times faster than in software. Single stand will be used for both case studies.

AF3-MC: DEVELOPMENT OF MIXED CRITICALITY SYSTEMS USING MBSE

Presenter: Thomas Boehm, fortiss, DE
Authors: Johannes Eder and Sebastian Voss, fortiss, DE

Timeslots: UB09.4 (Thursday, March 30, 2017 1000 - 1200)
UB10.4 (Thursday, March 30, 2017 1200 - 1430)
UB11.4 (Thursday, March 30, 2017 1430 - 1630)

Abstract: AutoFOCUS3 (https://af3.fortiss.org/) is an open-source model-based development tool, including a number of different analysis- and verification tools as well as design space exploration functionality, task scheduling dependent on a number of system requirements (timing, resource, energy, etc.), and code generators targeting C-code or VHDL. The presented demonstrator illustrates both a SW tool demonstrator and a corresponding HW demonstrator setup to show how a seamless model-based system approach could look like, w.r.t. to mixed-critical applications integrated on a (COTS) MC-platform. A floating ball can be controlled by an person by moving his hand over an US sensor, providing input to the control loop implemented in the high criticality part of the system. The low criticality part of the system which is running on the same CPU consists of the computation of the digits of PI and of the Fibonacci sequence, providing computationally intensive neighbors to the control loop.

BRAIN TO COMPUTER CONNECTIONS: A FAST TIME-DOMAIN APPROACH FOR BCI TRAINING

Presenter: Giovanni Mezzina, Politecnico di Bari, Italy, IT
Authors: Valerio Francesco Annese and Daniela De Venuto, Politecnico di Bari, IT

Timeslots: UB06.6 (Wednesday, March 29, 2017 1200 - 1400)

Abstract: We present a P300-based Brain Computer Interface (BCI) approach for the brain control of external devices through an innovative approach. The herein proposed HW/SW system acquires the signal from 6 EEG channels and synchronizes them with ad-hoc designed visual stimuli that evocates the P300 signal. The BCI signal processing comprises: (i) a Machine Learning stage, which is based on an algorithm (t-RIDE), which calibrates the system in ~190s (ii) a smart approach for the time-domain features extraction greatly reduces the computational effort, speeding up the classification and finally (iii) the on-line classification, which is entrusted to a linear classifier. Noteworthy results obtained in experimental setup are: (i) P300 spatio-temporal characterization in 1.95s, (ii) classification accuracy of 80.5±4.1% on single-trial. (iii) real time classification in 22ms (WC). As a PoC, supporting videos will show how the BCI outcomes can pilot a prototype car.

COSSIM: A NOVEL, COMPREHENSIBLE, ULTRA-FAST, SECURITY-AWARE CPS SIMULATOR

Presenter: Nikolaos Tampouratzis, Technical University of Crete, GR
Authors: Antonios Nikitakis and Andreas Brokalakis, Synelixis Solutions Ltd, GR

Timeslots: UB07.1 (Wednesday, March 29, 2017 1400 - 1600)
UB08.1 (Wednesday, March 29, 2017 1600 - 1800)

Abstract: One of the main problems Cyber Physical Systems (CPS) and Highly Parallel Systems (HPS) designers face is the lack of simulation tools and models for system design and analysis. This is mainly because the majority of the existing simulation tools can handle efficiently only parts of a system (e.g. only the processing or only the network) while none of them supports the notion of security. Moreover, most of the existing simulators need extreme amounts of processing resources while faster approaches cannot provide the necessary precision and accuracy. COSSIM is an open-source framework that seamlessly simulates, in an integrated way, the networking and the processing parts of the CPS and Highly Parallel Heterogeneous Systems. In addition, COSSIM supports accurate power estimations while it is the first such tool supporting security as a feature of the design process. The complete COSSIM framework together with its sophisticated GUI will be presented.

DEMONSTRATION OF HW/SW CO-PROCESSING WITH FPGA FOR FAST VISUAL NAVIGATION OF ROVERS

Presenter: Konstantinos Maragos, National Technical University of Athens, GR
Authors: George Lentaris and Dimitrios Soudris, National Technical University of Athens, GR

Timeslots: UB01.3 (Tuesday, March 28, 2017 1030 - 1230)

Abstract: Autonomy, speed and accuracy constitute vital factors for the successful rover-exploration missions. However, the extremely low performance of the on-board space-grade CPUs in conjunction with the increased complexity of the sophisticated computer vision algorithms become a serious bottleneck for fast rover navigation. In this work, we present a HW/SW co-design solution based on FPGA to accelerate visual odometry algorithms tailored to the needs of future Mars exploration missions being scheduled by European Space Agency. For demonstration purposes, we use a Xilinx Kintex-7 FPGA to process images and perform feature detection, description, and matching. The FPGA communicates via ethernet port with the host CPU, which performs filtering and egomotion estimation with absolute orientation. We present the navigation path of a hypothetical moving rover which processes successively stereo images acquired by a hypothetical Martian surface while live-recording the CPU-FPGA co-processing.

EMU: RAPID FPGA PROTOTYPING OF NETWORK SERVICES IN C#

Presenter: Salvator Galea, University of Cambridge, GB
Authors: Nik Sultana[1], Pietro Bressana[2], David Greaves[1], Robert Soulé[2], Andrew W Moore[1] and Noa Zilberman[1]
[1]University of Cambridge, GB; [2]Università della Svizzera italiana, CH

Timeslots: UB09.7 (Thursday, March 30, 2017 1000 - 1200)
UB10.7 (Thursday, March 30, 2017 1200 - 1430)
UB11.7 (Thursday, March 30, 2017 1430 - 1630)

Abstract: General-purpose CPUs and OS abstractions impose overheads that make it challenging to implement network functions and services in software. On the other hand, programmable hardware such as FPGAs suffer from low-level programming models, which make the rapid development of network services cumbersome. We demonstrate Emu, a framework that makes use of an HLS tool (Kiwi) and enables the execution of high-level descriptions of network services, written in C#, on both x86 and Xilinx FPGA. Emu

therefore opens up new opportunities for improved performance and power usage, and enables developers to more easily write network services and functions. We demonstrate C# implementations of network functions, such as Memcached and DNS Server, using Emu running on both x86 and NetFPGA-SUME platform and show that they are competitive to natively written hardware counterparts while providing a superior development and debug environment.

FLEXPORT: FLEXIBLE PLATFORM FOR OBJECT RECOGNITION & TRACKING TO ENHANCE INDOOR LOCALIZATION AND MAPPING

Presenter: Marko Rößler, Technische Universität Chemnitz, DE
Authors: Christian Schott, Murali Padmanabha and Ulrich Heinkel, TU Chemnitz, DE

Timeslots: UB03.3 (Tuesday, March 28, 2017 1500 - 1730)
UB07.3 (Wednesday, March 29, 2017 1400 - 1600)
UB09.3 (Thursday, March 30, 2017 1000 - 1200)

Abstract: Object detection plays a crucial role in realizing intelligent indoor localization and mapping techniques. With the advantages of these techniques comes the complexity of computing hardware and the mobility. While the availability of open source computer vision algorithms and High-Level-Synthesis framework accelerates the development, the hybrid processing architecture of an All Programmable System on Chip (APSoC) enables efficient hardware-software partitioning. Using these tools, a generic platform was designed for evaluating the computer vision algorithms. Open source components such as Linux kernel and OpenCV libraries were integrated for evaluation of the algorithms on the software while Vivado HLS framework was used to synthesize the hardware counter parts. Algorithms such as Sobel filtering and Hough Line transformation were implemented and analyzed. The capabilities of this platform were used to realize a mobile object detection system for enhancing the localization techniques.

GNOCS: AN ULTRA-FAST, HIGHLY EXTENSIBLE, CYCLE-ACCURATE GPU-BASED PARALLEL NETWORK-ON-CHIP SIMULATOR

Presenter: Amir CHARIF, TIMA, FR
Authors: Nacer-Eddine Zergainoh and Michael Nicolaidis, TIMA, FR

Timeslots: UB04.6 (Tuesday, March 28, 2017 1730 - 1930)
UB07.6 (Wednesday, March 29, 2017 1400 - 1600)
UB08.6 (Wednesday, March 29, 2017 1600 - 1800)
UB11.6 (Thursday, March 30, 2017 1430 - 1630)

Abstract: With the continuous decrease in feature sizes and the recent emergence of 3D stacking, chips comprising thousands of nodes are becoming increasingly relevant, and state-of-the-art NoC simulators are unable to simulate such a high number of nodes in reasonable times. In this demo, we showcase GNoCS, the first detailed, modular and scalable parallel NoC simulator running fully on GPU (Graphics Processing Unit). Based on a unique design specifically tailored for GPU parallelism, GNoCS is able to achieve unprecedented speedups with no loss of accuracy. To enable quick and easy validation of novel ideas, the programming model was designed with high extensibility in mind. Currently, GNoCS accurately models a VC-based microarchitecture. It supports 2D and 3D mesh topologies with full or partial vertical connections. A variety of routing algorithms and synthetic traffic patterns, as well as dependency-driven trace-based simulation (Netrace), are implemented and will be demonstrated

GREENOPENHEVC: LOW POWER HEVC DECODER

Presenter: Menard Daniel, INSA Rennes, FR
Authors: Julien Heulot[1], Erwan Nogues[1], Maxime Pelcat[2] and Wassim Hamidouche[1]
[1]INSA Rennes, IETR, UBL, FR; [2]Institut Pascal, Université Clermont-Ferrand, FR

Timeslots: UB04.9 (Tuesday, March 28, 2017 1730 - 1930)
UB06.2 (Wednesday, March 29, 2017 1200 - 1400)

Abstract: Video on mobile devices is a must-have feature with the prominence of new services and applications using video like streaming or conferencing. The new video standard HEVC is an appealing technology for service providers. Besides, with the recent progress of SoC, software video decoders are now a reality. The challenge is to provide power efficient design to fit with the compelling demand for long battery. We present here a practical set-up demonstrating that the new HEVC standard can be implemented in software on an embedded GPP multicore platform. Different techniques have been integrated to optimize the energy: data-level and thread level parallelisms, video aware Dynamic Voltage and Frequency Scaling. To push back the limits, algorithm level approximate computing is carried-out on the in-loop filtering. The subjective tests have demonstrated that the quality degradation is almost imperceptible. A mean power of less than 1 Watt is reported for a HD 1080p/24fps video decoding.

HEPSYCODE: A SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF HETEROGENEOUS PARALLEL DEDICATED SYSTEMS

Presenter: Luigi Pomante, University of L'Aquila, IT
Authors: Giacomo Valente[1], Vittoriano Muttillo[1], Daniele Di Pompeo[1], Emilio Incerto[2] and Daniele Ciambrone[1]
[1]University of L'Aquila, IT; [2]Gran Sasso Science Institute, IT

Timeslots: UB08.9 (Wednesday, March 29, 2017 1600 - 1800)
UB09.9 (Thursday, March 30, 2017 1000 - 1200)
UB10.9 (Thursday, March 30, 2017 1200 - 1430)
UB11.9 (Thursday, March 30, 2017 1430 - 1630)

Abstract: Heterogeneous parallel systems have been recently exploited for a wide range of application domains, for both the dedicated (e.g. embedded) and the general purpose products. Such systems can include different processor cores, memories, dedicated ICs and a set of connections between them. They are so complex that the design methodology plays a major role in determining the success of the products. So, this demo addresses the problem of the electronic system-level hw/sw co-design of heterogeneous parallel dedicated systems. In particular, it shows an enhanced CSP/SystemC-based design space exploration step (and related ESL-EDA prototype tools), in the context of an existing hw/sw co-design flow that, given the system specification and related F/NF requirements, is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.

ITMD: RUN-TIME MANAGEMENT OF CONCURRENT MULIT-THREADED APPLICATIONS ON HETEROGENEOUS MULTI-CORES

Presenter: Karunakar Reddy Basireddy, University of Southampton, GB
Authors: Amit Singh, Bashir M. Al-Hashimi and Geoff V. Merrett, University of Southampton, GB

Timeslots: UB06.5 (Wednesday, March 29, 2017 1200 - 1400)
UB08.5 (Wednesday, March 29, 2017 1600 - 1800)

Abstract: Heterogeneous multi-cores often need to deal with multiple applications having different performance requirements concurrently, which generate varying and mixed workloads. Runtime management is required

for adapting to such performance requirements and workload variabilities, and to achieve energy efficiency. It is challenging to efficiently exploit different types of cores simultaneously and DVFS potential of cores. We present a run-time management approach that first selects thread-to-core mapping based on the performance requirements and resource availability. Then, it applies online adaptation by adjusting the voltage-frequency (V-f) levels to achieve energy optimization. We demonstrate the proposed run-time management approach on the Odroid-XU3, with various combinations of multi-threaded applications from PARSEC and SPLASH benchmarks. Results show an average improvement in energy efficiency up to 33% compared to existing approaches.

LABSMILING: A FRAMEWORK, COMPOSED OF A REMOTELY ACCESSIBLE TESTBED AND RELATED SW TOOLS, FOR ANALYSIS AND DESIGN OF LOW DATA-RATE WIRELESS PERSONAL AREA NETWORKS BASED ON IEEE 802.15.4

Presenter: Marco Santic, University of L'Aquila, IT
Authors: Luigi Pomante, Walter Tiberti, Carlo Centofanti and Lorenzo Di Giuseppe, DEWS - Università di L'Aquila, IT

Timeslots: UB02.10 (Tuesday, March 28, 2017 1230 - 1500)
UB05.10 (Wednesday, March 29, 2017 1000 - 1200)
UB06.10 (Wednesday, March 29, 2017 1200 - 1400)

Abstract: Low data-rate wireless personal area networks (LR-WPANs) are even more present in the fields of IoT, wearable devices and health monitoring. The development, deployment and test of such systems, based on IEEE 802.15.4 standard (and its derivations, e.g. 15.4e), require the exploitation of a testbed when the network is not trivial and grows in complexity. This demo shows the framework of LabSmiling: a testbed and related SW tools that connect a meaningful (but still scalable) number of physical devices (sensor nodes) located in a real environment. It offers the following services: program, reset, switch on/off single devices; connect to devices up/down links to inject or receive commands/msgs/packets in/from the network; set devices as low level packet sniffers, allowing to test/debug protocol compliances or extensions. Advanced services are: possibility of design test scenarios for the evaluation of network metrics (throughput, latencies, etc.) and custom application verification.

MARGOT: APPLICATION ADAPTATION THROUGH RUNTIME AUTOTUNING

Presenter: Gianluca Palermo, Politecnico di Milano, IT
Authors: Davide Gadioli, Emanuele Vitali and Cristina Silvano, Politecnico di Milano, IT

Timeslots: UB01.6 (Tuesday, March 28, 2017 1030 - 1230)
UB02.6 (Tuesday, March 28, 2017 1230 - 1500)
UB10.6 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Several classes of applications expose parameters that influence their extra-functional properties, such as the quality of the result or the performance. This leads the application designer to tune these parameters to find the configuration that produces the desired outcome. Given that the application requirements and the resources assigned to each application might vary at runtime, finding a one-fit-all configuration is not a trivial task. For this reason, we implemented the mARGOt framework that enhances an application with an adaptation layer in order to continuously tune the parameters according to the evolving situation. More in detail, mARGOt is composed of a monitoring infrastructure, an application-level adaptation engine and an extra-functional configuration framework based on the separation of concerns paradigm between functional and extra-functional aspects. At the booth, we plan to demonstrate the effectiveness of the proposed infrastructure on three real-life applications.

MATISSE: A TARGET-AWARE COMPILER TO TRANSLATE MATLAB INTO C AND OPENCL

Presenter: Luís Reis, University of Porto, PT
Authors: João Bispo and João Cardoso, University of Porto / INESC-TEC, PT

Timeslots: UB02.4 (Tuesday, March 28, 2017 1230 - 1500)
UB03.4 (Tuesday, March 28, 2017 1500 - 1730)
UB04.4 (Tuesday, March 28, 2017 1730 - 1930)
UB05.4 (Wednesday, March 29, 2017 1000 - 1200)

Abstract: Many engineering, scientific and finance algorithms are prototyped and validated in array languages, such as MATLAB, before being converted to other languages such as C for use in production. As such, there has been substantial effort to develop compilers to perform this translation automatically. Alternative types of computation devices, such as GPGPUs and FPGAs, are becoming increasingly more popular, so it becomes critical to develop compilers that target these architectures. We have adapted MATISSE, our MATLAB-compatible compiler framework, to generate C and OpenCL code for these platforms. In this demonstration, we will show how our compiler works and what its capabilities are. We will also describe the main challenges of efficient code generation from MATLAB and how to overcome them.

MTA: MANCHESTER THERMAL ANALYZER

Presenter: Scott Ladenheim, University of Manchester, GB
Authors: Yi-Chung Chen, Vasilis Pavlidis and Milan Mihajlović, University of Manchester, GB

Timeslots: UB01.8 (Tuesday, March 28, 2017 1030 - 1230)
UB05.8 (Wednesday, March 29, 2017 1000 - 1200)

Abstract: The Manchester Thermal Analyzer (MTA) is a fast thermal analysis tool to compute temperature profiles of integrated circuits (ICs) in 3-D. The thermal simulations use the finite element method to discretize the heat equation in space coupled to an implicit time-integration method and are implemented with the open-source C++ library deal.II. The MTA supports higher-order elements, several time-integration methods, and fully adaptive spatiotemporal refinement. State-of-the-art preconditioned iterative methods solve the linear systems arising from the discretized equations as efficiently as possible. Using shared memory parallelization, the MTA solves systems on the order of tens of millions enabling modeling ICs at the cell-level. We present a thermal simulation of an Intel Xeon processor within a FCLGA package with heatsink to show the diverse structures of modern ICs the MTA simulates. The MTA also models other 3-D structures such as bonded tiers, TSVs, heatsinks, and heat spreaders.

MULTI-CORE VERIFICATION: COMBINING MICROTESK AND SPIN FOR VERIFICATION OF MULTI-CORE MICROPROCESSORS

Presenter: Mikhail Chupilko, ISPRAS, RU
Authors: Alexander Kamkin, Mikhail Lebedev and Andrei Tatarnikov, ISPRAS, RU

Timeslots: UB01.4 (Tuesday, March 28, 2017 1030 - 1230)
UB05.6 (Wednesday, March 29, 2017 1000 - 1200)
UB09.5 (Thursday, March 30, 2017 1000 - 1200)

Abstract: The complexity of modern cache coherence protocols (CCP) in multi-core microprocessors prevents from complete verification of shared memory subsystems by means of random test-program generators (TPG). The following steps are suggested to target the problem. The first step is to separately specify CCP features and generate CCP-specific events to be used in TPG when generating a test program (TP). The protocol is specified in Promela, with Spin making a test template (TT). Spin also produces UVM (or C++TESK) testbench to make the execution of the resulting TPs to be controlable and deterministic. The second step is to let TPG produce the mem-

ory access instructions causing desired CCP-specific behavior. As a TPG we use MicroTESK. Its Ruby-based TTs abstractly describe future TPs. MicroTESK processes that TT making TP with CCP-specific events. The resulting TP is executed together with the testbench to exactly reproduce the situation Spin had found to be important for such a protocol.

NETFI-2: AN AUTOMATIC METHOD FOR FAULT INJECTION ON HDL-BASED DESIGNS

Presenter: Alexandre Coelho, Université Grenoble Alpe, FR
Authors: Miguel Solinas, Juan Fraire, Nacer-Eddine Zergainoh, Pablo Ferreyra and Raoul Velazco, TIMA, FR

Timeslots: UB08.2 (Wednesday, March 29, 2017 1600 - 1800)
UB11.2 (Thursday, March 30, 2017 1430 - 1630)

Abstract: Fault injection tools, which include fault simulation and emulation, are a well-known technique to evaluate the susceptibility of integrated circuits to the effects of radiation. This work presents a methodology to emulate Single Event Upsets (SEUs) and Single Event Transients (SETs) in a Field Programmable Gate Array (FPGA). The method proposed combines the flexibility of FPGA with the controllability provided by the MicroBlaze, to emulate HDL circuit and control the fault injection campaign. This approach has been integrated into a fault-injection platform, named NETFI (NETlist Fault Injection), developed by our research group, and received the name of NETFI-2. To validate this methodology fault injection campaign have been performed in Leon3 and Stochastic Bayesian Machine. Results on an Artix-7 FPGA show that NETFI-2 provides accurate measurements while improving the execution time of the experiment by more than 300% compared with analogous simulation-based campaigns.

NETWORKED LABS-ON-CHIPS

Presenter: Andreas Grimmer, Johannes Kepler University Linz, AT
Authors: Werner Haselmayr, Andreas Springer and Robert Wille, Johannes Kepler University Linz, AT

Timeslots: UB03.8 (Tuesday, March 28, 2017 1500 - 1730)
UB07.4 (Wednesday, March 29, 2017 1400 - 1600)

Abstract: Labs-on-Chip (LoC) allow for the miniaturization, integration, and automation of medical and bio-chemical procedures. In recent years, different technologies have been considered. However, all of them have their drawbacks, e.g. electrowetting-based LoCs suffer from the evaporation of liquids, the fast degradation of the surface coatings, and the inferior biocompatibility, while flow-based LoCs require a complex and costly multilayer fabrication process. Hence, an alternative has recently been proposed in terms of Networked Labs-on-Chips. We present and demonstrate the NLoC technology where so-called droplets flow inside channels of micrometer-size. Networking functionalities enable the designer to dynamically select the operations to be conducted. These networking functionalities exploit hydrodynamic forces acting on droplets. Moreover, NLoC devices can be produced at low cost (e.g. using 3D printers). By this, drawbacks of established LoC-technologies are addressed.

NNDNN: NEURAL NETWORKS DESIGNING NEURAL NETWORKS

Presenter: Brett Meyer, McGill University, US
Authors: Warren Gross, Sean Smithson, Ossama Ahmed and Guang Yang, McGill University, US

Timeslots: UB05.3 (Wednesday, March 29, 2017 1000 - 1200)

Abstract: Modern artificial neural networks currently achieve state-of-the-art results in various difficult problems, including image classification and speech recognition. However, both the performance and computational complexity of such models are heavily dependent on the design of charac-

teristic hyper-parameters (e.g., numbers of hidden layers or nodes per layer) which are often manually optimized. With neural networks penetrating low-power mobile and embedded areas, the need now arises to optimize not only for performance, but also for implementation cost. In our work, we present a multi-objective design space exploration method leveraging machine learning based response surface modelling to reduce the number of solutions trained and evaluated. Experimental results are presented for several image recognition datasets, demonstrating the evolution of the approximated Pareto-optimal hyper-parameters and corresponding GPU code; all while exploring only a small fraction of the design space.

NOXIM-XT: A BIT-ACCURATE POWER ESTIMATION SIMULATOR FOR NOCS

Presenter: Pierre Bomel, Université de Bretagne Sud, FR
Authors: André Rossi[1], Johann Laurent[2] and Erwan Moreac[2]
[1]LERIA, Université d'Angers, Angers, France, FR; [2]Lab-STICC, Université de Bretagne Sud, Lorient, FR

Timeslots: UB01.1 (Tuesday, March 28, 2017 1030 - 1230)
UB04.1 (Tuesday, March 28, 2017 1730 - 1930)
UB05.1 (Wednesday, March 29, 2017 1000 - 1200)
UB06.1 (Wednesday, March 29, 2017 1200 - 1400)

Abstract: We have developped an enhanced version of Noxim (Noxim-XT) to estimate the energy consumption of a NoC in a SOC. Noxim-XT is used in a two-step methodology. First, applications are mapped on a SoC and their traffics are extracted by simulation with MPSOcBench. Second, Noxim-XT tests various hardware configurations of the NoC, and for each configuration, the application's traffic is re-injected and replayed, an accurate performance and power breakdown is provided, and the user can choose different data coding strategies. With the help of Noxim XT, each configuration is bit-accurately estimated in terms of energy consumption. After simulation, a spatial mapping of the energy consumption is provided and highlights the hot-spots. Moreover, the new coding strategies allows significant energy saving. Noxim XT simulations and a FPGA-based prototype of a new coding strategy will be demonstrated at the U-booth to illustrate these works.

OPENCTMOD: AN OPEN SOURCE COLLABORATIVE MATLAB TOOLBOX FOR THE DESIGN AND SIMULATION OF CONTINUOUS-TIME SIGMA DELTA MODULATORS

Presenter: Dang-Kiên Germain Pham, LTCI, Télécom ParisTech, Université Paris-Saclay, [75013], Paris, France, FR
Author: Chadi Jabbour, LTCI, Télécom ParisTech, Université Paris-Saclay, FR

Timeslots: UB04.3 (Tuesday, March 28, 2017 1730 - 1930)

Abstract: Simulating Continous Time (CT) Sigma Delta Modualors (SDM) is commonly done using block level systems such as Simulink which is a highly time consuming task even at system level. Therefore, the existing design tools for SDM are either discrete time oriented (Schreier toolbox) or proprietary (Ulm toolbox). In this work, we propose a new Matlab/C toolbox for the design of CT SDM. Simulation is based on state space representation thereby allowing to support most of the existing SDM architectures. Moreover, the main non-idealities of the main blocks are modeled (opamp DC gain, finite GBW, DACs mismatch, ISI and quantizer offset). Besides, thanks to the modular and open source approach for this toolbox, every user can easily implement additional features and include it. During the forum, designs and simulations for various architectures of CT SDM will be performed to demonstrate the accuracy and efficiency of the proposed toolbox. The collaborative aspect will be also shown.

PER: METHOD AND TOOL FOR ANALYZING THE INTERPLAY BETWEEN PERFORMANCE, ENERGY AND SCALING IN MULTI- AND MANY-CORE PLATFORMS

Presenter: Fei Xia, Newcastle University, GB
Authors: Ashur Rafiev, Alexander Romanovsky and Alex Yakovlev, Newcastle University, GB

Timeslots: UB01.10 (Tuesday, March 28, 2017 1030 - 1230)
UB06.7 (Wednesday, March 29, 2017 1200 - 1400)
UB07.7 (Wednesday, March 29, 2017 1400 - 1600)

Abstract: Parallelization has been used to maintain a reasonable balance between energy consumption and performance in computing systems. However, the effectiveness of parallelization scaling is different for different hardware platforms. This is because the reliable operation region (ROR), a region defined in the voltage-throughput space for any hardware platform, is platform-dependent and its shape determines how effective parallelization scaling is in improving throughput and/or reducing power consumption. Although many of the interlinked issues are known, a unifying analysis method has just now been proposed to study the interplay between performance, energy, reliability and parallelization scaling. The method of bi-normalization of the ROR is designed to help achieve a meaningful cross-platform analysis of this interplay. The PER tool brings all these issues together and helps designers reason about hardware parallelization, DVFS and software parallelizability.

PULP: A ULTRA-LOW POWER PLATFORM FOR THE INTERNET-OF-THINGS

Presenter: Francesco Conti, ETH Zurich, CH
Authors: Stefan Mach[1], Florian Zaruba[1], Antonio Pullini[1], Daniele Palossi[1], Giovanni Rovere[1], Florian Glaser[1], Germain Haugou[1], Schekeb Fateh[1] and Luca Benini[2]
[1]ETH Zurich, CH; [2]ETH Zurich, CH and University of Bologna, IT

Timeslots: UB03.10 (Tuesday, March 28, 2017 1500 - 1730)
UB07.10 (Wednesday, March 29, 2017 1400 - 1600)
UB08.10 (Wednesday, March 29, 2017 1600 - 1800)
UB09.10 (Thursday, March 30, 2017 1000 - 1200)

Abstract: The PULP (Parallel Ultra-Low Power) platform strives to provide high performance for IoT nodes and endpoints within a very small power envelope. The PULP platform is based on a tightly-coupled multi-core cluster and on a modular architecture, which can support complex configurations with autonomous I/O without SW intervention, HW-accelerated execution of hot computation kernels, fine-grain event-based computation - but can also be deployed in very simple configuration, such as the open source PULPino microcontroller. In this demonstration booth, we will showcase several prototypes using PULP chips in various configuration. Our prototypes perform demos such as real-time deep-learning based visual recognition from a low-power camera, and online biosignal acquisition and reconstruction on the same chip. Application scenarios for our technology include healthcare wearables, autonomous nano-UAVs, smart networked environmental sensors.

RIMEDIO: WHEELCHAIR MOUNTED ROBOTIC ARM DEMONSTRATOR FOR PEOPLE WITH MOTOR SKILLS IMPAIRMENTS

Presenter: Alessandro Palla, University of Pisa, IT
Authors: Gabriele Meoni and Luca Fanucci, University of Pisa, IT

Timeslots: UB03.2 (Tuesday, March 28, 2017 1500 - 1730)
UB04.2 (Tuesday, March 28, 2017 1730 - 1930)
UB05.2 (Wednesday, March 29, 2017 1000 - 1200)
UB07.2 (Wednesday, March 29, 2017 1400 - 1600)

Abstract: People with reduced mobility experiment many issues in the interaction with the indoor and outdoor environment because of their disability. For those users even the simplest action might be a hard/impossible task to perform without the assistance of an external aid. We propose a simple and lightweight wheelchair mounted robotic arm with the focus on the human-machine interface that has to be simple and accessible for users with different kind of disabilities. The robotic arm is equipped with a 5 MP camera, force and proximity sensors and a 6 axis Inertial Measurement Unit on the end-effector that can be controlled using an app running on a tablet. When the user selects the object to reach (for instance a button) on the tablet screen, the arm autonomously carries out the task, using the camera image and the sensors measurements for autonomous navigation. The demonstrator consists in the robotic arm prototype, the Android tablet and a personal computer for arm setup and configuration.

RUNNING CONVOLUTIONAL LAYERS OF ALEXNET IN NEUROMORPHIC COMPUTING SYSTEM

Presenter: Yongshin Kang, Incheon National University, KR
Authors: Seban Kim, Taehwan Shin and Jaeyong Chung, Incheon National University, KR

Timeslots: UB03.6 (Tuesday, March 28, 2017 1500 - 1730)

Abstract: Neuromorphic hardware has drawn attention as an approach to deal with the issues of today's computing platforms based on Von Neumann architecture when running deep learning models, but large-scale deep neural networks such as AlexNet have not been demonstrated yet in any neuromorphic systems. Since 2014, we have been developing a non-Von Neumann computing system called INSight based on data flow architecture that aims at running large-scale deep neural networks in the neuromorphic fashion. We have now reached a major milestone and will demonstrate INSight running the convolutional layers of AlexNet. The proposed system is implemented with Xilinx Virtex 7 FPGA and performs the processing using 100K synapses mapped on LUTs without any array-type memories. It processes 1552 images per second and consumes 7.2W, resulting in the state-of-the-art energy efficiency.

SCCHARTS: SYNCHRONOUS STATECHARTS FOR SAFETY-CRITICAL APPLICATIONS

Presenter: Reinhard von Hanxleden, Kiel University, DE
Authors: Michael Mendler[1], Christian Motika[2], Christoph Daniel Schulze[2] and Steven Smyth[2]
[1]Bamberg University, DE; [2]Kiel University, DE

Timeslots: UB05.5 (Wednesday, March 29, 2017 1000 - 1200)
UB07.5 (Wednesday, March 29, 2017 1400 - 1600)

Abstract: We present a visual language, SCCharts, designed for specifying safety-critical reactive systems. SCCharts use a statechart notation and provide determinate concurrency based on a synchronous model of computation (MoC), without restrictions common to previous synchronous MoCs. Specifically, we lift earlier limitations on sequential accesses to shared variables, by leveraging the sequentially constructive MoC. For further de-

tails, see [von Hanxleden et al., PLDI'14] and http://www.sccharts.com. The SCCharts demonstrator is an Eclipse Richt Client and part of KIELER (http://www.rtsys.informatik.uni-kiel.de/en/research/kieler). The demonstration shows how to write an SCChart model using a textual notation, from which a visual model is generated on the fly using the Eclipse Layout Kernel (ELK). We also present a compilation chain that allows efficient synthesis of software and hardware.

SEFILE: A SECURE FILESYSTEM IN USERSPACE VIA SECUBE™

Presenter: Giuseppe Airofarulla, CINI, IT
Authors: Paolo Prinetto[1] and Antonio Varriale[2]
[1]CINI & Politecnico di Torino, IT; [2]Blu5 Labs Ltd., IT

Timeslots: UB01.9 (Tuesday, March 28, 2017 1030 - 1230)
UB02.9 (Tuesday, March 28, 2017 1230 - 1500)
UB05.9 (Wednesday, March 29, 2017 1000 - 1200)
UB06.9 (Wednesday, March 29, 2017 1200 - 1400)

Abstract: The SEcube™ Open Source platform is a combination of three main cores in a single-chip design. Low-power ARM Cortex-M4 processor, a flexible and fast Field-Programmable-Gate-Array (FPGA), and an EAL5+ certified Security Controller (SmartCard) are embedded in an extremely compact package. This makes it a unique Open Source security environment where each function can be optimized, executed, and verified on its proper hardware device. In this demo, we present a Windows wrapper for a Filesystem in Userspace (FUSE) with an HDD firewall resorting to the hardware built-in capabilities, and the software libraries, of the SEcube™.

SELINK: SECURING HTTP AND HTTPS-BASED COMMUNICATION VIA SECUBE™

Presenter: Airofarulla Giuseppe, CINI & Politecnico di Torino, IT
Authors: Paolo Prinetto[1] and Antonio Varriale[2]
[1]Politecnico di Torino, IT; [2]Blu5 Labs Ltd., IT

Timeslots: UB04.8 (Tuesday, March 28, 2017 1730 - 1930)
UB07.8 (Wednesday, March 29, 2017 1400 - 1600)
UB08.8 (Wednesday, March 29, 2017 1600 - 1800)

Abstract: The SEcube™ Open Source platform is a combination of three main cores in a single-chip design. Low-power ARM Cortex-M4 processor, a flexible and fast Field-Programmable-Gate-Array (FPGA), and an EAL5+ certified Security Controller (SmartCard) are embedded in an extremely compact package. This makes it a unique Open Source security environment where each function can be optimized, executed, and verified on its proper hardware device. In this demo, we present a client-server HTTP and HTTPS-based application, for which the traffic is encrypted resorting to the hardware built-in capabilities, and the software libraries, of the SEcube™. By doing so, we show how communication can be secured from an attacker capable of inspecting, and tampering, the regular communication.

STACKADROP: A MODULAR DIGITAL MICROFLUIDIC BIOCHIP RESEARCH PLATFORM

Presenter: Oliver Keszöcze, University of Bremen, DE
Authors: Maximilian Luenert and Rolf Drechsler, University of Bremen & DFKI GmbH, DE

Timeslots: UB03.9 (Tuesday, March 28, 2017 1500 - 1730)
UB07.9 (Wednesday, March 29, 2017 1400 - 1600)
UB10.5 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Advances in microfluidic technologies have led to the emergence of Digital Microfluidic Biochips (DMFBs), which are capable of automating

laboratory procedures. These DMFBs raised significant attention in industry and academia creating a demand for devices. Commercial products are available but come at a high price. So far, there are two open hardware DMFBs available: the DropBot from WheelerLabs and the OpenDrop from GaudiLabs. The aim of the StackADrop was to create a DMFB with many directly addressable cells while still being very compact. The StackADrop strives to provide means to experiment with different hardware setups. It's main feature are the exchangeable top plates, supporting 256 high-voltage pins. It features SPI, UART and I2C connectors for attaching sensors/actuators and can be connected to a computer using USB for interactive sessions using a control software. The modularity allows to easily test different cell shapes, such as squares, hexagons and triangles.

TFA: TRANSPARENT CODE OFFLOADING ON FPGA

Presenter: Roberto Rigamonti, HEIG-VD/HES-SO, CH
Authors: Anthony Convers, Baptiste Delporte, Xavier Ruppen and Alberto Dassatti, HEIG-VD/HES-SO, CH

Timeslots: UB01.2 (Tuesday, March 28, 2017 1030 - 1230)
UB09.2 (Thursday, March 30, 2017 1000 - 1200)
UB10.2 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Genomics, molecular dynamics, and machine learning are just the most recent examples of fields where FPGAs could provide the means to achieve interesting breakthroughs. However, HDL programming requires considerable multi-disciplinary skills, experience, large budgets, time, and a bit of wizardry. Given that most implementations are short-lived, the investment simply does not pay off. In this demo we propose a multi-vendor LLVM-based automated framework that can transparently - without the user or developer being aware of it - offload computing-intensive code fragments to FPGAs. The system relies on a performance monitor to detect computing-intensive code sections and, if they are suitable for offloading, extracts the Data Flow Graph and uses it to program an overlay pre-programmed on the FPGA, which then interacts with the Just-In-Time compiler executing the program. The overall process requires hundreds of microseconds, and can be easily reverted should the outcome be unsatisfactory.

TGV: TESTER GENERIC AND VERSATILE FOR RADIATION EFFECTS ON ADVANCED VLSI CIRCUITS

Presenter: Miguel Solinas, TIMA, FR
Authors: Alexandre Coelho Coelho, Juan Fraire, Nacer Eddine Zergainoh and Raoul Velazco, Univ. Grenoble Alpes, CNRS, Grenoble INP, FR

Timeslots: UB11.1 (Thursday, March 30, 2017 1430 - 1630)

Abstract: The purpose of this work is to describe a novel tester for radiation effects experiments, called TGV (Tester Generic and Versatile) based on a commercial development board ZEDBOARD. The main idea is to implement the whole DUT (Device Under Test) board architecture controlled by an FPGA, whose configuration is obtained from compiling the description of key features of the DUT in a high-level language such as C. This tester constitutes a powerful tool with generic capabilities for the functional validation and test under radiation of any digital circuit, with a particular focus on processor-like circuits. In this way, there is only a minor hardware development, limited to wiring the DUT pins to the ones of the tester connector. During the demonstration will be shown details of TGV platform, its use being illustrated be means of fault injection experiments which reproduces in a realistic way the random occurrence in time and location of SEUs in sensitive targets of the considered circuit.

TIDES: NON-LINEAR WAVEFORMS FOR QUICK TRACE NAVIGATION

Presenter: Jannis Stoppe, University of Bremen, DE
Author: Rolf Drechsler, University of Bremen / DFKI, DE

Timeslots: UB02.8 (Tuesday, March 28, 2017 1230 - 1500)
UB06.8 (Wednesday, March 29, 2017 1200 - 1400)
UB09.8 (Thursday, March 30, 2017 1000 - 1200)
UB10.8 (Thursday, March 30, 2017 1200 - 1430)

Abstract: System trace analysis is mostly done using waveform viewers -- tools that relate signals and their assignments at certain times. While generic hardware design is subject to some innovative visualisation ideas and software visualisation has been a research topic for much longer, these classic tools have been part of the design process since the earlier days of hardware design -- and have not changed much over the decades. Instead, the currently available programs have evolved to look practically the same, all following a familiar pattern that has not changed since their initial appearance. We argue that there is still room for innovation beyond the very classic waveform display though. We implemented a proof-of-concept waveform viewer (codenamed Tides) that has several unique features that go beyond the standard set of features for waveform viewers.

TTOOL5G: MODEL-BASED DESIGN OF A 5G UPLINK DATA-LINK LAYER RECEIVER FROM UML/SYSML DIAGRAMS

Presenter: Andrea Enrici, Nokia Bell Labs France, FR
Authors: Julien Lallet[1], Imran Latif[1], Ludovic Apvrille[2], Renaud Pacalet[2] and Adrien Canuel[2]
[1]Nokia Bell Labs France, FR; [2]Télécom ParisTech, FR

Timeslots: UB02.3 (Tuesday, March 28, 2017 1230 - 1500)
UB06.3 (Wednesday, March 29, 2017 1200 - 1400)
UB10.3 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Future 5G networks are expected to provide an increase of 10x in data rates. To meet these requirements, the equipment of baseband stations will be designed using mixed architectures, i.e., DSPs, FPGAs. However, efficiently programming these architectures is not trivial due to the drastic increase in complexity of their design space. To overcome this issue, we need to have unified tools capable of rapidly exploring, partitioning and prototyping the mixed architecture designs of 5G systems. At DATE 2017 University Booth, we demonstrate such a unified tool and show our latest achievements in the automatic code generation engine of TTool/DIPLODOCUS, a UML/SysML framework for the hardware/software co-design of dataflow systems, to support mixed architectures. Our demonstration will show the full design and evaluation of a 5G data-link layer receiver for both a DSP-based and an IP-based designs. We will validate the effectiveness of our solution by comparing automated vs manual designs.

WE DARE: WEARABLE ELECTRONICS DIRECTIONAL AUGMENTED REALITY

Presenter: Davide Quaglia, University of Verona, IT
Authors: Gianluca Benedetti[1] and Walter Vendraminetto[2]
[1]Wagoo LLC, IT; [2]EDALab srl, IT

Timeslots: UB02.2 (Tuesday, March 28, 2017 1230 - 1500)
UB06.4 (Wednesday, March 29, 2017 1200 - 1400)
UB10.10 (Thursday, March 30, 2017 1200 - 1430)

Abstract: Current augmented reality (AR) eyewear solutions require large form factors, weight, cost and energy that reduce usability. In fact, connectivity, image processing, localization, and direction evaluation lead to high processing and power requirements. A multi-antenna system, patented by the industrial partner, enables a new generation of smart eye-wear

that elegantly requires less hardware, connectivity, and power to provide AR functionalities. They will allow users to directionally locate nearby radio emitting sources that highlight objects of interest (e.g., people or retail items) by using existing standards like Bluetooth Low Energy, Apple's iBeacon and Google's Eddystone. This booth will report the current level of research addressed by the Computer Science Department of University of Verona and the company Wagoo LLC. In the presented demo, different objects emit an "I am here" signal and a prototype of the smart glasses shows the information related to the observed object.

WORKCRAFT: TOOLSET FOR FORMAL SPECIFICATION, SYNTHESIS AND VERIFICATION OF CONCURRENT SYSTEMS

Presenter: Danil Sokolov, Newcastle University, GB

Timeslots: UB02.1 (Tuesday, March 28, 2017 1230 - 1500)
UB03.1 (Tuesday, March 28, 2017 1500 - 1730)

Abstract: A large number of models that are employed in the field of concurrent systems' design, such as Petri nets, gate-level circuits, dataflow structures have an underlying static graph structure. Their semantics, however, is defined using additional entities, e.g. tokens or node/arc states, which collectively form the overall state of the system. We jointly refer to such formalisms as interpreted graph models. This demo will show the use of an open-source cross-platform Workcraft framework for capturing, simulation, synthesis, and verification of such models. The focus of our case study will be on synthesis from technology-independent formal specifications to verifiable circuit implementations.

XBARGEN: A TOOL FOR DESIGN SPACE EXPLORATION OF MEMRISTOR BASED CROSSBAR ARCHITECTURES.

Presenter: Marcello Traiola, LIRMM, FR
Authors: Mario Barbareschi[1] and Alberto Bosio[2]
[1]University of Naples Federico II, IT; [2]University of Montpellier - LIRMM laboratories, FR

Timeslots: UB01.7 (Tuesday, March 28, 2017 1030 - 1230)
UB05.7 (Wednesday, March 29, 2017 1000 - 1200)
UB09.6 (Thursday, March 30, 2017 1000 - 1200)

Abstract: The unceasing shrinking process of CMOS technology is leading to its physical limits, impacting several aspects, such as performances, power consumption and many others. Alternative solutions are under investigation in order to overcome CMOS limitations. Among them, the memristor is one of promising technologies. Several works have been proposed so far, describing how to synthesize boolean logic functions on memristors-based crossbar architecture. However, depending on the synthesis parameters, different architectures can be obtained. In this demo, we show a Design Space Exploration (DSE) that we use to select the best crossbar configuration on the basis of workload dependent and independent parameters, such as area, time and power consumption. The main advantage is that it does not require any simulation and thus it avoid any runtime overheads. The demo aims to show the tool prototype on a selected set of benchmarks which will be synthesized on a memristor-based crossbar circuit.

See you at the University Booth!

University Booth Co-Chairs
Elena Ioana Vatajelu, TIMA Laboratory, FR and
Andreas Vörg, edacentrum, DE

FRINGE TECHNICAL MEETINGS

A number of specialist interest groups will be holding their meetings at DATE 2017. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage **www.date-conference.com**

Day+Time	Meeting & Contact	Room
MON 1800-2100	**Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA** Cecilia Metra, University of Bologna, IT cecilia.metra@unibo.it	Campus Foyer (Grätzel)
TUE 1300-1430	**eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)** Giorgio Di Natale, LIRMM, FR giorgio.dinatale@lirmm.fr	4A
TUE 1615-1800	**EDAA General Assembly** Wolfgang Nebel, OFFIS & University of Oldenburg, DE, wolfgang.nebel@offis.de	4A
WED 1230-1430	**Meeting of the IFIP Working Group 10.5** Masahiro Fujita, University of Tokyo, JP fujita@ee.t.u-tokyo.ac.jp	4A
THU 1400-1500	**DATE Sister-Events Meeting** David Atienza, EPFL, CH david.atienza@epfl.ch	Office C

MON

Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Campus Foyer (Grätzel), First Level 1800 - 2100

Organiser: Cecilia Metra, University of Bologna, IT

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2017 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 27, 2017, from 1800 - 2100. The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

TUE

eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)

4A 1300 - 1430

Organiser: Giorgio Di Natale, LIRMM, FR

The European Test Technology Technical Council (eTTTC) is the European Section of the TTTC. eTTTC is a volunteer professional organization sponsored by the IEEE Computer Society. TTTC's goals are to contribute to our members' profesional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the-art. This meeting provides all actors involved in test technology to share information on upcoming events and projects.

TUE

EDAA General Assembly

4A 1615 - 1800

Organiser: Wolfgang Nebel, OFFIS & University of Oldenburg, DE

General assembly meeting for the members of EDAA, open to everyone interested in Electronic Design Automation

WED

Meeting of the IFIP Working Group 10.5

4A 1230 - 1430

Organiser: Masahiro Fujita, University of Tokyo, JP

International Federation for Information Processing (IFIP) is the leading multinational, apolitical organization in Information & Communications Technologies and Sciences and is recognized by United Nations and other bodies. It has over 100 Working Groups and 13 Technical Committees. This is a meeting organized by WK10.5 (VLSI related technologies).

THU

DATE Sister-Events Meeting

Office C 1400 - 1500

Organiser: David Atienza, EPFL, CH

Meeting of representatives from the sister conferences ASP-DAC, ICCAD, DAC, and DATE

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54

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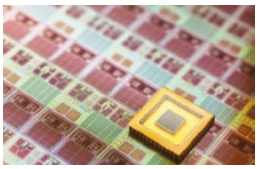


Engaging Technical Sessions - EDA, Embedded Systems, IoT, Automotive, Security, plus Designer Track and IP Track

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10:00am - 6:00pm
Tuesday, June 20:
10:00am - 6:00pm
Wednesday, June 21:
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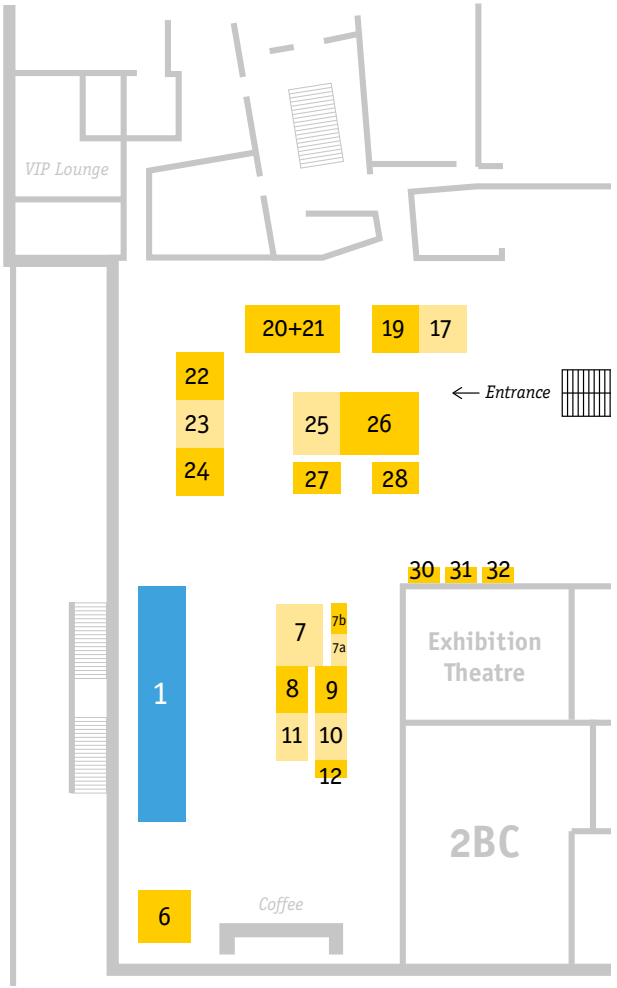
All corporate sponsors and participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

EXHIBITION FLOOR PLAN



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Cadence Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems. Cadence Academic Network is sponsoring the DATE Interactive Presentations (IPs) again.

Booth 6 Center for Advancing Electronics Dresden (cfaed)

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Germany

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W: www.cfaed.tu-dresden.de

The Cluster of Excellence 'Center for Advancing Electronics Dresden' (cfaed) of Technische Universität Dresden comprises eleven research institutes in Saxony. Further members are the Technische Universität Chemnitz, two Max Planck Institutes, two Fraunhofer Institutes, two Leibniz Institutes and the Helmholtz-Research Center Dresden-Rossendorf. About 300 scientists are working in nine research paths to investigate completely new technologies for electronic information processing. These technologies are inspired by innovative materials such as silicon nanowires, carbon nanotubes or polymers or based on completely new conceptions such as circuit fabrication methods by self-assembling structures, e.g. DNA-Origami. The orchestration of these new devices into heterogeneous information processing systems with focus on their resilience and energy-efficiency is also part of cfaed's research program. To complement the Cluster, the Collaborative Research Center (CRC) 912 'Highly Adaptive Energy-Efficient Computing' (HAEC) has been integrated in cfaed. Both, cfaed and HAEC, are coordinated by Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis, who holds the Vodafone Chair Mobile Communications Systems at TU Dresden.

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Booth 17 Circuits Multi-Projects (CMP)

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Cobham Gaisler AB is a provider of system-on-chip (SoC) solutions for advanced applications in the commercial and space flight domain. Cobham Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP cores and associated software and development tools. Our solutions help companies and research institutes develop highly competitive application-specific SoC designs, as well as providing radiation-hardened components for the space market.

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Booth 25 EcoCloud Center

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HiPEAC - European Network on High Performance and Embedded Architecture and Compilation

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HiPEAC is the largest and fastest growing membership network for High Performance Computing (HPC) and Embedded Computing professionals in Europe. Becoming a HiPEAC industry member indicates a commitment to learning, growing and personal and business success. All our membership benefits are aimed at providing members with a wealth of exclusive resources. HiPEAC membership is also a two-way street. It's not just about consuming, but also contributing – not just to the organisation, but more importantly to other members and the HPC and Embedded Computing industry as a whole. Our members drive our work through their participation at events and sharing of best practices and more. We draw on our members' expertise and experiences to shape our services. Each and every member brings something different to the table and it's those unique characteristics that make HiPEAC strong. HiPEAC membership is invaluable. Our vendor-neutral position, coupled with our communities targeted to specific market segments, allow us to create customised services – a huge benefit to our members and organisations like your own. Joining as a HiPEAC industry member, helps you and your business grow through timely industry insight, training, recruitment and peer-to-peer interaction. Get guidance from industry experts and attend our events and discuss business opportunities and challenges. Meet EU policy makers and help to shape the HiPEAC Vision, the definitive guide for EU policy makers on future technology action areas. To join for free email membership@hipeac.net. For further information visit www.hipeac/net/industry and don't forget to visit our stand here at DATE 2017!

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IEEE Council on Electronic Design Automation (IEEE CEDA)

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The Council on Electronic Design Automation (CEDA) was established to foster design automation of electronic circuits and systems at all levels. The Council's field of interest spans the theory, implementation, and use of EDA/CAD tools to design integrated electronic circuits and systems. This includes tools that automate all levels of the design, analysis, and verification of hardware and embedded software up to and including complete working systems. CEDA enables the exchange of technical information by sponsoring publications, conferences and workshops and through local chapters for volunteers activities.

If you are interested, please contact admin@ieee-ceda.com or check our website for more information about our activities and how to become a member for free.

Sponsor

Institute of Electrical Engineering (IEL)

EPFL STI IEL-GE, Station 11
CH-1015 Lausanne
Switzerland

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Website: http://sti.epfl.ch

The Section of Electrical Engineering offers a wide ranging Bachelor program covering three large intimately interconnected domains:

- Micro- Nano- Bioelectronics: microelectronics, integrated circuit design, transducers, nano- and bioelectronics
- Information technologies: acoustics, RF and microwaves, photonics, signal and image processing, image analysis, pattern recognition
- Energy - Smart Grids science and technology: smart grids, renewable energy, energy storage, production, transport, transformation by electronic means, study of devices to convert electrical to mechanical energy

We also offer a "MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING" EPFL that can be complemented by a minor in Space Technology, in Biomedical Engineering, in Energy, in Materials Science, in Management of Technology or in Contemporary Asian Studies.

Booth 32

INTENTO DESIGN

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Intento Design provide responsive technology for analog IP. The company was born from 25 years of research aimed at developing a new analog design methodology . This research resulted in an extensive portfolio of intellectual property, including an innovative EDA tool that accelerates the design cycle by automating the sizing and migration of analog and mixed-signal circuitry used in complex SoCs for a variety of connected applications.

The Intento Design methodology solves the productivity gap inherent in the analog design process by reducing lengthy simulation iterations. Traditionally, analog and mixed-signal design requires the engineer to compute initial circuit dimensions from hand analysis using first order transistor models followed by successive simulations.

This tedious and time-consuming process can take weeks for a complex circuit. Intento accelerates this process with software that plugs into the existing design flows and standard tools, and automates the circuit sizing,

thereby allowing designers to move on to layout, placement and routing in a fraction of the time.

The Intento Design methodology keeps the designer at the centre of the process, specifying the parameters that must be met by the circuit; reviewing the options based on desired power consumption, performance and surface area; and selecting the optimal solution.

Booth 12

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Linktronix AG has been the official Tektronix, Keithley and Fluke Partner for Switzerland since 2004. We help you to choose the right measurement system, we demonstrate the newest products and deliver a wide range of instruments from our warehouse in Thalwil in 24h.

We have access to a large pool of demo equipment. It is our pleasure to assist you in all belongings regarding Tektronix, Keithley and Fluke products.

Booth 28

MAGILLEM

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Magillem is a Leading Provider of Complex Design Flow and Content Management Software Solutions.
Magillem has developed an easy-to-use, state of the art platform to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SoC.
Magillem integrated design environment offers a non-disruptive framework, a backbone to the design flow, providing fluidity, flexibility, seamless execution of the entire flow and better control to designers.
Thanks to early focus on XML, the company has quickly become a specialist of design and content automation, offering a multi-industry and cross-disciplinary approach to its clients.
Magillem's innovative technology now enables the integration of specification, design and documentation into a unique process.

ASIC and SOC Design:
Design Entry • Analogue and Mixed-Signal Design

System-Level Design:
Hardware/Software Co-Design

Booth 24

MathWorks

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MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development.

MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink® is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. The company produces nearly 100 additional products for specialized tasks such as machine learning, computer vision, robotics, and C and HDL code generation.

MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. MATLAB and Simulink enable the design and development of a wide range of advanced products, including automotive systems, aerospace flight control and avionics, telecommunications and other electronics equipment, industrial machinery, and medical devices. More than 5000 colleges and universities around the world use MATLAB and Simulink for teaching and research in a broad range of technical disciplines.

ASIC and SOC Design:
Behavioural Modelling & Simulation • Verification • Analogue and Mixed-Signal Design • RF Design

System-Level Design:
Behavioural Modelling & Analysis • Hardware/Software Co-Design

Test:
System Test

Services:
Design Consultancy • Training

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Mentor Graphics

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Mentor Graphics is a technology leader in electronic design automation, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues of $1.24 billion in the last fiscal year. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: www.mentor.com. We offer the broadest industry portfolio of best-in-class hardware and software design solutions focused on IC design and physical verification, functional verification, FPGA/PLD, design-for-test, PCB design embedded software and automotive EE design. Mentor Graphics innovative tools help our customers solve current and future design challenges, including scalable solutions for functional verification, cutting-edge technology for design-for-manufacturability and mixed-level IC design verification, award-winning test compression technology, embedded software development systems, and market-leading integrated system design solutions.

ASIC and SOC Design:
Design Entry • Verification • Analogue and Mixed-Signal Design

System-Level Design:
Acceleration & Emulation • PCB & MCM Design

Test:
Design for Test

Embedded Software Development:
Compilers • Real Time Operating Systems

Booth 26 Nano-Tera.ch

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Nano-Tera.ch is a Swiss national program supporting research in multi-scale system engineering for health, security, energy and the environment. The broad objectives of the program are to improve quality of life and security of people and to create innovative products, technologies and manufacturing methods, thus resulting in job and revenue creation.

Launched in 2008, Nano-Tera.ch is one of the largest federal programs funding research in engineering sciences. It is a strongly established program which has been supporting about 140 projects for a total budget of more than 250 MCHF. The 1200+ staff members active in Nano-Tera.ch projects represent 50 research institutions which constitute an almost exhaustive coverage of the Swiss scientific community in the program's fields.

The research funded resulted in more than 1000 peer-reviewed publications (40% of which in established journals) and numerous prototypes and demonstrators, a tangible sign that the program focuses on concrete collaborative research leading to potentially exploitable results.

Building upon this success, the program is further pursuing its main objectives: excellence in collaborative research in engineering disciplines, educational programs, design of applied demonstrators, and transfer of acquired research results to the Swiss industry.

The research carried out in the program explores various key thematic areas, such as smart prosthetics and body repair, health monitoring, as well as various medical platforms. In addition to these health-related challenges, Nano-Tera.ch also tackles important issues in environmental monitoring, and on the crucial theme of smart energy.

Product Key Finders: Engineering, Multi-Scale, Complex, Health, Energy, Environment

Booth 7 NCCR Robotics, Swiss National Center of Robotics

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The Swiss National Centre of Competence in Research Robotics (NCCR Robotics) brings together a selection of the top robotics laboratories in Switzerland to advance research, education and technology transfer of future intelligent robots with a focus on wearable robotics and mobile robotics for rescue and education.

Wearable robots: prosthetic robots and exoskeletons for rehabilitation and training. We work with neurologists and physicians to truly understand the human body and nervous system so that robots are attuned to the needs of the wearer. This includes developing novel prosthetic limbs to process impulses directly from the brain with implantable or surface sensors; developing novel soft technologies such as artificial skin, stretchable electronics and compliant actuators; developing novel forms of artificial intelligence to make these robots more human; and immersive human-robot interaction.

Mobile robotics for Rescue/Education: flying, walking, or swimming robots for rescue missions or transportation, inspection and human assistance. Our strength is the inspiration from biological systems to make mobile robots perceptually aware and autonomous, safe and easy to use by humans, and capable of moving in very diverse environments. We work with

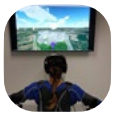
robotics

Swiss National Centre of Competence in Research

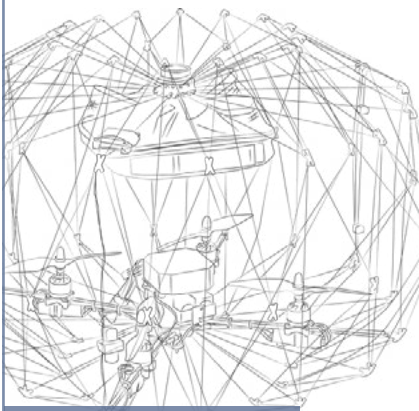
FNSNF Swiss National Science Foundation

Intelligent Robots for Improving the Quality of Life

The Swiss National Centre of Competence in Robotics (NCCR Robotics) is a federally funded programme bringing together robotics laboratories from EPFL, ETH Zurich, University of Zurich and IDSIA to work on wearable, rescue and educational robots.





Competencies
- Brain-computer interface
- Functional electrical stimulation
- Neural implants
- Wearable sensors
- Tactile sensors
- Vision sensors
- Neuromorphic chips
- Machine learning
- Haptic feedback
- Autonomous navigation
- Perception and control
- Virtual reality

Hardware
- Prosthetic robots
- Rehabilitation robots
- Walking robots
- Swimming robots
- Flying robots
- Multimodal robots
- Biomimetic robots
- Soft robots
- Foldable robots
- Swarm robots
- Manipulating robots
- Educational robots

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SWISS ROBOTICS INDUSTRY DAY 2017

The third Swiss Robotics Industry Day organised by NCCR Robotics on 2nd November 2017 at the Swiss Tech Convention Center, Lausanne, will showcase cutting edge robotics research and SMEs from the 23 professorships in NCCR Robotics and the Swiss Robotics ecosystem. The day is a vital opportunity for industry in fields that use robotics to network with potential partners, talents and collaborators as well as offering privileged access to new and emerging technologies. Find out more and request an invitation at swissroboticsindustry.ch

EPFL École polytechnique fédérale de Lausanne
ETH zürich
Universität Zürich
IDSIA

end users and regulators to make sure that these robots respond to real needs and have an impact on society.

Booth 9 POLYTEDA CLOUD LLC

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POLYTEDA CLOUD, established in 2015 and headquartered in Kyiv, Ukraine, develops cloud-ready PV-workflow based on the fastest and most accurate flat engine in the market with hierarchical and multi-CPU capabilities. POLYTEDA CLOUD introduces an innovative, new business model to the traditional EDA industry. PowerDRC/LVS addresses the complex "physical verification" stage of microchip design, critical before the actual manufacturing at the semiconductor foundry.

In December 2016 POLYTEDA CLOUD signed agreement with the European Commission under Horizon 2020 SME Instrument for a 2-year project "Innovative Cloud-Based PV Workflow for Semiconductor Foundries".

ASIC and SOC Design:
Verification

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The privately held company was founded in 1982 and has around 80 employees, with various facilities in Germany and France. PRO DESIGN has more than 30 years of experience in the EDA market and as provider in the E²MS market. It has built extensive knowledge in the areas of FPGA Board development, electronic engineering, FPGA design, high performance PCB design, construction, production, assembly and testing.

PRO DESIGN is the vendor of the successful proFPGA product line. The proFPGA product family is a complete, scalable, and modular multi FPGA Prototyping solution, which fulfills highest needs in the area of ASIC and IP Prototyping and pre-silicon software development. The proFPGA product series consists of different kind of motherboards, various Xilinx Virtex 7 and Virtex UltraScale based FPGA Modules, a set of interconnection boards/cables, and a range of daughter boards (e.g. DDR3 memory boards, high speed interface boards (like PCIe, USB 3.0, Gigabit Ethernet, etc.). It addresses customers who need a scalable and most flexible high performance FPGA based Prototyping solution for early software development and IP and ASIC verification. The innovative system concept and technologies offers best in class reusability for several projects, which guarantees the best return on invest. For more information about PRO DESIGN please visit: www.proFPGA.com

ASIC and SOC Design:
Verification

System-Level Design:
Acceleration & Emulation • Hardware/Software Co-Design

Test:
System Test

Services:
Prototyping

Hardware:
FPGA & Reconfigurable Platforms • Development Boards

Booth 8

Silvaco

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Silvaco is a leading EDA provider of software tools used for process and device development and for analog/mixed-signal, power IC and memory design. The portfolio also includes tools for power integrity sign off, reduction of extracted netlist, variation analysis and also production-proven intellectual property (IP) cores. Silvaco delivers a full TCAD-to-Signoff flow for vertical markets including: displays, power electronics, optical devices, radiation & soft error reliability, analog and HSIO design, library and memory design, advanced CMOS process and IP development.

ASIC and SOC Design:
Design Entry • Analogue and Mixed-Signal Design

Services:
IP e-commerce & Exchange

Semiconductor IP:
Analogue & Mixed Signal IP • CPUs & Controllers • On-Chip Bus Interconnect • On-Chip Debug

Application-Specific IP:
Analogue & Mixed Signal IP • Data Communication

B.20+21

Springer Nature

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Synopsys is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products.

Founded by Dr. Aart de Geus and a team of engineers from General Electric's Microelectronics Center in Research Triangle Park, North Carolina, Synopsys was first established as "Optimal Solutions" with a charter to develop and market ground-breaking synthesis technology developed by the team at General Electric. The company pioneered the commercial application of logic synthesis that has since been adopted by every major semiconductor design company in the world. This technology provided an exponential leap in integrated circuit (IC) design productivity by enabling engineers to specify chip functionality at a higher level of abstraction. Without this technology, the complex designs of today would not be possible.

Since 1986, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems that are found in the electronics that people rely on every day.

See more at: www.synopsys.com/company.html

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Texas Instruments

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The Texas Instruments University Program is dedicated to supporting engineering educators, researchers and students worldwide. Since 1982, the program has facilitated the inclusion of TI analog and embedded processing technology in the learning experience for engineering students, including classrooms; teaching and research labs; textbooks; design projects and contests; and course curricula. By doing this, TI aims to bridge the gap between the worlds of business and academia, bringing real world engineering concepts to life for thousands of students every year. Imagine the impact.

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Booth 1

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The University Booth fosters the transfer of academic work to industry. The University Booth is part of the DATE 2017 exhibition and is free of charge for presenters and their visitors. The University Booth is sponsored by the DATE Sponsor's Committee. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are invited to present innovative hardware and software demonstrations. All demonstrations will be hosted in the DATE exhibition area, within a dedicated time slot.

Research institutes and universities interested in demonstrating their mature prototypes and pre-commercial results can find submission details at www.date-conference.com/exhibition/u-booth.

The University Booth is organized by the University Booth Co-Chairs
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university-booth@date-conference.com
Andreas Vörg, edacentrum GmbH, DE
university-booth@date-conference.com

ASIC and SOC Design:
Design Entry • Behavioural Modelling & Simulation • Synthesis • Power & Optimisation • Physical Analysis (Timing, Themal, Signal) • Verification • Analogue and Mixed-Signal Design • MEMS Design • RF Design

System-Level Design:
Behavioural Modelling & Analysis • Physical Analysis • Acceleration & Emulation • Hardware/Software Co-Design • Package Design • PCB & MCM Design

Test:
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Services:
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Embedded Software Development:
Compilers • Real Time Operating Systems • Debuggers • Software/Modelling

Hardware:
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Semiconductor IP:
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Application-Specific IP:
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Chair: Christoph Scholl, University of Freiburg, DE
Co-Chair: Armin Biere, Johannes Kepler University, AT

DT5 Design and Test for Analog and Mixed-Signal Systems and Circuits, and MEMS
Chair: Andre Ivanov, University of British Columbia, CA
Co-Chair: Georges Gielen, Katholieke Universiteit Leuven, BE

D6 Power Modeling, Optimization and Low-Power Design
Chair: Alberto Macii, Politecnico di Torino, IT
Co-Chair: Naehyuck Chang, KAIST, KR

D7 Network on Chip
Chair: Luca Carloni, Columbia, US
Co-Chair: Sebastien Le Beux, ECL, FR

D8 Architectural and Microarchitectural Design
Chair: Cristina Silvano, Politecnico di Milano, IT
Co-Chair: Elaheh (Eli) Bozorgzadeh, UC Irvine, US

D9 Temperature and Variability Aware System Design and Optimization
Chair: Giovanni Ansaloni, Universitá della Svizzera Italiana, CH
Co-Chair: Jose L. Ayala, Complutense University of Madrid, ES

D10 Reconfigurable Computing
Chair: Fabrizio Ferrandi, Politecnico di Milano, IT
Co-Chair: Philip Brisk, University of California, Riverside, US

D11 Logical and Physical Analysis and Design
Chair: Luis Miguel Silveira, Inesc, PT
Co-Chair: Tiziano Villa, Universita' di Verona, IT

D12 Emerging Technologies for Future Computing
Chair: Aida Todri-Sanial, CNRS, FR
Co-Chair: Subhasish Mitra, Stanford University, US

D13 Emerging Technologies for Future Computing
Chair: Jean-Michel Portal, IM2NP, FR
Co-Chair: Pierre-Emmanuel Gaillardon, University of Utah, US

A1 Green Computing Systems
Chair: Andreas Burg, EPFL, CH
Co-Chair: Muhammad Shafique, Technische Universität Wien, AT

A2 Communication, Consumer and Multimedia Systems
Chair: Steffen Paul, Universität Bremen, DE
Co-Chair: Theo Theocharides, University of Cyprus, CY

A3 Automotive Systems and Smart Energy Systems
Chair: David Boyle, Imperial College London, UK
Co-Chair: Davide Brunelli, DISI - University of Trento, IT

TECHNICAL PROGRAMME TOPIC CHAIRS

A4 Healthcare, Wellness and Assistive Technology
Chair: Francisco Rincon, EPFL, CH
Co-Chair: Olivier Romain, ENSEA, FR

A5 Secure Systems
Chair: Tim Güneysu, University of Bremen, DE
Co-Chair: Wieland Fischer, Infineon Technologies, DE

A6 Reliable and Reconfigurable Systems
Chair: Praveen Raghavan, IMEC, BE
Co-Chair: Christian Weis, University of Kaiserslautern, DE

A7 Applications of Emerging Technologies
Chair: Andy Tyrrell, University of York, GB
Co-Chair: Yu Wang, Tsinghua University, CN

A8 Industrial Experiences Brief Papers
Chair: Raphaël David, CEA LIST, FR
Co-Chair: Eugenio Villar, University of Cantabria, ES

T1 Modeling and Mitigation of Defects, Faults, Variability, and Reliability
Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE
Co-Chair: Said Hamdioui, TU Delft, NL

T2 Test Generation, Simulation and Diagnosis
Chair: Wu-Tung Cheng, Mentor, US
Co-Chair: Matteo Sonza Reorda, Politecnico di Torino, IT

T3 Design-for-Test, Test Infrastructures, Test Standards
Chair: Sybille Hellebrand, University of Paderborn, DE
Co-Chair: Ozgur Sinanoglu, New York University – Abu Dhabi, AE

T4 System-Level Reliability Design, Analysis and On-line Test
Chair: Cristiana Bolchini, Politecnico di Milano, IT
Co-Chair: Jaume Abella, Barcelona Supercomputing Center, ES

DT5 Design and Test for Analog and Mixed-Signal Systems and Circuits, and MEMS
Chair: Andre Ivanov, University of British Columbia, CA
Co-Chair: Georges Gielen, Katholieke Universiteit Leuven, BE

E1 Real-time, Networked, and Dependable Systems
Chair: Rodolfo Pellizzoni, University of Waterloo, CA
Co-Chair: Kai Lampka, University of Uppsala, SE

E2 Compilers and Software Synthesis for Embedded Systems
Chair: Frank Hannig, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair: Aviral Shrivastava, Arizona State University, US

E3 Model-based Design and Verification for Embedded Systems
Chair: Petru Eles, Linköping University, SE
Co-Chair: Alain Girault, INRIA, FR

E4 Embedded Software Architectures
Chair: Hiroyuki Tomiyama, Ritsumeikan University, JP
Co-Chair: Akash Kumar, Technische Universitaet Dresden, DE

E5 Software architectures for Cyber-Physical Systems
Chair: Paul Pop, Technical University of Denmark, DK
Co-Chair: Karl-Erik Årzén, Lund University, SE

DETAILED INDEX

NOTES

NOTES

Scope of the Event

The 21st DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers, and vendors, as well as specialists in hardware and software design, test, and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems, and embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days, and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design, and test communities. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, EDA algorithms and tools, testing of electronic circuits and systems, embedded software, application design, and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis, and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Green Computing Systems and Applications
- Temperature-Aware Design
- Temperature Modeling and Management
- Emerging Technologies for Computing Systems
- Emerging Memory Technologies and Applications
- Formal Methods and Verification
- Network-on-Chip
- Architectural and Microarchitectural Design
- Reconfigurable Computing
- Physical Design and Verification
- Analog and Mixed-Signal Circuits and Systems
- Interconnect and Packaging Modeling
- Communication, Consumer, and Multimedia Systems
- Transportation Systems
- Medical, Healthcare, and Assistive Technology Systems
- Energy Generation, Recovery, and Management Systems
- Secure Systems
- Reliable and Dependable Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation, and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time and Networked Systems
- Compilers and Code Generation for Embedded Systems
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software and Optimization for MPSoCs, Many-core, GPU-based, or Heterogeneous Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 10, 2017 via:
www.date-conference.com

Papers can be submitted either for standard oral presentation or for interactive presentation. **The Programme Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.**

Conference Organization

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Programme Chair: Ayse K. Coskun
Boston University, MA, US
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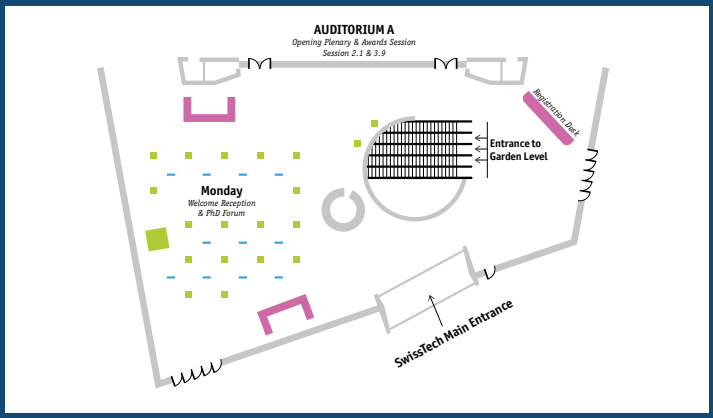
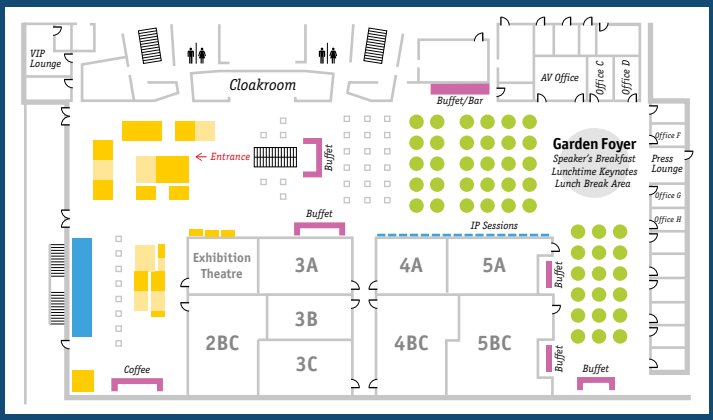
VENUE PLAN: FOYER CAMPUS GRAETZEL



VENUE PLAN: MONDAY 27 – THURSDAY 30



VENUE PLAN: FRIDAY 31