event guide

DATE 13

Alpexpo, Grenoble, France

Event 18 – 22 March Exhibition 19 – 21 March

Design, Automation & Test in Europe

The European System Design Show

From Systems-on-Chip to Embedded Computing




www.date-conference.com

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5 mailings a year (each 2 in 3 months)

Welcome to DATE 13

In this exhibition guide you will find listings of exhibitors contact details and their products being demonstrated on the exhibition floor. The classified product finder will help you locate the right solution within the show; maps and plans of Alpexpo and the exhibition hall will also help you to get around.

FREE - ENTRY to KEYNOTE SESSIONS, EXHIBITION THEATRE (see p.7) & SPECIAL EVENTS!

OPENING PLENARY KEYNOTES –

Tuesday, March 19, 2013, 0830 – 1030

Smart systems for internet of things

Benedetto Vigna -
Executive VP of STMicroelectronics, IT

Creating a sustainable information and communication infrastructure

Massoud Pedram -
Professor at University of Southern California, US

Exhibition Opening Times:

Tuesday 19 March 1000 - 1830*
(*Evening Reception from 1830 – 1930hrs)
Exhibition Drinks Reception offered by the City of Grenoble

Wednesday 20 March 1000 - 1800

Thursday 21 March 1000 - 1700

Entrance to the Exhibition is FREE

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tuesday 19 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030-1130 Exhibition Break, 1300-1430 Lunch, 1600-1700 Exhibition Break (1600-1630 IP1)					
0830	1.1 PLENARY: OPENING, AWARDS PRESENTATION AND KEYNOTE ADDRESSES, Auditorium Dauphine							
	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	APPLICATIONS	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1130 to 1300	2.1 EXECUTIVE SESSION - Advanced Technology Nodes: Dependency on Collaboration	2.2 Acceleration and Verification of ESL and Analog Systems	2.3 Energy Optimization in Multi-core Systems	2.4 Memory and Cache Architectures	2.5 Communications, Multimedia, and Consumer Electronics	2.6 HOT TOPIC: Reliability Challenges of Real-time Systems in Forthcoming Technology Nodes	2.7 Safety Critical Real-Time Systems	2.8 HOT TOPIC: IP Subsystems: The next productivity wave?
1300	1300-1400, Auditorium Dauphine: 3.0 Special Lunch-Time Session: Grenoble Ecosystem to Provide Semiconductor Alternative Process for Advanced CMOS							
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1430 to 1600	3.1 EXECUTIVE SESSION - The Role of Prototyping in Today's SOCs	3.2 PANEL: The Heritage of Mead & Conway	3.3 Addressing Process and Delay Variation in High-Level Synthesis	3.4 Microarchitectural Techniques for Reliability	3.5 Energy Efficient Mobile and Cloud Computing Systems	3.6 Dealing with Timing Variation in Advanced Technologies	3.7 Timing Analysis	3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1700 to 1830	4.1 EXECUTIVE SESSION - Is reusing off-the-shelf Semiconductor IP possible today?	4.2 The Quest for Better NoCs	4.3 EMBEDDED TUTORIAL: Reliability Analysis Reloaded: How Will We Survive?	4.4 Emerging Solutions to Manage Energy/Performance Trad-Offs Along the Memory Hierarchy	4.5 Device Identification and Protection	4.6 New Techniques for Test Pattern Generation	4.7 HOT TOPIC: Security Challenges in Automotive Hardware/Software Architecture Design	4.8 EXHIBITION THEATRE: Testimonials
1830	Evening Reception sponsored by the IEEE Council on EDA							

wednesday 20 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP2), 1230-1340 Lunch, 1600-1700 Exhibition Break (1600-1630 IP3)					
	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	APPLICATIONS	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
0830 to 1000	5.1 SPECIAL DAY 1 HOT TOPIC - System Approaches to Energy-Efficiency	5.2 PANEL - Can Energy Harvesting Deliver Enough Power for Automotive Electronics?	5.3 Post-Silicon Debug Techniques	5.4 Novel Approaches for Real-Time Architectures	5.5 Error-Aware Adaptive Modern Computing Architectures	5.6 Advances in Mixed-Signal, RF, and MEMS testing	5.7 Compilers and Software Synthesis for Embedded Systems	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1100 to 1230	6.1 SPECIAL DAY 1 - EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency	6.2 HOT TOPIC - Emerging Nanoscale Devices: A Booster for High Performance Computing	6.3 Verification and Simulation Support for Architecture	6.4 Design Space Exploration for Application Specific Architectures	6.5 Reliable Multi-Processor Computing Systems Design	6.6 HOT TOPIC - Energy-Efficient Design and Test Techniques for Future Multi-Core Systems	6.7 Model-Based Design and Verification for Embedded Systems	6. 8 EXHIBITION THEATRE: Silicon Europe – Leading European Regions Join Forces
1300	1330-1400, Room Oisans: 7.0 Special Day 1 Lunch-Time Keynote: Energy-Efficient Computing							
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1430 to 1600	7.1 SPECIAL DAY 1 HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency	7.2 Formal Verification Algorithms and Models	7.3 Dynamic Reconfiguration	7.4 Emerging Memory	7.5 Energy-efficient architectures and software design for power-constrained systems	7.6 On-Line Approaches Towards Processor Resilience	7.7 SPECIAL SESSION EMBEDDED TUTORIAL: From multi-core SoC to scale-out processors	
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1700 to 1830	8.1 SPECIAL DAY 1 HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency	8.2 Scheduling for Real-Time Embedded Systems	8.3 Logic Synthesis Techniques	8.4 High-Speed Robust NoCs	8.5 Industrial Experiences with Embedded System Design	8.6 DfT Methods	8.7 Monitoring and Control of Cyber Physical Systems	8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics

thursday 21 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP4), 1230-1400 Lunch, 1530-1600 Break (1530-1600 IP5)					
	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	DESIGN	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
0830 to 1000	9.1 SPECIAL DAY 2 - HOT TOPIC: Smart Grid and Buildings	9.2 System-Level Analysis and Simulation	9.3 Thermal/Power Management Techniques for Energy-Efficient Systems	9.4 Emerging Architectures	9.5 Manufacturing and Design Security	9.6 Improving IC Quality and Lifetime Though Advanced Characterisation	9.7 Design and Scheduling	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1100 to 1230	10.1 SPECIAL DAY 2 - HOT TOPIC: Smart Data Centers Design and Optimisation	10.2 EMBEDDED TUTORIAL: On the use of GP-GPUs for accelerating computing intensive EDA applications	10.3 Thermal Analysis and Power Optimisation Techniques	10.4 Abstraction Techniques and SAT/SMT-Based Optimisations	10.5 Design and Verification of Mixed-Signal Circuits	10.6 On-Line Testing Techniques	10.7 Embedded Software for Many-Core Architectures	10.8 PANEL: Will 3D-IC Remain a Technology of the Future... Even in the Future?
1330	1330-1400, Room Oisans: 11.0 Special Day 2 Lunch-Time Keynote: SMART CITIES AND COMMUNITIES AT THE REGIONAL, NATIONAL AND EUROPEAN LEVELS							
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1400 to 1530	11.1 SPECIAL DAY 2 - HOT TOPIC: Smart Health	11.2 High-Level Synthesis and Coarse-Grained Reconfigurable Architectures	11.3 Efficient NoC Routing Mechanisms	11.4 System-Level Modelling for Physical Properties	11.5 Energy Challenges for Multi-Core and NoC Architectures	11.6 Modelling and Design for Signal and Power Integrity	11.7 Powerful Aging	11.8 EMBEDDED TUTORIAL: Advances in Asynchronous logic
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1600 to 1730	12.1 SPECIAL DAY 2 - HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud	12.2 Methodologies to Improve Yield, Reliability and Security in Embedded Systems	12.3 NoC Mapping and Synthesis	12.4 Emerging Logic	12.5 Emerging Technology Architectures for Energy-Efficient Memories	12.6 Clock Distribution and Analogue Circuit Synthesis	12.7 Physical Design	12.8 EMBEDDED TUTORIAL: Closed-Loop Control for Power and Thermal Management

monday 18 march

0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS				
BREAKS	1100-1130 Morning, 1300-1430 Lunch, 1600-1630 Afternoon.				
0930 to 1800	A (Room - Belle-Etoile)	B (Room – Les Bans)	C (Room – Chartreuse)	F (Room – Stendhal)	G (Room – Bayard)
	Design Automation Of Electronic Systems: Past Accomplishments And Challenges Ahead - A Tribute To Robert Brayton	Advanced Techniques For Power-Aware System-Level Prototyping	E-Health: Systems, Components, Technologies	Post-Silicon Validation: Old Challenges and New Solutions	Design Methodologies For Adaptive Circuits And Systems
0930 to 1300	D1 (Room – Meije 2)	E1 (Room – Meije 3)	H1 (Room – 7 Laux 4)		
	Digital Microfluidic Biochips: Towards Hardware/Software Co-Design And Cyberphysical System Integration	Assertion Based Verification: A Common Verification Infrastructure For Soc And Embedded Software	Mixed-Signal Dft & Bist: Trends, Principles, And Solutions		
1430 to 1800	D2 (Room – Meije 2)	E2 (Room – Meije 3)	H2 (Room – 7 Laux 4)		
	Hardware Security And Trust	Design And Verification Of Embedded Systems From Natural Language Descriptions	Beyond Dft: The Convergence Of Dfm, Variability, Yield, Diagnosis And Reliability		
1800	Welcome Reception				

plenary session

Tuesday, March 19, 2013, 0830 – 1030 Auditorium Dauphine

Opening Address – Awards – Keynote Speakers

first keynote address

Smart systems for internet of things

Benedetto Vigna -
Executive VP of STMicroelectronics, IT

Sensors add intelligence to systems which represent a broad class of devices incorporating functionalities like sensing, actuation, and control. They are the core of smart components and subsystems; then, the challenge in the realization of such smart systems goes beyond the design of the individual components and subsystems and consists of accommodating a multitude of functionalities, technologies, and materials to play a key role to augment our daily life.

second keynote address

Creating a sustainable information and communication infrastructure

Massoud Pedram -
Professor at University of Southern California, US

Modern society's dependence on information and communication infrastructure (ICI) is so deeply entrenched that it should be treated on par with other critical lifelines of our existence, such as water and electricity. As is the case with any true lifeline, ICI must be reliable, affordable, and sustainable. Meeting these requirements (especially sustainability) is a continued critical challenge, which will be the focus of my talk. More precisely, I will provide an overview of information and communication technology trends in light of various societal and environmental mandates followed by a review of technologies, systems, and hardware/software solutions required to create a sustainable ICI.

wednesday lunchtime keynote

Energy efficient computing

John Goodacre, ARM, UK

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

tuesday 19 march

EXECUTIVE SESSIONS

2.1 Advanced Technology Nodes: Dependency on Collaboration

Room - Oisans 1130-1300

Moderator:
Gary Smith,
Gary Smith EDA, US

Organiser:
Yervant Zorian,
Synopsys, US

Executives:
Maria Marced,
President - TSMC Europe, NL
Bipin Nair,
General Manager - Infotech, DE
Naveed Sherwani,
President, CoFounder & CEO - Open Silicon, US
Juan Rey,
Senior Director - Mentor Graphics, US
Raj Yavatkar,
Fellow - Intel, US

Abstract: The continuous technology scaling and new multi-die solutions are dramatically impacting the business performance of semiconductor industry. This may also significantly affect the dependency between eco-system players necessitating stronger collaboration and interdependency between them. The executives in this session will discuss upcoming changes in the semiconductor industry and their impact on collaboration between the foundries, design service and IP providers, EDA companies, and the rest of the value chain.

3.1 The Role of Prototyping in Today's SOCs

Room - Oisans 1430 - 1600

Organiser:
Yervant Zorian,
Synopsys, US

Executives:
Ivo Bolsens,
Senior Vice President & CTO - Xilinx, US
Joachim Kunkel,
Senior Vice President & GM - Synopsys, US
Sanjiv Taneja,
VP Product Engineering - Cadence, US

The widening gap between growing SOC complexity and designer productivity limits traditional system design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design, such as early investing in prototyping solutions. Executives in this session will discuss the role of prototyping and the new opportunities it may bring in designing today's complex chips.

4.1 Is reusing off-the-shelf Semiconductor IP possible today?

Room - Oisans 1700 - 1830

Organiser:
Yervant Zorian,
Synopsys, US

Moderator:
Peggy Aycinena,
EDA Weekly, US

Executives:
Christoph Heer,
Hear Design System & IP - Intel Mobile Communication, DE
Navraj Nandra,
Senior Director - Synopsys, US
James McNiven,
Vice President - ARM, UK

While today's SOCs systematically use a range of IP blocks, meeting end product requirements, such as power, performance and area, remain an obstacle on reusing off-the-shelf IP blocks. The speakers in this executive session will address the current trends and challenges in the semiconductor IP industry and discuss the level of customization versus reuse needed to meet today's SOC requirements.

wednesday 20 march

High-Performance Low-Power Computing

5.1 HOT TOPIC - System Approaches to Energy-Efficiency

Room - Oisans 0830-1000

Organiser:
Ahmed Jerraya - CEA-LETI-MINATEC, FR

At system level, energy consumption optimisation may be the most rewarding. Different approaches may be applied to improve energy efficiency. This Hot-Topic Session explores both system architecture and applications to reach better energy efficiency.

6.1 EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency

Room - Oisans 1100 - 1230

Organiser:
Ahmed Jerraya - CEA-LETI-MINATEC, FR

Traditionally HW-SW interfaces are defined twice using two different models: one representing HW from a SW point of view, and one representing SW from a HW point of view. These separate views create a discontinuity in the design process and inevitably induces non-optimised designs from an energy-efficiency point of view. This embedded tutorial presents a HW view, a SW view, and an integrated HW-SW view to study the different approaches to energy efficiency

7.0 Special Day Keynote

Room - Oisans 1330 - 1400

ENERGY-EFFICIENT COMPUTING

John Goodacre - ARM

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

7.1 HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency

Room - Oisans 1430-1600

Organiser:
Ahmed Jerraya, CEA-LETI-MINATEC, FR

The evolution of the semiconductor industry is allowing intensive computing on a single chip through heterogeneous and homogeneous architectures. This increase in compute density on a single chip is both a threat and an opportunity for energy-efficiency. This Hot-Topic Session presents different many-core SoC approaches to improve energy-efficiency.

8.1 HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency

Room - Oisans 1700-1830

Organiser:
Ahmed Jerraya, CEA-LETI-MINATEC, FR

SoC designs integrate an increasing number of heterogeneous programmable units (CPU, GPU, ASIP sub-systems), sophisticated interconnect, innovative memory architecture, and are using energy-efficient libraries that target advanced fabrication process technologies. This Hot-Topic Session presents the key challenges for aligning the most advanced fabrication technologies, FDSOI with circuit and architecture technologies to master energy-efficiency.

thursday 21 march

Special Day - Electronic Technologies for Smart Cities

9.1 HOT TOPIC: Smart Grid and Buildings

Room - Oisans 08:30 – 10:00

Organiser:
Luca Benini, Università di Bologna, IT

This session will provide a top-down view of energy management and optimization in Smart Environments, with emphasis on Buildings and grid-level integration. The first paper will focus on the design and computer-aided optimization of regional policies for generation, storage and distribution of sustainable energy. The second paper will give a holistic view of grids and building as cyber-physical systems and propose autonomic approaches for managing them. Finally, the third paper will look at design challenges for the distributed smart energy metering infrastructure, with the ultimate goal of reaching self-sustainability through energy harvesting

10.1 HOT TOPIC: Smart Data Centers Design and Optimization

Room - Oisans 1100-1230

Organiser:
David Atienza, EPFL, CH

This special session presents an overview of some of the hottest research topics towards the conception of future smart and energy-efficient datacenters. The first presentation explores the limits in the conception of highly dense datacenter infrastructures under current and future energy constraints. The second presentation presents smart energy-aware allocation techniques in virtualized datacenters to maximize the use of free cooling. The third presentation explores the limits of energy-efficient servers and resources utilization in next-generation computing systems for datacenters.

11.0 Smart Cities and Communities at the Regional, National and European Levels

Room - Oisans 1330 - 1400

Francesco Profumo, Italian Minister of Education, University and Research **and**
Genevieve Fioraso, French Minister for Higher Education and Research

11.1 HOT TOPIC: Smart Health

Room - Oisans 1400 - 1535

Organisers:
Daniela De Venuto,
Politecnico di Bari, IT

Alberto Sangiovanni Vincentelli,
University of California, Berkeley, US

The Smart Health session is about fundamental technical and scientific advances that may change radically the way healthcare is conceived today. Longer life expectation, aging, overweight and pollution are among factors that pose severe challenges to healthcare and its sustainability. Wireless devices, brain-machine interfaces, and cognitive process models may provide potential solutions to a vast array of problems involving clinical and human aspects, as well as economics and social issues. The presenters will introduce and discuss some aspects of devices and technologies that are essential in defining new approaches to healthcare and human well-being.

12.1 HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud

Room - Oisans 1600-1730

Organiser:
Ovidiu Vermesan, SINTEF, NO

The Internet of Energy (IoE) provides an innovative concept for power distribution, energy storage, grid monitoring and communication. It will allow units of energy to be transferred when and where it is needed. Power consumption monitoring will be performed on all levels, from local individual devices up to national and international level. In this context the new smart electric mobility vehicles will be integrated in the Internet of Energy, creating new mobile ecosystems based on trust, security and convenience to mobile/contactless services and transportation applications will ensure security, mobility and convenience to consumer-centric transactions and services. This special session/workshop will provide different views on the smart mobility concepts and future electric mobility trends by addressing the interaction with the smart city environments in creating an intelligent energy network platform for sustainable transportation systems.

friday 22 march

Friday Workshops

0730	**WORKSHOP REGISTRATION & WELCOME REFRESHMENTS**
BREAKS	**Please see individual workshop programmes for lunch and break times**

	Room – Meije 2	Room – Stendhal	Room – Oisans	Room – Chartreuse	Room – Bayard
0830 TO 1700	W1 ESCUG 2013: ESL - Putting the Pieces Together: Integrating SystemC Design and Verification with AMS and Algorithm Design	W2 1st RIIF Workshop - Towards Standards for Specifying and Modeling the Reliability of Complex Electronic Systems	W3 International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2013)	W4 Platform 2012 / STHORM embedded many-core acceleration	W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test

	Room – Berlioz	Room – Les Bans	Room – Belle-Etoile	Room – Meije 3	
0830 TO 1700	W6 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications	W7 Reconfigurable Computing V2.0: The Next Generation of Technology, Architectures and Design Tools	W8 Workshop on Industry-Driven Approaches for Cost-effective Certification of Safety-Critical, Mixed-Criticality Systems (WICERT)	W9 International Workshop on Software Approaches to Resilient System Design	

tuesday 19 march

2.8 HOT TOPIC: IP Subsystems: The next productivity wave?

1130 - 1300

Organisers:
Wido Kruijtzer - Synopsys, NL
Luciano Lavagno - Politecnico di Torino, IT

Chair:
Wido Kruijtzer - Synopsys, NL

Co-Chair:
Luciano Lavagno - Politecnico di Torino, IT

System-on-Chip (SoC) integrators have to deal with more and more complexity during integration of their architectures. For cost and time-to-market reasons, SoCs tend to be architected as a set of coarse-grain subsystems for recognized system functions like audio, video, connectivity, modem, etc. Such subsystem solutions consist of multiple integrated hardware IP blocks together with associated software. Till recently IP subsystems were mostly adopted internally within SoC integrators and were not yet available from traditional IP companies. However, in 2012 multiple companies announced the availabily of IP subsystem solutions. This special session will provide an update on the state-of-the art with regards to IP subsystems and review if IP subsystems indeed will be the way forward to boost productivity of SoC design.

3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug: Many Faces of the Same Coin?

1430 - 1600

Organiser:
Vikas Chandra - ARM, US

Chair:
Vikas Chandra - ARM, US

Co-Chair:
Kartik Mohanram - University of Pittsburgh, US

Complex SoCs of the future are subject to various sources of variability, reliability failures and design errors (logical or electrical) due to sheer design complexity, and marginal behaviors induced by uncertainties in manufacturing processes, temporal variability and operating conditions. In this session, we will cover this entire spectrum ranging from state-of-the-art techniques for manufacturability, variability and aging mitigation to effective post-silicon debug methods and everything in between.

4.8 EXHIBITION THEATRE: Testimonials

1700 - 1830

Organiser:
Jürgen Haase - edacentrum, DE

Chair:
Jürgen Haase - edacentrum, DE

In this session industrial testimonials will offer engineers an insight into good working practices and state-of-the-art design methods of market leaders. This sessions features design centering of IO in 28nm FDSOI technology, SoC power integrity verification with focus on analogue/mixed signal macros, data management for future SoCs and evolutionary computation for validation, testing and design automation.

wednesday 20 march

6.8 EXHIBITION THEATRE: Silicon Europe – Leading European Regions Join Forces

1100 - 1230

Organiser:
Jürgen Haase - edacentrum, DE

Chair:
Thomas Reppe - Silicon Saxony, DE

Four of the leading European micro- and nanoelectronics regions are joining their research, development and production expertise to form the transnational, research-driven cluster "Silicon Europe – The Leaders for Energy Efficient ICT Electronics". The cluster partners from Germany, Belgium, France and the Netherlands are linked by a common goal: They aim to secure and expand Europe's position as the world's leading center for energy efficient micro- and nanoelectronics and information and communications technology (ICT). In order to reach this goal, Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France) and High Tech NL (Eindhoven/Netherlands) are cooperating in research, development and business expertise. Together they represent about 800 research institutes and companies, which account for more than 150,000 jobs; among the companies are global market leaders such as Philips, NXP, Globalfoundries, Infineon, STMicroelectronics, Schneider Electric und Thales. This makes Silicon Europe one of the largest technology clusters of the world.

8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics

1700 - 1830

Organiser:
Erik Jan Marinissen - IMEC, BE
Ingrid Verbauwhede - KU Leuven, BE

Chair:
Steven Jeter - Infineon Technologies, DE

Co-Chair:
Ingrid Verbauwhede - KU Leuven, BE

Counterfeited ICs are an increasing problem. In 2011, a record high of 1,363 counterfeit-part incidents were reported world-wide, representing a $169B risk. Counterfeit incidents include the relatively straight-forward extra production at an outsourced manufacturing site for sales through alternative channels, but also the technically more advanced Trojan Horse "sniffer" ICs hidden in a 3D die stack of a telecom product. What can semiconductor suppliers do in technology, design, and test to assure that their customers get to use only genuine components in their systems?

thursday 21 march

10.8 PANEL: Will 3D-IC Remain a Technology of the Future... Even in the Future?

1100 - 1230

Organiser:
Marco Casale-Rossi - Synopsys, US

Chair:
Giovanni De Micheli - EPFL, CH

Co-Chair:
Marco Casale-Rossi - Synopsys, US

If asked "who needs faster planes?" the vast majority of the 2.75 billion airline passengers (source: IATA 2011) would say that they do need faster planes, and that they need them right now. Still, the commercial aircrafts cruising speed has remained the same – 800 km/hour – over the last 50+ years, and after the sad end of the Concorde project, neither Airbus nor Boeing are seriously working on the topic. Along the same lines, when asked "who needs 3D-IC?", most IC designers say that they desperately need 3D-IC to keep advancing electronic products performance, whilst addressing the needs of higher bandwidth, lower cost, heterogeneous integration, and power constraints. Still, 3D-IC continues to be the technology of the future. What are the road blocks towards 3D-IC adoption? Is it process technology, foundry or OSAT commercial offering, or EDA, or the business economics that is holding 3D-IC on the ground? In the introductory presentation of this panel session, LETI Patrick Leduc will illustrate the state-of-the-art of commercial, mainstream 3D-IC. EPFL Professor Giovanni de Micheli will moderate an industry and research panel, to understand what are the key factors preventing 3D-IC from becoming the technology of today.

11.8 EMBEDDED TUTORIAL: Advances in Asynchronous Logic: from Principles to GALS & NoC, Recent Industry Applications, and Commercial CAD Tools

1400 - 1530

Organiser:
Pascal Vivet - CEA-LETI, FR

Chair:
Robin Wilson - STMicroelectronics, FR

Co-Chair:
Beigné Edith - CEA-LETI, FR

The growing variability and complexity of advanced CMOS technologies makes the physical design of clocked logic in large Systems-on-Chip more and more challenging. Asynchronous logic has been studied for many years and become an attractive solution for a broad range of applications, from massively parallel multi-media systems to systems with ultra-low power & low-noise constraints, like cryptography, energy autonomous systems, and sensor-network nodes. The objective of this embedded tutorial is to give a comprehensive and recent overview of asynchronous logic. The tutorial will cover the basic principles and advantages of asynchronous logic, some insights on new research challenges, and will present the GALS scheme as an intermediate design style with recent results in asynchronous Network-on-Chip for future Many Core architectures. Regarding industrial acceptance, recent asynchronous logic applications within the microelectronics industry will be presented, with a main focus on the commercial CAD tools available today.

12.8 EMBEDDED TUTORIAL: Closed-Loop Control for Power and Thermal Management in Multi-core Processors: Formal Methods and Industrial Practice

1600 - 1730

Organiser:
Ibrahim Elfadel - Masdar Institute of Science and Technology, AE

Chair:
Petru Eles - Linköping University, SE

Co-Chair:
Jose Ayala - Complutense University of Madrid, ES

The objective of this embedded tutorial is to bring DATE attendees who are interested in low-power design for MPSoC to the forefront of the latest academic research and industrial practice in the area of closed-loop control of power and temperature in MPSoC. Starting with power capping techniques based on classical control theory, the tutorial will cover the more advanced techniques of optimal control, model predictive control, and adaptive control. Practical issues such as power and thermal proxies, power and thermal sensors, and various actuation techniques will be surveyed. Furthermore, the tutorial will cover recent techniques for pro-active and reactive closed-loop temperature control for 2D and 3D MPSoC, including the handling of emerging inter-tier liquid cooling techniques. It will also address optimal power control techniques in NoC architectures, with particular attention to methods for handling multiple voltage and clock domains under variable workloads. Important emerging problems such as heterogeneity of the computational fabric and scalability of the control methods will also be discussed along with their emerging solutions.

The DATE 13 conference programme allows generous opportunities for delegates to visit the exhibition and attend the presentations in the exhibition theatre.

COFFEE & LUNCH BREAKS

Delegate coffee will be served in the main exhibition hall. Lunch is available in Room Ecrins on the lower ground floor (on Tuesday the sandwich lunch is also available in Auditorium Dauphine for those wishing to attend the open special lunch session) and in the exhibition hall there is a cash bar for visitors and exhibitors.

Tuesday 19 March

Morning Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Afternoon	1600 – 1700

Wednesday 20 March

Morning Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Afternoon	1600 – 1700

Thursday 21 March

Morning Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Afternoon	1530 – 1600

Evening Reception offered by the City of Grenoble

1830-1930 - Tuesday 19 March

DATE PARTY at the WTC

1930 - Wednesday 20 March

This year the DATE party will take place in the World Trade Centre, Grenoble. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 75 Euros each

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – www.date-conference.com

Day	Time	Meeting & Contact	Room	Type
Mon	1300-1700	**Challenges in Design and Qualification for Automotive Electronics** Michael Nicolaidis, Rubin Parekhji <parekhji@ti.com>	7 Laux 4	Open
Mon	1900-2100	**EDAA PhD Forum** Peter Marwedel <peter.marwedel@tu-dortmund.de>	Salle de Reception	Open
Tues	1300-1430	**ETTTC Meeting** Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Bayard	Open
Tues	1830-1930	**EDAA General Assembly** Georges Gielen <georges.gielen@esat.kuleuven.be>	7 Laux 4	Open
Tues	1830-2130	**European SystemC Users Group Meeting** Axel Braun <abraun@informatik.uni-tuebingen.de>	Meije	Open

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INTERACTIVE PRESENTATIONS

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the Exhibition Hall in 30-minute time slots during exhibition and coffee breaks.

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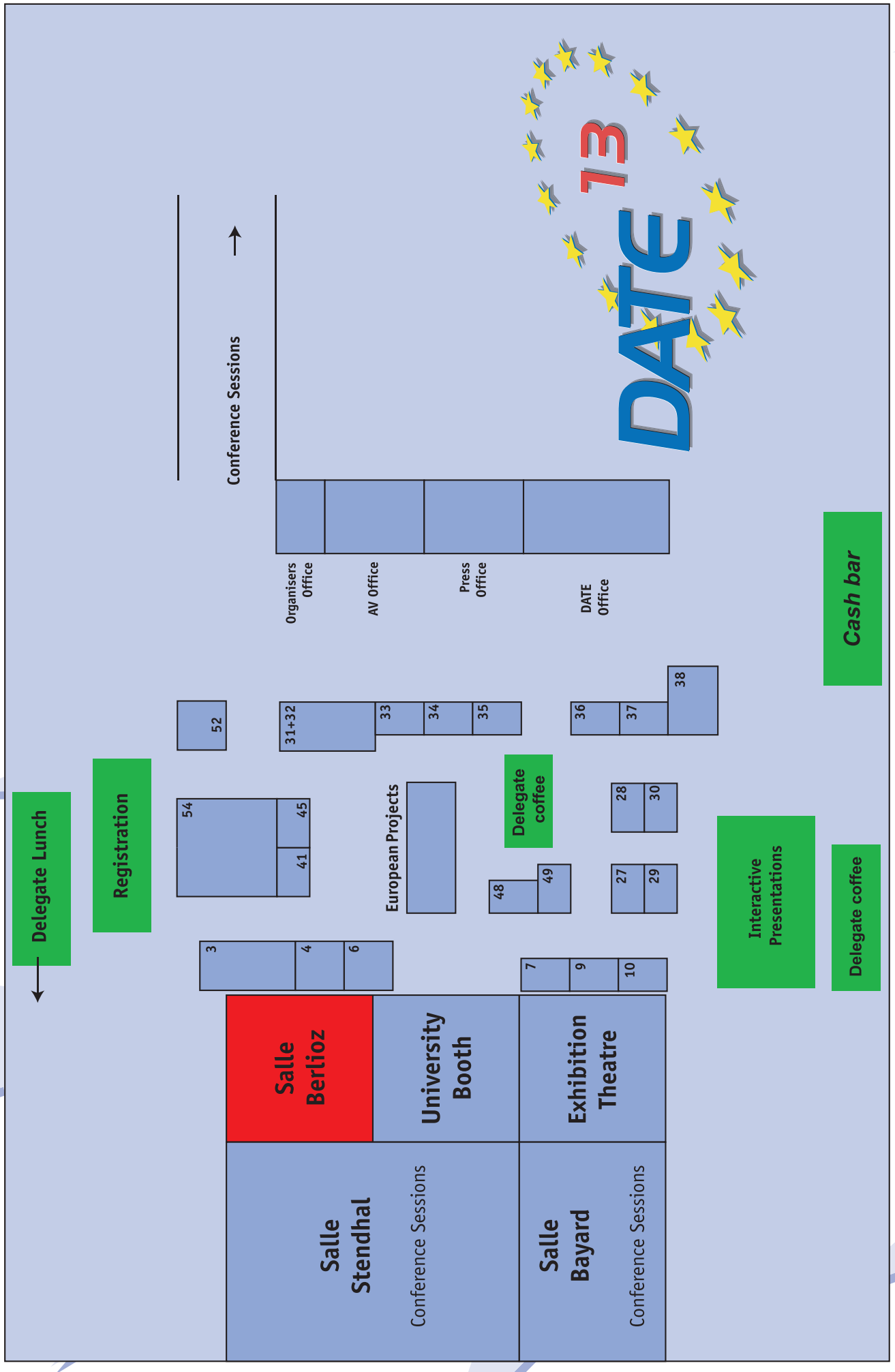
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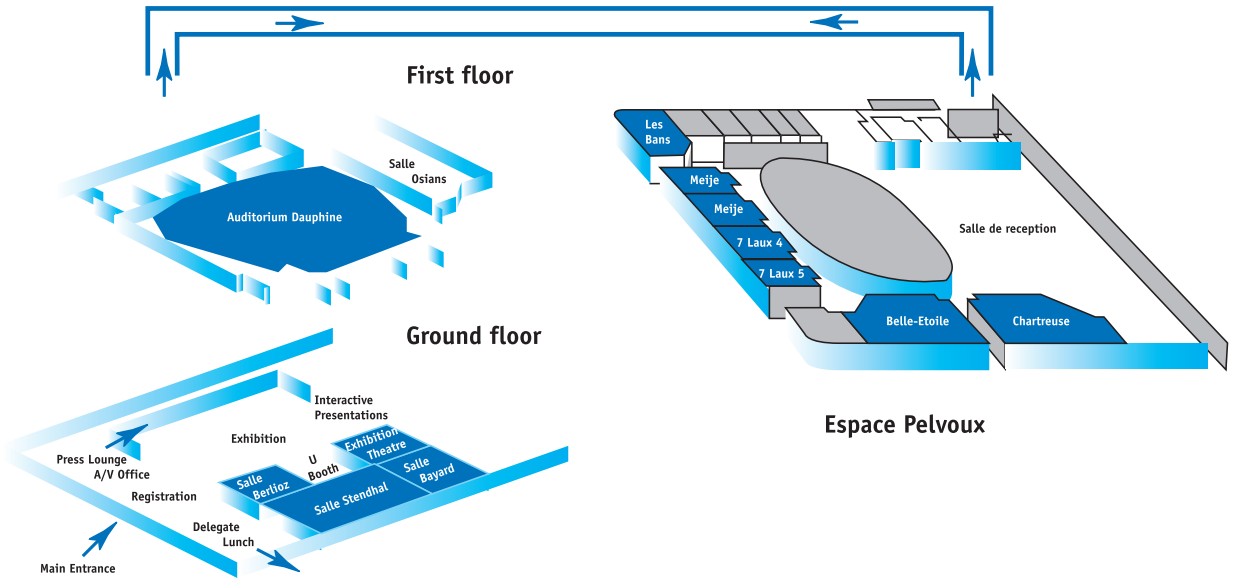

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50 DAC

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The Design Automation Conference (DAC) is the leading technical conference and tradeshow on electronic design, design automation, embedded systems and software. It is where IC Design and the EDA ecosystem learns, networks, and conducts business. DAC features over 300 presentations consisting of technical sessions, panels, exciting keynotes, tutorials, workshops and co-located events covering the latest in design methodologies, embedded software and EDA tool developments. The exhibition offers booths and suites from over 175 of the leading EDA, IP, embedded systems and design services providers. 50th DAC, June 2 – 6, 2013, Austin Convention Center. www.dac.com.

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ApS Brno Ltd., Codasip Division

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We are a small company that provides an all-in-one development environment for application processors and ASIP design services. Our Codasip® Framework enables designers to create the most effective Application-Specific Instruction-set Processors (ASIPs) for both the target applications, and the application domain. Our customized Codasip® Framework outperforms related Synopsys and Cadence development tools in many aspects. Through the use of Codasip® Framework you will shorten development time substantially and you will deliver higher performance ASIPs. Codasip® Framework incorporates the innovative feature of the automated generation of the OVM based functional verification. As a result of this unique functionality, designers utilize fluent flow from the processor specification to the validation of the generated C/C++ compiler when compared to the generated synthesizable RTL. The time savings are achieved through the automation of tasks that would otherwise be done manually, including the fully automatic generation of the programming and simulation toolchain, and the generation of the synthesizable RTL and support of functional verification.

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Semiconductor IP:
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On-Chip Bus Interconnect
On-Chip Debug
Processor Platforms
Application-Specific IP:
Digital Signal Processing
Multimedia Graphics

stand 10

Blue Pearl Software

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We are excited to announce Release 6.0 of Blue Pearl Software Suite which includes comprehensive RTL analysis, clock-domain crossing (CDC) checks, and automatic SDC generation for SoC designs. Blue Pearl Software Suite is easy to use for any level of ASIC/FPGA designers.

Our Software Suite which runs on Windows and Linux, offers multi- language (Verilog, SystemVerilog and VHDL) support, and supports major synthesis flows. Designers can mix and match hardware languages in the same design with language checking that matches downstream tools. Its visualization and validation technology gives immediate feedback for validating its automatically generated timing constraints.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry

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CEA LETI

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Leti is an institute of CEA, a French research-and-technology organization with activities in energy, IT, healthcare, defence and security. Leti is focused on creating value and innovation through technology transfer to its industrial partners. It specializes in nanotechnologies and their applications, from wireless devices and systems, to biology, healthcare and photonics. NEMS and MEMS are at the core of its activities. An anchor of the MINATEC campus, CEA-Leti operates 8,000-m² of state-of-the-art clean room space on 200mm and 300mm wafer platforms. It employs 1,700 scientists and engineers including 240 Ph.D. students and 200 assignees from partner companies. CEA-Leti owns more than 1,880 patent families.

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RF Design
System-Level Design:
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Physical Analysis
Acceleration & Emulation
Hardware/Software Co-Design
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CimAlpes

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Shared Service Platform for Micro-electronic and Embedded Software Design CimAlpes focuses on SMEs and startups seeking access to EDA and embedded software design tools for usage patterns that do not justify the purchase or lease of costly annual licenses. From a practical standpoint, CIME Nanotech provides the facilities and infrastructures allowing companies to use the EDA tools and computing infrastructure already installed and preconfigured. The time for a company to be fully operational is therefore considerably shortened. In addition, Minalogic ensures that start-ups and SMEs are aware of the added value provided by CimAlpes and how it significantly reduces the time and cost devoted to design micro-nanoelectronics systems. Moreover, the access to design kits can be hosted by CMP which offers various MPW runs. CimAlpes offers users special rates that include an annual membership that depends on the size of the company and variable rental cost based on their usage time (pay per use model). The list of tools made available by the EDA partners as well as the access conditions (rates and terms of use) are available on our Internet site http://cimalpes.minalogic.com.

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CMP: Circuits Multi-Projects

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CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production.
Since 1981, more than 1000 Institutions from 70 countries have been served, more than 6700 projects have been prototyped through 800 manufacturing runs, and 60 different technologies have been interfaced.
Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and AMS down to 28 nm FDSOI, 3D-IC from TEZZARON/GLOBALFOUNDRIES, and 150nm pHEMT GaAs from TRIQUINT. ARM IP cores are available on 130nm µ and 65 nm CMOS.
MEMS are available on various processes: specific MEMS technologies (PolyMUMPS, SOIMUMPS, MetalMUMPS from MEMSCAP) and bulk micromachining.
Design kits for most IC CAD tools and Engineering kits for MEMS are available.
Assembling is provided in a wide range of plastic and ceramic packages.

PRODUCT FINDER

Services:
Prototyping
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stand EP4

COMPLEX - COdesing and power Management in PLatform-based design space EXploration

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Website: complex.offis.de

The primary objective of the COMPLEX (COdesing and power Management in PLatform-based design space EXploration) European Integrated Project has been to develop an innovative, highly efficient and productive design methodology and a holistic framework for iteratively exploring the design space of embedded HW/SW systems. COMPLEX focussed on early, fast yet accurate platform-based design space exploration at the system level.
The COMPLEX consortium has developed a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and assessment of the platform at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle.
Partners: OFFIS (DE), STMicroelectronics (IT), STMicroelectronics (CN), Thales Communications (FR), GMV (ES), Synopsys (BE), EDALab (IT), Magillem Design Services (FR), Politecnico di Milano (IT), Universidad de Cantabria (ES), Politecnico di Torino (IT), IMEC (BE), ECSI (FR)

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Behavioural Modelling & Analysis
Hardware/Software Co-Design

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Concept Engineering GmbH

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Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, FPGA and IC designers.
Nlview WidgetsTM – a family of schematic generation and visualization engines (Tcl/TK, MFC, Qt, Java, Perl/Tk, wxWidgets) that can be easily integrated into EDA tools.
RTLVisionTM PRO – a graphical debugger for SystemsVerilog, Verilog and VHDL based designs.
GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and

EDIF based designs.
SpiceVision® PRO – a customizable debugger for SPICE based designs.
SGvisionTM PRO – a customizable mixed-mode debugger (SPICE and Verilog).
StarVisionTM PRO - a customizable mixed-signal and mixed-language debugger.

PRODUCT FINDER

ASIC and SOC Design:
Verification
Analogue and Mixed-Signal Design
Test:
Mixed-Signal Test

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CST - Computer Simulation Technology AG

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CST develops and markets high performance software for the simulation of electromagnetic fields in all frequency bands. Its products allow you to characterize, design and optimize electromagnetic devices all before going into the lab or measurement chamber. This can help save substantial costs especially for new or cutting edge products, and also reduces design risk and improves overall performance and profitability. Its success is based on the implementation of leading edge technology in a user-friendly interface. Furthermore, CST's "complete technology" complements its market and technology leading time domain solver (CST MICROWAVE STUDIO®), thus offering unparalleled speed, accuracy and versatility for all applications. CST's customers operate in industries as diverse as Telecommunications, Defense, Automotive, Electronics, and Medical Equipment, and include market leaders such as IBM, Intel, Mitsubishi, Samsung, and Siemens. CST markets its products worldwide through a network of distribution and support centers which also provide comprehensive customer support and training.
More information at http://www.cst.com.

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Package Design
PCB & MCM Design
Test:
Design for Test
Embedded Software Development:
Software/Modelling

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DeFacTo Technologies

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DeFacTo Technologies provides innovative and non-intrusive EDA solutions to help achieving "Design & DFT" closure at RTL by delivering a high quality suite of tools which cover IP Integration, Design Verification & DFT Signoff needs.

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ASIC and SOC Design:
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Test:
Design for Test
Test Automation (ATPG, BIST)
Boundary Scan

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Design and Reuse

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DOCEA Power

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DOCEA Power develops and markets dedicated system-level tools for modeling and optimizing power/thermal behavior of whole electronics systems. DOCEA's Aceplorer software offers a framework to capture all power related data in a single environment and integrates a consistent methodology for modeling and simulating the power behavior of electronics systems, from SoCs, to systems-in-package and complete boards. The "separation of concerns" approach makes Docea's standalone power models usable across teams and project stages from system level early measurements, to power budget tracking and to silicon validation.
The Aceplorer innovative platform is the solution for early power estimation, architecture and power management strategies exploration, use case profiling, package selection and other technology choices that are impacted by power consumption and thermal distribution. Dealing with power and/or thermal issues with Docea Power solutions at system level is fast, secure and efficient.
DOCEA technology has been adopted by world's largest semiconductor companies as well as major system integrators in the mobile communications industry.

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Dolphin Integration

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Website: www.dolphin.fr/product_offering.html

Dolphin Integration (www.dolphin-ip.com) is a developer and marketer of virtual components of Intellectual Property partaking in the design of multi-domain Integrated Circuits with a focus on Systems-on-Chip and MEMS with micromechanical structures. The range of products includes:
* a handful of microprocessors in synthesizable logic VHDL or Verilog around the Flip8051,
* the library of standard cells with generators of embedded RAMs and ROMs, down to 65 nm, patented for high density and low power-consumption, with the unique advantage to enable Back-Tracking Free Placement and Routing,

* as well as Virtual Components for high resolution for Voice and Audio applications such as Portable Multimedia Players, and Sensors for high resolution measurements. Their secret weapon is multi-level simulator SMASH All-in-1, the best VHDL-AMS solution with its powerful add-ons for Multi-Domain Modeling.
The company has been active since 1985 and has received the ISO-9001: 2000 certification.

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EDA Solutions LTD

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For over 10 years EDA Solutions have provided cost effective and highly productive IC Design software and manufacturing services to European industry. Visit us on Stand 7 to find out more about the digital synthesis tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the MPW and low volume production services from MOSIS.

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EDXACT

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Website: www.edxact.com

EDXACT focuses on design tools aimed at physical design and verification of Integrated Circuits, with a specialization on questions related to netlist parasitics and their impact on simulation time, signal integrity, delay, crosstalk and other.
EDXACT is best known for netlist reduction technology JIVARO, offering additional dedicated analysis tools BELLEDONNE and VISO.
http://www.edxact.com

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Elsip

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"SoC Memory Management made easy"

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Europractice

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The EUROPRACTICE IC service offers low cost and easy access to ASIC prototype and small volume fabrication.
The service is offered by IMEC (B) and FhG/IIS (D).
Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW (Multi Project Wafer) runs whereby many designs from different customers are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemi, austriamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC.
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stand 54

Grenoble-Isère/AEPI

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AEPI is the economic development agency for Grenoble-Isere/France. The Grenoble area, smart valley in southeastern France, is Europe's top center in micro-nanotechnologies and derived applications, and home of the program Nano2012, representing over 2.3 billion investment on the Crolles STMicroelectronics site. Working closely with Minatec-CEA-Leti as well as the industrial cluster Minalogic, AEPI provides complimentary information and services to companies exploring business opportunities.

AEPI is also a member of the local board of the Semi Europe Grenoble office, located on the Minatec Campus, and is an active supporter of the European cooperation between Silicon Saxony and Grenoble microelectronics clusters.

stand EP1

HiPEAC NoE

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Website: www.hipeac.net

The HiPEAC network of excellence (i) steers to increase the European research in computing systems; (ii) improves the quality of such research, (iii) and creates a visible and integrated pan-European community in computing systems. The membership program aims at growing the network. It creates a vibrant industrial membership and reaches out to companies and academics in the new member states and beyond. The mobility program brings the partners and the members closer together by funding one-to-three month internship exchanges, collaboration grants, mini-sabbaticals and by organizing networking events. The research coordination program aims at coordinating the joint research between the HiPEAC members. A tangible result of the research coordination is the bi-annual HiPEAC vision. The visibility program manages all the public activities of the network such as an annual conference, the summer school, the HiPEAC website, a quarterly newsletter and the award program.

stand 7

Incentia

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Incentia Design Systems, Inc. is a leading provider of advanced Timing and Signal Integrity Analysis, Design Closure, and Logic Synthesis software for multi-million-gate nanometre designs. Incentia patented technologies provide the fastest Static Timing Analysis (STA) tool in the market today.

Incentia's products are in use at leading semiconductor, fabless IC design, systems, and design service companies worldwide and have produced numerous customer tape-outs, including those using advanced 40nm technologies and designs over 50 million gates. Incentia are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

ASIC and SOC Design:
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Test:
Design for Test
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan

stand EP5

MADNESS - Methods for predictAble Design of heterogeneous Embedded Systems with adaptivity and reliability Support

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E-Mail: request@madnessproject.org
Website: www.madnessproject.org

The main goal of the project is to define innovative methodologies for system-level design, able to guide designers and researchers to the optimal composition of embedded MPSoC architecture, according to the requirements and the features of a given target application field.
The proposed methodologies will extend the classic concept of design space exploration to:
• Improve design predictability, bridging the so called "implementation gap", i.e. the gap between the results that can be predicted during the system-level design phase and those eventually obtained after the on-silicon implementation.
• Consider, in addition to traditional metrics (such as cost, performance and power consumption), continued availability of service, taking into account fault resilience as one of the optimization factors to be satisfied.
• Support adaptive runtime management of the architecture, considering, while tailoring the architecture, new metrics posed by novel dynamic strategies and advanced support for communication issues that will be defined.

Partners: Università degli Studi di Cagliari (IT), Università della Svizzera italiana (USI), Silicon Hive (NL), Lantiq (DE), University of Amsterdam (NL), University of Leiden (NL), Informatik Centrum Dortmund (DE).

stand 54

Minalogic

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FRANCE
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E-Mail: contact@minalogic.com
Website: www.minalogic.com

Minalogic brings together the Rhône- Alpes region's leading innovators in the field of smart miniaturized systems. By leveraging the Grenoble area's synergies between research, higher education, and industry, we have achieved a global leadership position in smart embedded systems. Our cluster actively facilitates networking among innovators, manufacturers, and investors to get new technologies to market quickly. The technologies developed at the cluster are applicable to all business sectors, including more traditional industries. The role of Minalogic is to respond to the business community's need to identify new value-added services that can be integrated into existing products in fields that include health care, the environment, mobility, the media, and the textile industry.

stand 7

MOSIS

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MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world. Processes offered include SOS, SOI, CMOS and SiGe BiCMOS, in

geometries from 0.7um to 32nm, from the foundries IBM, TSMC, ON Semiconductor, austriamicrosystems, Globalfoundries, and Peregrine. MOSIS are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

Services:
Prototyping
Foundry & Manufacturing

stand 48

MunEDA

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MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

stand 35

Nano-Tera.ch

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Website: www.nano-tera.ch

Nano-Tera.ch is a Swiss national program supporting research in multi-scale system engineering for heath, security, energy and the environment. The broad objectives of the program are to improve quality of life and security of people and to create innovative products, technologies and manufacturing methods, thus resulting in job and revenue creation.
Launched officially in February 2008, with the first projects starting in March 2009, Nano-Tera.ch is now a strongly established program that is currently funding 75 research projects, including 19 RTD (Research, Technology, Development) projects, for a total budget of about 123 MCHF.

The research involves more than 700 researchers and 31 Swiss research institutions, yielding about 575 publications and 1000 presentations in conferences and workshops, as well as several presentations in the media. 30 industrial partners are involved in the projects and a total of 15 patent applications have been filed so far.

stand 27

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Publishers of the highly acclaimed FOUNDATIONS AND TRENDS journals. Peer-reviewed surveys, reviews and tutorials in electronic design automation. Visit our booth to browse the available titles and meet the publisher. All print titles available for the special DATE price of €35.
www.nowpublishers.com/eda

Semiconductor IP:
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On-Chip Debug
Physical Libraries
Processor Platforms
Synthesizable Libraries
Test IP
Verification IO
Application-Specific IP:
Analogue & Mixed Signal IP
Data Communication
Digital Signal Processing
Multimedia Graphics
Networking
Security
Telecommunication
Wireless Communication

stand 49

OneSpin Solutions GmbH

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Electronic design automation (EDA) supplier OneSpin Solutions of Munich, Germany, was founded in 2005 as a spin-off from Infineon Technologies AG. It leverages more than 300 engineer-years of formal verification technology development and application service experience to enable design teams to avoid costly redesigns and respins, while dramatically cutting their verification effort and costs and time-to-market pressures. Market-leading telecommunications, automotive, consumer electronics, and embedded systems companies rely on OneSpin to reduce their verification effort and achieve the industry's highest possible verification quality.

stand EP6

PHARAON – Parallel and Heterogeneous Architectures for Real-time ApplicatiONs

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The PHARAON project is a European collaborative initiative between universities, research labs and industrials. It is sponsored by the European Commission that supports part of the costs and assists partners in the project management. The main objective of PHARAON is to improve competitiveness of the European embedded electronic industry, especially with respect to reducing power consumption and improving performance, by providing new paradigms for multicore architectures programming, monitoring and control, as well as new dynamic power adaptation strategies, algorithms and interfacing standards. Raising the expertise of European industry in system architecture, software development and power management is crucial to ease the transition to multicore platforms. It will enlarge the range of applicability of a hardware platform and plays in favour of re-use, cost and time-to-market reduction, which have become crucial requirements in a worldwide competition.
Partners: Thales Communications & Security, Politecnico di Torino, IMEC, University of Cantabria, ENS, Tedesys, Vector Fabrics

Interactive Presentations
will be held in the Exhibition Hall in 30-minute time slots during exhibition and coffee breaks.

stand 54

Presto Engineering

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Presto Engineering has been created in 2006 (San Jose, California) and has now global hubs in USA, Israël and Europe (Grenoble and Caen). Presto Engineering is a global engineering services provider for the overall microelectronics industry from discrete to complex IC's. Our focus is in RF and high-speed communications and we provide Turn-key Production solutions. From design of our customers, we deliver Test Engineering, Characterization, Qualification and Failure Analysis. We also support Test Production, Assembly, Yield Management and Turn-Key Solution with wafer fab foundries. Presto Engineering provides also Consulting Services including Audits (tier party Audits, Manufacturing lines,...), Consulting and Assistance, Training (FA techniques,...). Different platforms are available in Presto Engineering to perform Test Engineering and Characterization (V93K Verigy, LTX X-Series MX, µFlex Teradyne,...). We handle all the tests needed for a qualification (HTOL, HAST, TMCL,...). Our team supports also the hardware development for these Test and qualification fields. We have all the techniques needed for FA in order to address the most advanced technologies. Presto Engineering is ISO9001:2008 certified and COFRAC ISO17025:2005 accreditated.

stand EP3

SEEMPubs

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Politecnico di Torino, with over 27.000 students, is the second largest technical university in Italy. The workforce dedicated to research and teaching includes around 900 Professors, 700 PhD Students and 300 Research Assistants, covering all major areas of the engineering and architecture disciplines.

stand 54

Serma Technologies

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Website: www.serma-technologies.com/en

Serma Technologies is an FA Laboratory and a Test house Company (170 people) located in Paris, Bordeaux and Grenoble and part of the Serma Group (670 people, 80 Million Euros Turnover). The company offer services such as: - Test Program Development including DfT - Test Production - Supply Chain Management - Environmental & ESD Qualification according to standards (JEDEC, MIL, AECQ100). - Failure Analysis (Wafer, Die, Component, System).

PRODUCT FINDER

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal)
System-Level Design:
Physical Analysis
Hardware/Software Co-Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Training
Application-Specific IP:
Security

stand 9

Solvertec

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solvertec is an EDA start-up that responds to the biggest bottleneck in the design of digital integrated circuits: the localization and fixing of bugs (debugging). solvertec's next generation RTL debugging tool Debug!t reduces the time-to-market of chip designs by adding automated analysis for bug localization and bug fixing to basic debugging functionalities. Debug!t automatically pinpoints bug locations in HDL code, classifies bug locations, checks bug responsibility of third party IP, provides explanations and hints to fix and assigns bugs to the respective chip design engineers.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Hardware:
FPGA & Reconfigurable Platforms

stand 31 + 32

SPRINGER

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Springer is one of the world-leaders in book publishing, boasting a broad range of subject matter, and a history of working with the most prestigious scholars in the field. Additionally, Springer publishes an astute collection of Journals, with a track record of generating the latest sought after content. For additional information about all our engineering publications, please stop by our booth, or visit us at springer.com

stand 7

Tanner EDA

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Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. Tanner are represented in Europe by EDA Solutions, who

will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
Test:
Silicon Validation
Mixed-Signal Test

stand 3

Target Compiler Technologies

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Target Compiler Technologies is the leading provider of retargetable software tools for the design, programming and verification of application-specific processor cores (ASIPs). ASIPs are key building blocks of single- and multi-core systems-on-chip (SoCs) that power today's electronic systems. IP Designer, Target's flagship product, enables the design of ASIPs with performance and energy characteristics close to hardwired datapaths. Yet these ASIPs provide software programmability, thus permitting changes in specifications and extending the revenue lifetime of SoCs. IP Designer supports ASIP architectural exploration, and generates a complete C compiler based software development kit as well as a low-power hardware implementation for each ASIP. The tools have been used by customers around the globe to design SoCs for 2G/3G/4G handsets, cordless and VoIP phones, audio/video/image processing, infotainment and security for cars, DSL modems, DSL access multiplexers, wireless LAN, hearing instruments, and personal health-care systems. Target is also introducing MP Designer, a new tool for multicore parallelisation and design in an SoC context.
URL: www.retarget.com

DATE PARTY
See page 8

stand 30

The IET

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The IET is europe's largest professional body for engineers and technologists, we offer a wide range of products, services and professional qualifications to keep you ahead of the game. With 150,000 members based in 127 countries networking is key to their and your success - find out how to join and be part of the Knowledge Network by visiting us at our stand or visit www.theiet.org

stands EP2

TouCHMore

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Politecnico di Torino is an engineering university based in Turin, northern Italy. Established in 1859, Politecnico di Torino is Italy's oldest Technical University. It is one of the top technical universities in Italy. TOUCHMORE is coordinated by the Department of Computer and Control Engineering. In particular, EDA research group inside DAUIN has expertise in system level design, energy and performance optimization of multicore platforms with thermal and process variability constraints.
http://www.touchmore-project.eu

stand 46

University Booth

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university-booth@date-conference.com
Website: date-conference.com/group/exhibition/u-booth

The University Booth is part of the DATE program and is sponsored by the DATE Sponsor Society. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot. The University Booth is organized by Laurent Fesquet (TIMA) and Andreas Vörg (edacentrum).

stand 54

UXP

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UXP is a designer, developer and integrator of its own technologies in advanced automation solution, industrial data processing and real-time embedded systems. UXP develops product systems (hardware and software) to build open systems in the fields of Building management systems, Energy, Embedded systems, construction and public works, and Industry.

stand EP8

WiserBAN

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stand 54

XYALIS

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Website: www.xyalis.com

XYALIS introduces its new highly parallel CMP metal fill engine at the Date Conference, GTstyle.
The new GTstyle release has been successfully used on a multi-billion transistor processor design using TSMC 28nm process, in a few hours, allowing metal fill to be run as part as the design flow.
XYALIS will also present its proven integrated Mask Data Preparation solution automating frame generation, multichip assembly, mask set creation, and mask order form management, which shortens time to manufacturing, increases yield, and removes errors during mask and wafer production.

DATE 14

Conference and Exhibition
March 24-28, 2014
ICC, Dresden, Germany

Preliminary Call for Participation

Scope of the Event

The 17th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. **More details are given on the DATE website (www.date-conference.com).**

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling

- Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems "

Submission of Papers

All papers have to be submitted electronically by Friday September 13, 2013 via: http://www.date-conference.com/ Papers can be submitted either for standard oral presentation or for interactive presentation.

Event Secretariat

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