DATE 2013
Monday
Tutorials

Tutorials Chair
Franco Fummi - Università di Verona – Italy

http://www.date-conference.com

February 24, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

Summary

Tutorial A

Design Automation of Electronic Systems: Past accomplishments and Challenges Ahead A Tribute to Robert Brayton

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

A: Design Automation of Electronic Systems: Past accomplishments and Challenges Ahead A Tribute to Robert Brayton

Full-day	Topic: Design	Room Belle-Etoile
Organizer:	Tiziano Villa	Università di Verona - Italy
Speakers:	Jacob White	MIT - USA
	Jaijeet Roychowdhury	University of California at Berkeley - USA
	Masahiro Fujita	University of Tokyo – Japan
	Jordi Cortadella	Universitat Politecnica de Catalunya - Spain
	Victor Kravets	IBM - USA
	Rajeev Murgai	Synopsys - India
	Igor Markov	University of Michigan - USA
	Ken McMillan	Microsoft - USA
	Sanjit Seshia	University of California at Berkeley - USA
	Giovanni De Micheli	Ecole Polyt. de Lausanne - Switzerland
	Douglas Densmore	Boston University - USA
	Rupak Majumdar	University of California at LA - USA
	Alexandre Petrenko	CRIM - Canada
	Luca Carloni	Columbia University - USA
	Alberto Sangiovanni-Vincentelli	University of California at Berkeley - USA
	Robert Brayton	University of California at Berkeley - USA

Description

This tutorial brings together world-wide experts in Computer-Aided Design of Electronics Systems to assess past successes and present challenges in electronic design automation (EDA). This event will celebrate the scientific contributions of Prof. Robert Brayton who has been since many decades a major driving force for all fields of EDA in industrial and academic research. Prof. Brayton, who is still an active researcher at UC Berkeley, will turn eighty in 2013. The tutorial will be a unique opportunity for the EDA community to get a perspective on the major directions of development, past and future.

Detailed program

8:15-8:30: Opening Session

8:30-9:30: Simulation and Circuit Design:

- EDA beyond Electronics: Anecdotal Evidence in Systems Biology, MRI Optimization, and Electric Vehicle Simulation (Jacob White)
- Phase Logic Using Self-Sustaining Nonlinear Oscillators (Jaijeet Roychowdhury)

9:30-11:00: Logic Synthesis and Computer Architecture:

- Towards the Unification of Synthesis and Verification in Logic and Architectural Design (Masahiro Fujita)
- From 2-Level to Architectural Synthesis: a Long Trip for Design Automation (Jordi Cortadella)
- Decomposition of Boolean Expressions 30 Years After the First Algebraic Factoring Algorithm (Victor Kravets)

11:00-12:00: Physical Design and Timing Analysis:

- Space (and Physical Design): the Final Frontier for VLSI (Igor Markov)
- Technology-Based Logic Transforms (Rajeev Murgai)

12:00-13:00: Lunch

13:00-14:00: Formal Verification and Equivalence Checking:

- Combining Algorithms to Solve Intractable Problems (Ken McMillan)
- Integrating Induction and Deduction for Verification and Synthesis (Sanjit Seshia)

14:00-15:00: New Frontiers of EDA:

- New Frontiers of Logic Design Tools (Giovanni De Micheli)
- Bio-Design Automation: Designing Genetic Circuits with EDA Principles (Douglas Densmore)

15:00-16:00: Formal Models:

- Error Localization using Maximal Satisfiability (Rupak Majumdar)
- The Unknown Component Problem (Alexandre Petrenko)

16:00-17:00: System Design:

- From Latency-Insensitive to Communication-Based System-Level Design (Luca Carloni)
- EDA: the Last 40 Years and the next 20 Years (Alberto Sangiovanni-Vincentelli)

17:00: Conclusions (Robert Brayton)

Robert Brayton

Robert Brayton received the BSEE degree from Iowa State University in 1956 and the Ph.D. degree in mathematics from MIT in 1961. He was a member of the Mathematical Sciences Department of the IBM T. J. Watson Research Center until he joined the EECS Department at Berkeley in 1987. He held the Edgar L. and Harold H. Buttner Endowed Chair and retired as the Cadence Distinguished Professor of Electrical Engineering at Berkeley.

He is a member of the US National Academy of Engineering, an IEEE Fellow, and has received the following awards: IEEE Guilleman-Cauer (1971), ISCAS Darlington (1987), IEEE CAS Technical Achievement (1991), IEEE Emanuel R. Piore (2006), ACM Kanallakis (2006), European DAA Lifetime Achievement (2006), EDAC/CEDA Phil Kaufman (2007), D.O. Pederson best paper in Trans. CAD (2008), ACM/IEEE A. Richard Newton Technical Impact in EDA (2009), Iowa State University Distinguished Alumnus (2010), SRC Technical Excellence (2011) and ACM/SIGDA Pioneering Achievement (2011).

He has co-authored over 460 technical papers, and 11 books in the areas of the analysis of nonlinear networks, simulation and optimization of electrical circuits, logic synthesis, and formal design verification.

Tutorial B

Advanced Techniques for Power-Aware System-Level Prototyping

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

B: Advanced Techniques for Power-Aware System-Level Prototyping

Full-day	Topic: System design	Room Les Bans
Organizers:	Frank Oppenheimer	OFFIS - Germany
	Eugenio Villar	Universidad de Cantabria - Spain
	Adam Morawiec	ECSI - France
	Philipp A. Hartmann	OFFIS - Germany
Speakers:	Eugenio Villar	Universidad de Cantabria - Spain
	Davide Quaglia	EDALab - Italy
	Emmanuel Vaumorin	Magillem - France
	Francisco Ferrero	GMV AD - Spain
	Carlo Brandolese	Politecnico di Milano - Italy
	Philipp A. Hartmann	OFFIS - Germany
	Sara Bocchio	STMicroelectronics - Italy

Description

In the design of embedded systems extra-functional properties like timing and power need to be considered during the entire design process. Often these properties can only be estimated after manually implementing a design for a certain target platform and using component-level timing and power analysis tools. At the same time, exploration, analysis, and optimization of embedded applications running on today's platforms require fast and early virtual system models enabling the consideration of extra-functional properties under real-world application scenarios.

With a group of experts from industry and academia, the tutorial discusses the major challenges and presents novel and innovative research results including tool support to create timing and power-aware Virtual Platforms. In this context, the following key aspects are covered:

- Model-driven design and automatic platform performance and power model synthesis, enabling early design space exploration,
- efficient application mapping onto resource-constrained platform models,
- early and automatic timing and power estimation for embedded software and custom hardware components, suitable for integration into Virtual Platform models,
- RTL-to-TLM re-synthesis and abstraction of timing and power properties, suitable for integration into Virtual Platform models

The presentations will be accompanied by concrete tool introductions and demonstrations, showing how the presented concepts support improvement of today's state-of-the-art system-level design flows.

Detailed program

0930 – 1100: Introduction and tutorial overview (Frank Oppenheimer)
An MDD Methodology for Specification and Performance Estimation of Embedded Systems (Eugenio Villar)
1100 – 1130: Break
1130 – 1300: Virtual Platform Generation, Integration and Extension of Extra-Functional Properties (Emmanuel Vaumorin)
Industrial experience report for model-based design in space/aerospace applications (demo) (Francisco Ferrero)
1300 – 1430: Lunch Break
1430 – 1600: From RTL IP to Functional System-Level Models with Extra-Functional Properties (Davide Quaglia)
High-Level Synthesis-based Hardware Power and Timing Estimation (Philipp A. Hartmann)
1600 – 1630: Break
1630 – 1800: Software Power and Timing Estimation (Carlo Brandolese)
Network-aware Design-Space Exploration of a Power-Efficient Embedded Application (demo) (Sara Bocchio)
Summary and Closing remarks (Frank Oppenheimer)

Tutorial C

E-Health: systems, components, technologies

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

C: E-Health: systems, components, technologies

Full-day	Topic: System design	Room Chartreuse
Organizer:	Giovanni De Micheli	Ecole Polytechnique de Lausanne - Switzerland
Speakers:	Rudy Lauwereins	IMEC - Belgium
	Giovanni De Micheli	Ecole Polytechnique de Lausanne - Switzerland
	Carlotta Guiducci	Ecole Polytechnique de Lausanne - Switzerland
	Sven Ingebrandt	University of Kaiserslautern - Germany
	Wayne Burleson	University of Massachusetts - USA

Description

There is a rapid growth of the electro-medical sector and a shortage of engineers and designers who can seize this opportunity. As mass production of standard electronic components is shifting to Asia, it is important for the European Industries and Universities to explore alternative use of silicon. Indeed, the use of silicon interfaces to living matter opens unforeseeable horizons and markets. New electronic systems for diagnostics and care are changing the practice of health management, opening the door to personalized medicine as well as to support for remote care of chronic patients.

This tutorial starts with a survey of the field and the motivations to develop biomedical electronic system. It will be followed by a survey of biosensing methods, for both diagnostics and implants in humans. Whereas the first two presentations will cover system and methodological aspects, the following two will focus on technology, and in particular on silicon technologies for sensing and on biosensor design. The final presentation will return to system aspects with a presentation of security features as a key design problem.

Detailed program

0930 – 1100: Introduction, motivation and big picture (Rudy Lauwereins)
1100 – 1130: Break
1130 – 1300: Survey of biosensors for medical applications (Sven Ingebrandt)
Biosensor integration (Carlotta Guiducci)
1300 – 1430: Lunch Break
1430 – 1600: MEMS for health applications (Benedetto Vigna)
1600 – 1630: Break
1630 – 1800: System design issues in e-health applications (Wayne Burleson)
Case studies and conclusions (Giovanni De Micheli)

Tutorial D1

Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyberphysical System Integration

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

D1: Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyberphysical System Integration

Half-day	Topic: System design	Room Meije 2
Organizer:	Krishnendu Chakrabarty	Duke University - USA
Speakers:	Tsung-Yi Ho	National Cheng Kung Univ. - Taiwan
	Krishnendu Chakrabarty	Duke University - USA

Description

This tutorial will first provide an overview of typical biomolecular applications (market drivers) such as immunoassays, DNA sequencing, clinical chemistry, etc. Next, microarrays and various microfluidic platforms will be discussed.

The second part of the tutorial will focus on electrowetting-based digital microfluidic biochips. The key idea here is to manipulate liquids as discrete droplets. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial. Basic concepts in microfabrication techniques will also be discussed.

Attendees will next learn about CAD, design-for-testability, and reconfiguration aspects of digital microfluidic biochips. Synthesis tools will be described to map assay protocols from the lab bench to a droplet-based microfluidic platform and generate an optimized schedule of bioassay operations, the binding of assay operations to functional units, and the layout and droplet-flow paths for the biochip. The role of the digital microfluidic platform as a “programmable and reconfigurable processor” for biochemical applications will be highlighted. Sensor integration, and cyberphysical integration using low-cost sensors and adaptive control software will be highlighted. Reconfiguration techniques will be presented to easily bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. With the availability of these tools, chip users and chip designers will be able to concentrate on the development and chip-level adaptation of nano-scale bioassays (higher productivity), leaving implementation details to CAD tools.

Earlier offerings of this (and similar) tutorials covered technology aspects, initial work on CAD algorithms and test solutions. This tutorial will, for the first time, include sensor integration, cyberphysical adaptation and hardware/software co-design for biochemistry-on-a-chip, error recovery, and dynamic reconfiguration

Detailed program

0930 – 1015: Technology overview (Krishnendu Chakrabarty)
1015 – 1100: Fluidic synthesis methods (Tsung-Yi Ho)
1100 – 1130: Break
1130 – 1200: Chip design (Tsung-Yi Ho)
1200 – 1230: Cyberphysical integration (Krishnendu Chakrabarty)
1230 – 1300: Dynamic reconfiguration (Krishnendu Chakrabarty)
1300 – 1430: Lunch Break

Tutorial D2

Hardware Security and Trust

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

D2: Hardware Security and Trust

Half-day	Topic: System design	Room Meije 2
Organizer:	Ramesh Karri	New York university - USA
Speakers:	Ramesh Karri	New York university - USA
	Miodrag Potkonjak	University of California at LA - USA
	Ozgur Sinanoglu	New York University - USA

Description

Hardware security and trust is an important design objective similar to power, performance, reliability and testability. We will highlight why hardware security and trust are important objectives from the economics, security, and safety perspectives. We will highlight various attacks and countermeasure, hardware based security primitives, security vs reliability vs quality trade-offs.

Globalization of Integrated Circuit (IC) design is making designers and users of IC and Intellectual Property (IP) re-assess their trust in hardware. As the IC design flow spans the globe -driven by cost-conscious consumer electronics- hardware is increasingly prone to side channel analysis, reverse engineering, IP piracy and malicious modifications (i.e. hardware trojans). An attacker, anywhere within the global, horizontal design flow, can reverse engineer the functionality of an IC/IP, steal and claim ownership of the IP or introduce counterfeits into the supply chain. Moreover, an untrusted IC fab may overbuild ICs and sell them illegally. Finally, rogue elements in the fabs may insert hardware trojans into the design without the knowledge of the designer or the end-user of the IC; this additional functionality may subsequently be exploited to introduce errors in the results, steal sensitive information or incapacitate a fielded system. The semiconductor industry routinely loses over $4 billion annually due to these attacks. In this tutorial we will introduce this important, emerging area of Design, Test and EDA.

Detailed program

1300 – 1430: Lunch Break
1430 – 1600: Side channels and hardware security primitives
(Miodrag Potkonjak)
Malicious modifications (hardware trojans) to designs
(Ramesh Karri)
1600 – 1630: Break
1630 – 1800: IC reverse engineering, overbuilding and IP piracy
(Ozgur Sinanoglu)
Design for Test vulnerabilities and countermeasures
(Ramesh Karri)
Conclusions (Potkonjak/Karri/Sinanoglu)

Tutorial E1

Assertion Based Verification: a Common Verification Infrastructure for SoC and Embedded Software

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

E1: Assertion Based Verification: a Common Verification Infrastructure for SoC and Embedded Software

Half-day	Topic: Verification	Room Meije 3
Organizers:	Masahiro Fujita	University of Tokyo - Japan
	Graziano Pravadelli	Università di Verona - Italy
Speakers:	Giuseppe Di Guglielmo	Columbia University - USA
	Masahiro Fujita	University of Tokyo - Japan
	Cristina Marconcini	STM Product - Italy
	Graziano Pravadelli	Università di Verona - Italy

Description

Model driven design and virtual prototyping are pushing more and more towards the convergence between HW design and embedded SW development. However, the adoption of HW/SW unrelated verification approaches tends to increase both the verification time and the risk of bug escaping at the HW/SW frontier. In this context, assertion-based verification (ABV) is a promising approach for SoC as well as of embedded software. However, some practical aspects still prevent industries from definitely including ABV in their design process. Among the most relevant issues we can cite: (i) the difficulty of writing a complete and signification set of assertions, which really reflects the intent described in the test plan, and (ii) the lack of a design methodology for embedded SW development and FPGA prototyping, which easily enables dynamic ABV. For these reasons someone thinks ABV requires a too strong formal background to writing assertions, while others believe ABV mandatory needs the use of formal tools that cannot easily handle neither large SoC descriptions, nor complex embedded SW implementations. This half-day tutorial is intended to controvert such beliefs.

The first part introduces ABV and, particularly, the Property Specification Language for assertion definition.

The second part deals with basic and advanced ABV methods based on static and dynamic analysis targeting HW designs including SoC. This covers automatic generation of assertions from simulation results, as it is crucial to have sufficient sets of assertions for more complete verification. Automatic generation can provide assertions escaping manual definition. Both algorithmic as well as empirical results are shown. This part also discusses how to check the completeness of the assertions prepared for a particular design.

The third part describes dynamic ABV methods for embedded SW. Although both static and dynamic ABV methods are widely adopted for HW, software parts are traditionally verified by means of static ABV. This is because dynamic approaches need simulation assumptions that could not be true during

execution of general embedded software and also cannot be controlled by the assertion language. Here, dynamic ABV methods, which exploit model-driven designs for guaranteeing such simulation assumptions, are introduced. These techniques can also be applied to post-silicon verification and debugging for SoC.

Finally, the tutorial will be concluded by showing how ABV-based tools can be profitably used to accomplish verification process requirements, like, for example, those described in the IEC 60730 safety standard for automatic electronic controls used in household appliances.

Detailed program

0930 – 1000: Introduction to ABV and PSL (Graziano Pravadelli)
1000 – 1100: ABV for SoC (Masahiro Fujita)
1100 – 1130: Break
1130 – 1230: Dynamic ABV for embedded SW (Giuseppe Di Guglielmo)
1230 – 1300: ABV and the IEC 60730 safety standard
(Cristina Marconcini)
1300 – 1430: Lunch Break

Tutorial E2

Design and Verification of Embedded Systems from Natural Language Descriptions

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

E2: Design and Verification of Embedded Systems from Natural Language Descriptions

Half-day	Topic: Verification	Room Meije 3
Organizer:	Robert Wille	University of Bremen -Germany
Speakers:	Rolf Drechsler	DFKI GmbH - Germany
	Wolfgang Ecker	Infineon Technologies - Germany
	Rainer Findenig	Intel Mobile Communications - Austria
	Ian G. Harris	University of California Irvine - USA
	Robert Wille	University of Bremen - Germany

Description

The initial starting point of each design process usually is given by means of a textual specification provided in a natural language. However, the process of creating and verifying an accurate and complete formal representation has always been a bottleneck in the design. Manually generating such a formal description from the specification is expensive, requires significant time, and a large number of well-trained design and verification engineers. Usually, only humans with expert design knowledge are assumed to have the ability to properly interpret the respective specification documents. But in the recent years, much progress has been made in the (semi-)automatic transformation of textual specifications into formal descriptions.

At the same time, designers are constantly striving for higher levels of abstraction. After the gate level, the Register Transfer Level (ESL), and the Electronic System Level (ESL), researchers are increasingly considering the formal specification level. Modeling languages such as the Unified Modeling Language (UML) or the System Modeling Language (SysML) provide proper syntax and semantic for this purpose. They allow for a formal specification of the structure and the behavior of a system while, at the same time, hiding precise implementation details. Using these formal descriptions, crucial design flaws can already be detected at the specification level and, thus, before any line of code is written. Besides that, they provide a formal input for automatic code generation techniques.

Both developments build the basis to narrow the gap between the (natural language) specification as well as its actual implementation and, at the same time, allow for a verification-driven design flow. This tutorial will provide an overview on this progress and outline the challenges and opportunities resulting from these developments. We show how NLP and modeling languages build the basis for a new design flow, which incorporates automation from the beginning to the initial code generation.

Detailed program

1300 – 1430: Lunch Break
1430 - 1445: Introduction and Envisioned Design Flow (Robert Wille)
1445 - 1530: Natural Language Processing (Ian G. Harris)
1530 - 1600: Deriving Formal Specifications Through NLP (Rolf Drechsler)
1600 - 1630: Break
1630 - 1700: Verification of Formal Specifications (Robert Wille)
1700 - 1745: Code Generation (Wolfgang Ecker and Rainer Findenig)
1745 - 1800: Conclusion and Open Research Questions (Rolf Drechsler)

Tutorial F

Post-Silicon Validation: old challenges and new solutions

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

F: Post-Silicon Validation: old challenges and new solutions

Full-day	Topic: Validation	Room Stendhal
Organizers:	Valeria Bertacco	University of Michigan - USA
	Amir Nahir	IBM - Israel
Speakers:	Rand Gray	Intel Corp - USA
	Valeria Bertacco	University of Michigan - USA
	Sharad Malik	Princeton University - USA
	Wisam Kadry	IBM - Israel

Description

Taking complex designs, such as microprocessors, from design to manufacturing requires both pre-silicon and post-silicon validation efforts. Because modern designs are extremely complex, pre-silicon verification methods are no longer sufficient to guarantee a correct design. Therefore, a growing portion of the verification effort is shifting to the post-silicon phase, after the first few silicon prototypes become available. While post-silicon validation benefits from extremely high execution performance compared to pre-silicon simulation, major challenges are posed by the limited controllability and observability of internal circuit nodes, as well as the very long error traces generated. Increasing amounts of functionality and IP components integrated into a single chip exacerbate these issues significantly.

Compounding these issues are the ever-increasing speeds of high speed system level signaling schemes, which, in turn, drive up analog circuit complexity in silicon. Moreover, memory subsystem architecture continues to increase in complexity to keep up with power and performance targets.

This tutorial will provide an overview of the validation challenges that are specific to the post-silicon domain. It will then discuss strategies and methods used in the industry to expose, locate and debug the different classes of silicon bugs (functional, electrical and manufacturing errors). The discussion will also reference specific experiences and design case studies to which the techniques presented have been applied. We will also provide a forward-looking perspective regarding emerging solutions in silicon debug, based on recent academic research. The discussion will focus primarily on the post-silicon validation of complex processors, since this is a market segment where post-silicon validation is widely deployed; however, many of the solutions are suitable for digital designs in general.

Detailed program

0930 – 1100: Post-silicon bugs and industry tools
(Rand Gray, Wisam Kadry)
1100 – 1130: Break
1130 – 1300: Post-silicon monitoring infrastructures
(Valeria Bertacco, Sharad Malik)
1300 – 1430 Lunch Break
1430 – 1600: Bug localization. Microprocessor's solutions
(Valeria Bertacco, Sharad Malik)
1600 – 1630 Break
1630 – 1800: Post-silicon methodologies in the industry
(Rand Gray, Wisam Kadry)

Tutorial G

Design Methodologies for Adaptive Circuits and Systems

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

G: Design Methodologies for Adaptive Circuits and Systems

Full-day	Topic: Physical design	Room Bayard
Organizer:	Saibal Mukhopadhyay	Georgia Institute of Technology - USA
Speakers:	Saibal Mukhopadhyay	Georgia Institute of Technology - USA
	Abhijit Chatterjee	Georgia Institute of Technology - USA
	Sudhakar Yalamanchili	Georgia Institute of Technology - USA
	Arijit Raychowdhury	Intel - USA

Description

CMOS technology scaling along with the resulting large variability of circuit performance metrics in the presence of manufacturing process variations has made post-silicon and dynamic adaptation/tuning almost a necessity for nanometer scale silicon technologies. Currently, circuits and systems are designed to tolerate worst-case process corners and worst case operating conditions (e.g. worst case voltage and temperature conditions). The traditional design approach of excessively guard-banding the products results in unacceptable power-performance-yield tradeoffs as technology moves to 10nm nodes. The preceding challenge has led to significant research and development in designing circuits that are "self-aware" and can adapt to process (static) and environmental (dynamic) variations to minimize guard-banding and hence reduce power while maintaining desired yield and reliability. Such self-awareness involves incorporation of on-chip and on-line characterization static/dynamic variations using sensors and/or built-in test/diagnosis and performing on-line tuning/adaptation. The adaptation methodologies are different at the circuit and system levels. Likewise the digital and mixed-signal systems have different challenges for adaptation. This tutorial will provide a broad perspective of the emerging trend of adaptive circuits and systems for next generation electronics; summarize recent results obtained in this area; and points to directions for future work. First, the tutorial will discuss the circuit level techniques for adaptations including on-chip sensors. The advancements in the adaptive logic and memory circuits will be presented. Next, the tutorial will discuss the challenges in designing adaptive digital systems focusing on the architecture level adaptation. Special emphasis will be given in illustrating the need for innovative modeling and simulation methodologies required to design adaptive architectures. Finally, the tutorial will summarize recent results obtained in the design of self-aware wireless communications systems to illustrate the challenges and methodologies for adaptive mixed-signal systems.

A full-day tutorial is proposed to cover the different aspects of adaptive systems spanning different levels of design abstractions – from circuits to micro-architecture, and different types of circuits – logic, memory, and RF subsystems.

The coverage of all these various aspects in a single tutorial will provide the audience a broad perspectives of the very important topic of adaptive systems.

Detailed program

0930 – 1100: Introduction and Motivation (Saibal Mukhopadhyay)
Adaptive Logic Circuits (Saibal Mukhopadhyay)
1100 – 1130: Break
1130 – 1300: Adaptive SRAM circuits (Arijit Raychowdhury)
1300 – 1430: Lunch Break
1430 – 1600: Adaptive Architecture (Sudhakar Yalamanchili)
1600 – 1630: Break
1630 – 1800: Adaptive Wireless Systems (Abhijit Chatterjee)
Conclusion and Discussion

Tutorial H1

Mixed-signal DfT & BIST: Trends, Principles, and Solutions

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

H1: Mixed-signal DfT & BIST: Trends, Principles, and Solutions

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

Half-day		Room 7 Laux 4
Organizer(s):	Yiorgos Makris	University of Texas at Dallas – USA
	Dimitris Gizopoulos	University of Athens - Greece
Speakers:	Stephen Sunter	Mentor Graphics - USA

Description

We start by briefly looking at trends in process, design, and analogue/mixed-signal testing, then in more detail at trends in ad hoc design-for-test (DfT) and analogue defect simulation. We then review standardized DFT suitable for mixed-signal circuits, including IEEE 1149.1, .4, .6, .8, and 1687. The trend analysis concludes with an analysis of BIST techniques, especially for ADC/DAC, but also for PLL, SerDes, DDR, and miscellaneous analogue. Next, seven essential principles of practical analogue BIST are discussed, ranging from testing the BIST itself, and adding for precision, to subtracting for accuracy, and generating a digital result. Lastly, we discuss the most practical techniques to use in new DfT and BIST circuitry, ranging from the classic analogue test bus, to mostly-digital oversampling and undersampling circuits that improve measurement range, resolution, and reusability, to ultimately optimize quality and cost of test.

Detailed program

0930 – 1100: Trends, and Review of IEEE Standards
1100 – 1130: Break
1130 – 1300: BIST Principles, and Techniques for New DFT
1300 – 1430: Lunch Break

Tutorial H2

Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliabilty

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

Tutorials Chair
Franco Fummi - Università di Verona – Italy

March 18, 2013

Sponsored by the
European Design and Automation Association,
the EDA Consortium, the IEEE Council on EDA,
ECSI, ACM-SIGDA and RAS.

H2: Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliabilty

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

Half-day		Room 7 Laux 4
Organizer(s):	Yiorgos Makris	University of Texas at Dallas - USA
	Dimitris Gizopoulos	University of Athens - Greece
Speakers:	Rob Aitken	ARM - GB

Description

The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

Detailed program

1300 – 1430: Lunch Break
1430 – 1600: Introduction and Background
Yield and Fab Metrology
DFM/Y – Design for Manufacturability and Yield
Variability and DFV
1600 – 1630: Break
1630 – 1800: DFT / Test and the link to Manufacturability
Diagnosis and the Feedback Loop
Reliability
Putting it all together