advance programme

DATE 10

Design, Automation & Test in Europe

ICC, Dresden, Germany
March 8 - 12, 2010

www.date-conference.com

welcome to date 10

Dear Colleague,

We proudly present to you the Advance Programme of **DATE 10.** DATE combines the world's favourite electronic systems design conference with an international exhibition for electronic design, automation and test, from system level hardware and software implementation right down to integrated circuit design. While many conferences currently suffer from travel restrictions in many companies and face severe problems in attracting attendees, the total number of submissions for DATE 2010 reached an all-time high of more than 980 submissions. The importance of DATE as a worldwide indispensable meeting point is demonstrated by the fact that more than 50% of the submissions came from outside Europe. The most popular topics this year were Simulation/Emulation and Low Power Systems Design, Estimation and Optimisation.

For the 13th successive year DATE has prepared an exciting technical programme, with the help of the more than 550 members of the Technical Programme Committee, who dedicated their time to thoroughly review the submissions, ranging from system level down to circuit design and covering all the most relevant application domains.

This year the conference will be held in Germany, at the International Congress Center (ICC) in Dresden and will span an entire working week starting on Monday March 8 with tutorials, and ending on Friday March 12 with workshops.

The **plenary keynote speakers** on Tuesday are Alberto Sangiovanni-Vincentelli of UC Berkeley and Cadence, to talk about 'All Things are Connected', and Herman Eul, VP, Infineon and University of Hannover to talk about 'Wireless Communication – Successful Differentiation on Standard Technology by Innovation'. On the same day, the **Executive Track** offers a series of business panels discussing hot topics in design: 'How to Address Today's Growing System Complexity?', 'The Impact of Nanometer Technologies on Manufacturability on Yield' and 'Impacts of Continuous Scaling on the Semiconductor Industry'. To emphasise that DATE is the major event for the designers, DATE 10 features invited sessions where **Europe's famous consumer industry presents its best designs and design practices.**

The main conference programme from Tuesday to Thursday includes 77 technical sessions organised in parallel tracks from four areas:

D – Design Methods, Tools, Algorithms and Languages
A – Application Design
T – Test Methods, Tools and Innovative Experiences
E – Embedded Software

Extra tracks are dedicated to the Executive Day on Tuesday and the two special days: **Cool Electronic Systems** on Wednesday and **Nanoelectronics** on Thursday with Mark Horowitz (Stanford University, US) and Dimitris Antoniadis (MIT, US) as keynote speakers. Additionally, there are 86 Interactive Presentations which are organised into five IP sessions.

Finally, DATE offers a comprehensive overview of commercial design and verification tools in its exhibition including vendor seminars and abundant networking possibilities with fringe meetings.

We wish you a productive and exciting DATE 10 and a memorable social party on Wednesday evening.

DATE 10 General Chair Giovanni De Micheli
EPF Lausanne, Switzerland
giovanni.demicheli@epfl.ch

DATE 10 Programme Chair Wolfgang Mueller
University of Paderborn, Germany
wolfgang@acm.org

plenary session

Tuesday, March 9, 2010, 0830 – 1030

Opening Address – Awards – Keynote Speakers

first keynote address

All things are connected

Alberto Sangiovanni-Vincentelli, UC Berkeley and Cadence, US

Abstract: Design of complex system is essentially about connections: Connection of concepts, Connection of objects, Connection of teams. And products of the future will be connected seamlessly across physical and virtual domains. Connections can produce systems that offer more than the sum of the components but they can also yield to systems that are less powerful than the sum of the components or that are so compromised by their interactions that they do not work at all.

Collaboration is the name of the game for design, for production, for operation of multi-scale systems.

There is increasingly less distance between design and operation of systems. An efficient management of interactions among deployed parts of a larger systems requires principles that are common to the design methods developed at the bleeding edge of technology. I will examine the evolution of design principles and of multiscale systems and the challenges we are facing today. I will point to a number of exciting fields where advances are constantly made towards the mastering of connections.

plenary session

Tuesday, March 9, 2010, 0830 – 1030

Opening Address – Awards – Keynote Speakers

second keynote address

Wireless communication – successful differentiation on standard technology by innovation

Herman Eul, VP, Infineon and University of Hannover, DE

Abstract: The rise of the wireless internet is the megatrend in communication industry. Mobile communication devices will be the dominant platform for information access, gaming, music and spending time with distant friends. About 5 bn or three quarters of the world population is using mobile phones. Internet enabled mobile phones at affordable cost will be the most common internet access device in the near future. At the high end powerful and versatile smartphones need faster and more energy efficient semiconductors.

The presentation will start with a brief summary of the paradigm shifts in the "mobile world" from voice calls to data transmission and the current situation in the renascent mobile ecosystem. The entry of powerful internet and consumer brands and now even luxury designer brands into the mobile handset arena mark the start of a new era changing the dynamics in this field.

Today, fabless or fab-lite business models are common in the wireless semiconductor value chain. In this model vendors differentiate through services, architectures, design but also their capability to extract maximum product benefits in density, power consumption, performance, functionality and robustness/yield from a standard CMOS process. In the highly competitive mobile phone market growth and profit depends on differentiation by innovation. This requires technology know-how being effectively transferred into the design system and application specific device structures to create optimised circuits.

general information

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 10. Full General Information covering full technical programme details, conference registration costs and booking forms, hotel reservations and booking forms, travel to and in Dresden and social event details is available on the conference website - **www.date-conference.com**

interactive programme on web

A fully interactive DATE 10 programme is available on the web – **www.date-conference.com** - where you will be able to view the entire detail of the programme and plan your attendance in advance.

venue

The Conference will take place from 8-12 March 2010 and the Exhibition from 7-11 March 2010 in the excellent facilities of the International Congress Center (ICC), Dresden, Germany - **www.dresden-congresscenter.de**

date party – wednesday

This year the DATE party will take place in the Great Hall of the International Congress Center, Dresden. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. There will be relaxed musical entertainment. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 70 Euros each (see website for booking forms). Entrance will be by ticket only, so please check that you receive the party ticket when you register.

cancellation policy

Registered delegates should note that no refunds will be made unless a written request for cancellation is received prior to **12 February 2010.** All refunds are subject to a 10% processing fee. Substitutions will be accepted at any stage.

interactive presentations

Chair: **Andrea Acquaviva,** Politecnico di Torino, IT

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute, one-slide presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the ICC, Dresden, in the Exhibition Area 30-minute time slots during coffee and exhibition breaks. Presentations will be made in repeating ten minute slots during each session (three rounds of presentations in each IP Session). Coffee and water will be available during the session.

executive track – tuesday

Organiser:
Yervant Zorian, Virage Logic, US

DATE 10 will again feature an Executive Track of presentations by leading company executives (CEOs, Presidents and VPs) representing a range of semiconductor manufacturers, EDA vendors, fabless houses, IP providers and equipments suppliers. This one-day program will be held on Tuesday 9 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 5-6 executives and run in parallel to the technical conference tracks. All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1 EXECUTIVE SESSION – How to Address Today's Growing System Complexity?

– see page 25

3.1 EXECUTIVE SESSION – The Impact of Nanometer Technologies on Manufacturability on Yield

– see page 30

4.1 EXECUTIVE SESSION – Impacts of Continuous Scaling on the Semiconductor Industry

– see page 37

Organisers:
G Fettweis, TU Dresden, DE
B Ristau, TU Dresden, DE

Cool Electronic Systems Special Day

Innovations in micro and nanotechnology form the basis of modern ICT. However, the steady growth in the ICT sector has meanwhile a significant ecological footprint: 2% of global CO2 emissions are due to ICT systems already today – one fourth of the emissions caused by cars. The energy costs for running ICT infrastructure have turned into a significant economical factor. The most urgent challenge in the area of micro and nanotechnology is therefore to massively increase energy efficiency, in particular for ICT as a key sector for economic growth. Significant improvements in this area can only be achieved through disruptive innovations and new system approaches, which rely on a combination of excellent research & development and world leading know-how of semiconductor production.

The Cool Electronic Systems Special Day is a platform for discussing visions and recent advances in designing energy-efficient ICT systems. The day starts with a panel session where recognised experts from the design automation community will discuss 'The Road to Energy-Efficient Systems: From Hardware-Driven to Software-Defined'. The panel session is followed by three technical sessions, each targeting a different field of application for cool systems, namely 'Cool Wireless Systems', 'Cool Sensor Networks' and 'Cool Computing Platforms'. A special highlight will be the lunch-time keynote by Mark Horowitz entitled 'Why Design Must Change: Rethinking Digital Design'.

5.1 PANEL SESSION - The Road to Energy-Efficient Systems: From Hardware-Driven to Software-Defined – see page 42

6.1.1 COOL TOPIC - Cool Sensor Networks – see page 47

6.1.2 LUNCH-TIME KEYNOTE AND AWARDS – see page 52

7.1 COOL TOPIC - Cool Communications Systems – see page 54

8.1 COOL TOPIC - Cool Computing Platforms – see page 60

Organisers:
Adrian M Ionescu, EPF Lausanne, CH
Subhasish Mitra , Stanford University, US

Nanoelectronics Special Day

The nanoelectronics day at DATE 2010 has been designed as an event where the system/circuit design and technology/device communities can meet, communicate and exchange ideas on the great challenges and recent trends in modern nanoelectronics. Recent division of nanoelectronics research and applications domains in 'More Moore', 'beyond CMOS' and 'More then Moore' created unique challenges and opportunities for diversification and innovation beyond the aggressive scaling that characterized the long dominance of silicon CMOS.

The full day event includes two series of morning tutorials by international experts, dedicated to Beyond CMOS and More than Moore but also including some hot topics in the advanced CMOS such as the system design under variability.

An outstanding luncheon speaker will summarise the 'Nanoelectronics challenges for the 21st century' and the role of leading edge CMOS technologies compared to the most promising emerging non-CMOS technologies.

The afternoon is split into two parts; first, an all-invited paper session covering life with and after CMOS that includes power constraint design and technology, 3D integration and far looking non-charged based computation, followed by the second part, organised as a panel discussion preceded by an invited talk on nano-electro-mechanical systems, with main focus on More than Moore and Beyond CMOS, as vectors of progress in future nanoelectronics.

9.1 EMBEDDED TUTORIAL – Beyond CMOS – see page 65

10.1.1 EMBEDDED TUTORIAL – More than Moore – see page 71

10.1.2 LUNCH TIME KEYNOTE – see page 76

11.1 HOT TOPIC – Life with and after CMOS – see page 76

12.1 PANEL SESSION - Great Challenges in Nanoelectronics and Impact on Academic research: More than Moore or Beyond CMOS? – see page 83

Special Sessions Chair:
Wolfgang Rosenstiel, University of Tuebingen, DE

Panels Chair:
Donatella Sciuto, Politecnico di Milano, IT

12 Special Sessions have been organised, which should prove to be of great general interest.

Panel Sessions provide a forum in which motivated opinions on a controversial issue are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal from the audience.

Hot Topic sessions give technical information about emerging new topics and provide a good overview and technical insight. Presenters are leading experts in the field. They present their view on the relevant issues and their importance for research and development.

Embedded tutorials give an insight of relevant topics usually starting from an introductory base.

These are the Special Sessions for **DATE 10:**

2.2 Embedded Tutorial – Embedded Systems and their Physical Environment – The 'Cyberphysical' View
Organiser: **R Ernst,** TU Braunschweig, DE

2.8 Panel Session - Are we there yet? Has System Assembly from IP Blocks Become Like Connecting LEGO Blocks?
Organiser: **F Schirrmeister,** Synopsys, DE

3.8 Hot Topic - AUTOSAR and Automotive Software Design
Organiser: **S Fuerst,** BMW Group, DE

5.5 Embedded Tutorial – Adaptive Testing
Organiser: **E J Marinissen,** IMEC, BE

6.2 Hot Topic – Memristor: Device, Design and Application
Organiser: **Y Chen,** Seagate Technology, US

6.8 Panel Session – The Challenges of Heterogeneous Multi-Core Debug
Organiser: **G Martin,** Tensilica, US

7.8 Panel Session – Who is Closing the Embedded Software Design Gap?
Organiser: **W Ecker,** Infineon, DE

8.2 Hot Topic – Cross-Layer Optimisation to Address the Dual Challenges of Energy and Reliability
Organiser: **A DeHon,** Pennsylvania U, US

10.2 Panel Session – First Commandment: At Least Do Nothing Well
Organiser: **M Casale-Rossi,** Synopsys, US

10.8 PANEL SESSION – Embedded Software Testing: What Kind of Problem is This?
Organiser: **E Cota,** UFRGS, BR

11.2 Hot Topic – Cool MPSoC Programming
Organiser: **R Leupers,** RWTH Aachen U, DE

11.8 Panel Session – Reliability of Data Centers: Hardware vs. Software
Organiser: **M Tahoori,** Karlsruhe U, DE

MONDAY

Educational Tutorials
Welcome Drinks Reception

TUESDAY

Technical Conference and Exhibition Day 1
Vendor Exhibition
Exhibition Theatre (also featuring Track 8 special conference sessions)
Opening Plenary and Keynote Addresses
Executive Sessions
Exhibition Reception

WEDNESDAY

Technical Conference and Exhibition Day 2
Vendor Exhibition
Exhibition Theatre (also featuring Track 8 special conference sessions)
Cool Electronic Systems Special Day and Keynote
DATE Awards Ceremony
DATE Party

THURSDAY

Technical Conference and Exhibition Day 3
Vendor Exhibition
Exhibition Theatre (also featuring Track 8 special conference sessions)
Nanoelectronics Special Day and Keynote

FRIDAY

Special Interest Workshops

CONTACTS

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0730	TUTORIAL REGISTRATION & WELCOME REFRESHMENTS		
BREAKS	1100 to 1130 Morning, 1300 to 1430 Lunch Break, 1600 to 1630 Afternoon		
0930 to 1800	B (Room – Konferenz 6) Electronic Systems and Interfaces for Innovation in Life Sciences and Biomedical Applications	C (Room – Konferenz 5) State-of-the-Art and Challenges in ESL-Verification	D (Room – Konferenz 1) Chip-Package Co-Design Challenges for 3D Integration
0930 to 1300	A1 (Room – Konferenz 2) AUTOSAR	E1 (Room – Konferenz 3) IC yield, Reliability and Prognostic Methods using Nanoscale Test Structures	F1 (Room – Konferenz 4) Application of the SystemC AMS Standard
1430 to 1800	A2 (Room – Konferenz 2) Asynchronous Logic and GALS Design: Principles and State-of-the-Art	E2 (Room – Konferenz 3)	F2 (Room – Konferenz 4) Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices
1800	Reception		

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030 to 1130 Exhibition Break, 1300 to 1430 Lunch Break 1600 to 1700 Exhibition Break (1600 to 1630 IP1)
0830	1.1 PLENARY: OPENING, KEYNOTE ADDRESSES AND AWARDS PRESENTATION Room Grosser Saal		

	SPECIAL TRACK	EMERGING TECHNOLOGIES	DESIGN	APPLICATIONS	TEST	EMBEDDED SOFTWARE	DESIGN	SPECIAL SESSIONS
1130 to 1300	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	2.1 EXECUTIVE SESSION – How to Address Today's Growing System Complexity?	2.2 EMBEDDED TUTORIAL – Embedded Systems and their Physical Environment – The 'Cyberphysical' View	2.3 Power-Aware Technique for Real-Time Systems	2.4 System Level Design of Multicores	2.5 Reliability, Simulation, Yield and Enhancement	2.6 Advances in Embedded Software Development	2.7 Memory Stacking and Cooling Solutions	2.8 PANEL SESSION – Are we there yet? Has System Assembly from IP Blocks Become Like Connecting LEGO Blocks?
1430 to 1600	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	3.1 EXECUTIVE SESSION – The Impact of Nanometer Technologies on Manufacturability on Yield	3.2 Green and Emerging Technologies for Low Power	3.3 Game-Changing Technologies for System Design	3.4 Application Development for Multicores	3.5 Advanced System Chip Testing	3.6 Real-Time Scheduling in Embedded Systems	3.7 Architectural Techniques for Robust Design	3.8 HOT TOPIC - AUTOSAR and Automotive Software Design
1700 to 1830	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	4.1 EXECUTIVE SESSION – Impacts of Continuous Scaling on the Semiconductor Industry	4.2 Variability Aware Low Power Design	4.3 Performance Estimation and Runtime Management of MPSoCs	4.4 Application of Reconfigurable and Adaptive Systems	4.5 Wearout and Process Variation Mitigation and Modelling	4.6 Model Based Design of Embedded Systems	4.7 Extraction and Model Order Reduction	See web or leaflet for the latest exhibition programme

0730	REGISTRATION & SPEAKERS' BREAKFAST			BREAKS	1000 to 1100 Exhibition, (1000 to 1030 IP2), 1230 to 1340 Lunch Break, 1600 to 1700 Exhibition (1600 to 1630 IP3)			
	SPECIAL TRACK	EMERGING TECHNOLOGIES	DESIGN	APPLICATIONS	TEST	EMBEDDED SOFTWARE	DESIGN	SPECIAL SESSIONS
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
0830 to 1000	5.1 PANEL SESSION – The Road to Energy-Efficient Systems: From Hardware-Driven to Software-Defined	5.2 Automating Verification with Simulation, Properties and Assertions	5.3 Power Optimisation and Estimation for Flash and CMOS Technologies	5.4 Automotive Systems: Mastering Complexity and Uncertainty	5.5 EMBEDDED TUTORIAL – Adaptive Testing	5.6 Virtualisation Technologies	5.7 Variability Reliability and Thermal Trade-Offs for Low-Power Design	EXHIBITION OPENS AT 1000
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
1100 to 1230	6.1.1 COOL TOPIC – Cool Sensor Networks	6.2 HOT TOPIC – Memristor: Device, Design and Application	6.3 Addressing the Challenge of Technology Scaling	6.4 Analogue and Mixed-Signal System Implementations	6.5 On-Line Testing Techniques	6.6 Performance Analysis of Embedded Software for MPSoCs	6.7 Advances in Logic Synthesis for Reliability and Matching	6.8 PANEL SESSION – The Challenges of Heterogeneous Multi-Core Debug
1340	6.1.2 LUNCH-TIME KEYNOTE AND AWARDS 1340-1400 Awards and 1400-1430 Keynote, Room – Saal 5							
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
1430 to 1600	7.1 COOL TOPIC – Cool Communications Systems	7.2 Statistical Validation at 45nm and Beyond	7.3 Reconfigurable Architectures	7.4 Secure Embedded Systems	7.5 Test Generation, Fault Simulation and Diagnosis	7.6 Applications and Principles for Embedded Multi-Core Systems	7.7 Innovative Memory Architectures	7.8 PANEL SESSION – Who is Closing the Embedded Software Design Gap?'
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
1700 to 1830	8.1 COOL TOPIC – Cool Computing Platforms	8.2 HOT TOPIC – Cross-Layer Optimisation to Address the Dual Challenges of Energy and Reliability	8.3 System Modelling for Design Space Exploration and Validation	8.4 Sensor Networks and Security Technology	8.5 Variability and Yield in Analogue and Mixed-Signal Design	8.6 Resource-Aware Embedded Code Optimisation	8.7 Macromodelling for Thermal and Interconnect Systems	See web or leaflet for the latest exhibition programme

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000 to 1100 Exhibition Break, (1000 to 1030 IP4), 1230 to 1330 Lunch Break, 1530 to 1600 Break (1530 to 1600 IP5)					
	SPECIAL TRACK	EMERGING TECHNOLOGIES	DESIGN	APPLICATIONS	TEST	DESIGN	DESIGN	SPECIAL SESSIONS
0830 to 1000	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	9.1 NANOELECTRONICS TUTORIAL – Beyond CMOS	9.2 Multi-Level, Multi-Domain System Simulation	9.3 Language Based Approaches to System Level Design	9.4 Space and Aeronautics Avionics Application Design	9.5 Design for Test, Diagnosis, and Yield	9.6 High Level Synthesis	9.7 Physical Design Potpourri: DFM, Delay Modelling and Floorplanning	EXHIBITION OPENS AT 1000
1100 to 1230	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	10.1.1 NANOELECTRONICS TUTORIAL – More than Moore	10.2 PANEL SESSION – First Commandment: At Least Do Nothing Well	10.3 Characterising and Optimising NoC Performance	10.4 Architectures for Next Generation Wireless Communication	10.5 Advances in Delay Fault Testing	10.6 Optimisation of Fault Tolerant and Time Constrained Embedded and Cyber-Physical Systems	10.7 Advanced Clocking Strategies	10.8 PANEL SESSION – Embedded Software Testing: What Kind of Problem is This?
1330	10.1.2 LUNCH TIME KEYNOTE, Room – Saal 5							
1400 to 1530	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	11.1 NANOELECTRONICS HOT TOPIC – Life with and after CMOS	11.2 HOT TOPIC – Cool MPSoC Programming	11.3 Industrially-Oriented Formal Verification	11.4 Sensor Networks and Applications	11.5 Fault Tolerance	11.6 Synthesis and Optimisation of MpSoCs	11.7 Mixed-Technology and Analogue Design	11.8 PANEL SESSION – Reliability of Data Centers: Hardware vs. Software
1600 to 1730	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	12.1 NANOELECTRONICS PANEL – Great Challenges in Nanoelectronics and Impact on Academic research	12.2 HOT TOPIC – 3D Stacked ICs: Technology, Design and Test	12.3 Formal Methods: Advances in Core Technology	12.4 Video Encoding and Image Processing Techniques	12.5 Testing and Diagnosis of Analogue and Mixed-Signal Circuits	12.6 Timing Aspects in System Synthesis	12.7 Reliability and Power Optimisations for FPGAs	See web or leaflet for the latest exhibition programme

0730	WORKSHOP REGISTRATION & WELCOME REFRESHMENTS
BREAKS	Workshop programmes vary. Please see individual programmes for start, break and close times.

	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 6	Room – Konferenz 5
0830 to 1700	W1 The European landscape of reconfigurable computing: Lessons learned, new perspectives and innovations	W2 The Fruits of Variability Research in Europe	W3 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications	W4 SDD – Silicon Debug-and-Diagnosis	W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test	W6 1st Workshop on Model Based Engineering for Embedded Systems Design (M-BED 2010)

Organiser: Pol Marchal, IMEC, BE

Nine pre-conference tutorials will be given on Monday. Three are full-day tutorials (B, C and D). Six are half-day tutorials, three to be given in the morning (A1, E1 and F1) and three in the afternoon (A2, E2 and F2). A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

The titles, organisers, speakers, and abstracts of the tutorials are given below:

0930 FULL-DAY TUTORIALS – B, C, D

B (Room – Konferenz 6)

Electronic Systems and Interfaces for Innovation in Life Sciences and Biomedical Applications

Organiser: Georges Gielen, KU Leuven, BE
Carlotta Giuducci, EPF Lausanne, CH

Speakers: Carlotta Giuducci, EPF Lausanne, CH
Roland Thewes, TU Berlin, DE
Wolfgang Eberle, IMEC, BE
Marco Bianchessi, STMicroelectronics, IT

The interface between electronic circuits and life sciences is one of the focal points of future integrated system design. Applications include biomolecule detection, biosensor arrays, deep brain stimulation, cardiac cell monitoring, among many others. Several solutions for electronic devices/biological matter interactions are already available and they have proven their potential to be highly-portable systems or high-throughput systems or both. In this tutorial, we will address in detail the challenges in design and implementation of electronic sensors, circuits and systems as privileged means to interact with biological matter while bringing the advantage of almost unlimited choice of signal processing, storing and communication solutions. All aspects will be covered, ranging from providing an overview of different sensing solutions, discussing the architectural and circuit design issues to illustrating the packaging and testing solutions for both in vitro and in vivo applications. The tutorial scope goes from advanced research to commercial applications that are available on the market.

C (Room – Konferenz 5)

State-of-the-Art and Challenges in ESL-Verification

Organiser: Volkan Esen, Infineon Technologies AG, DE

Speakers: Oliver Bringmann, Forschungszentrum Informatik FZI, DE
Wolfgang Ecker, Infineon Technologies AG, DE
Erhard Fehlauer, Fraunhofer IIS/EAS Dresden, DE
Daniel Grosse, Bremen U, DE
Christoph Kuznik, Paderborn U, DE
Jan-Hendrik Oetjens, Robert Bosch GmbH, DE
Andreas v. Schwerin, Siemens AG, DE

The increasing complexity of embedded systems has driven the development of new abstract modeling techniques, leading to the so-called Electronic System Level (ESL). For ESL design SystemC has become the de-facto system description language. In SystemC the most popular and widely used abstraction level is Transaction Level Modelling (TLM). Over the last years intensive research in academia and industry brought new methodologies and modelling standards such as OSCI TLM2 to today's virtual prototype development. Virtual prototypes are used for many different tasks, as e.g. early SW development. As SW development based on virtual platforms is possible long before the silicon is available, the design productivity increases significantly.

However, to fully benefit from the productivity gain possible, the bottleneck of functional verification has to be addressed. Therefore, in the recent years different methodologies and approaches have been developed which target the verification of TLM designs and virtual prototypes. This tutorial outlines the verification challenges for SystemC models and in particular for ESL. Furthermore, different verification tasks are considered and the respective verification approaches are explained. It is shown to what level verification of TLM-models can be done with today's verification methodologies and pros and cons of the approaches are discussed.

D (Room – Konferenz 1)

Chip-Package Co-Design Challenges for 3D Integration

Organisers: Herb Reiter, EDA2ASIC
Pol Marchal, IMEC, BE

Speakers: Jochen Reisinger, Infineon, DE
Geert van der Plas, IMEC, BE
Ravi Varadarajan, Atrenta
Ghislain Kaiser, Docea Power
Edmund Cheng, Gradient DA
Dragomir Milojvic, IMEC, BE
Peter Schneider, Fraunhofer IIS/EAS Dresden, DE
Terry Ma, VP TCAD, Synopsys
Vassilios Gerousis, Cadence
Yann Guillou, STE
Jean Christophe Eloy, Yole

This tutorial will review new 3D integration technologies and their impact on chip-package co-design.

In the morning, the tutorial will highlight the continuing needs for higher levels of integration and the mandates imposed by the stringent cost- and power constraints. The presenters will address the many benefits but also challenges 3D chip-stacking introduces and suggest methods to adopt the design of dies and advanced packages to higher levels of integration.

In addition to new EDA tools and flows, our industry is adopting a new design practice: physical design prototyping of chip stacks. Several experts from industry and academia will share their experience and offer advice before the lunch break.

In the early afternoon session a representative from academia and two major EDA vendors will talk about the multi-physics challenges that need to be considered, both in new EDA flows and the physical design prototyping, to assure success.

Finally, two talks providing an outlook of how 3D technologies impact current and future products will summarise and end the day.

0930 **HALF-DAY TUTORIALS – A1, E1, F1**
Monday Morning

A1 (Room – Konferenz 2)

AUTOSAR

Organiser: Simon Fuerst, BMW Group, DE

Speakers: Simon Fuerst, BMW Group, DE
Gerulf Kinkelin, PSA, FR

The objective of the tutorial is to give an overview on the following main topics:

- Motivation and principles of AUTOSAR
- The technological conception of AUTOSAR
- The development of the AUTOSAR standard

AUTOSAR has been founded as a development partnership in 2003. The common vision was to pave the way for innovative electronic systems by establishing an open industry standard for the automotive software architecture between suppliers and manufacturers. The core partners and more than 170 members produced the first set of major specifications end of Phase I in 2006, meanwhile the standard is already being exploited by all major OEMs and 1st Tiers. The development of the cooperation and the roll-out of a standard will be explained.

The technical scope of AUTOSAR focuses on three main working topics: Basic Software Architecture, Methodology and Templates, and Application Interfaces. Thereby AUTOSAR consolidates existing design elements and new concepts into a coherent standard. The tutorial will show how the organisation of AUTOSAR has been adapting to the ever changing challenges of the automotive market. Currently about 25 work packages are working on developing the specifications.

Through Phase I and II releases R1.0/R2.0/R2.1/R3.0/R3.1 have been made available, while R4.0 followed end of 2009. Details on all major achievements of AUTOSAR Release 4.0 will be presented. At the beginning of 2010 AUTOSAR Phase III has started and will last till end of 2012. The planning of this phase will be presented and details on the new concepts will be given that will extend the AUTOSAR standard.

E1 (Room – Konferenz 3)

IC Yield, Reliability and Prognostic Methods using Nanoscale Test Structures

Organisers: Yiorgos Makris, Yale U, US
Dimitris Gizopoulos, Piraeus, U, GR
Douglas Goodman, Ridgetop Group, US

The mounting issues of decreased yield and reliability from nanoscale IC processes require advanced approaches to the measurement and mitigation of device degradation and variance. Shrinking process geometries, with their corresponding reduction in device lifetimes, have broad implications to critical applications having long intended design lifetimes. Nanoscale transistor sizes are emerging as a major concern to the long term reliability of safety-critical systems in aerospace and automotive applications. Common semiconductor failure modes include Time Dependent Dielectric Breakdown (TDDB), hot carrier damage (HCI), and Negative Bias Temperature Instability (NBTI). Die-level prognostic test structures can detect and help mitigate the untimely failures in critical systems. These test structures, with variance measurement capabilities, also provide an effective platform for improved process-aware design for improved yields. This tutorial will address concepts of in-situ test structures as a solution to yield, reliability and prognostic applications and include practical application examples.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)

F1 (Room – Konferenz 4)

Application of the SystemC AMS Standard

Organiser: Martin Barnasconi, NXP Semiconductors

Speakers: Karsten Einwich, Fraunhofer IIS/EAS Dresden, DE
Christoph Grimm, TU Vienna, AT
Francois Pecheux, Pierre et Marie Curie U, FR
Martin Barnasconi, NXP Semiconductors

Today's embedded systems interact more tightly with the analog physical environment, where digital HW/SW subsystems becomes functionally interwoven with analogue/mixed-signal (AMS) blocks such as RF interfaces, power electronics, or sensors and actuators. Examples are cognitive radios, sensor networks or systems for image sensing. This requires new means to model and simulate the interaction between AMS subsystems and HW/SW subsystems at functional and architecture level. Especially for this purpose, the SystemC language standard has been extended with AMS capabilities.

This tutorial will present the motivation and unique capacities of the SystemC AMS extensions for industrial applications in wireless communication and automotive. New modelling concepts and design refinement methods for mixed-signal systems are explained. An application example of a heterogeneous wireless sensor network is presented, covering modeling across several disciplines (physics, digital, analogue/RF, software), modelling principles and numerical analysis methods.

This tutorial targets hardware and system engineers, architects and verification engineers active in industrial projects where analogue and digital functionality comes together. The tutorial will bring hands-on experience how to efficiently use the SystemC AMS extensions for system design and verification tasks.

1430 **HALF-DAY TUTORIALS – A2, E2, F2**
Monday Afternoon

A2 (Room – Konferenz 2)

Asynchronous Logic and GALS Design: Principles and State-of-the-Art

Organisers: Pascal Vivet, CEA-LETI, FR
Alex Yakovlev, Newcastle U, UK

Speakers: Alex Yakovlev, Newcastle U, UK
Jens Sparso, TU Denmark, DK
Yvain Thonnart, CEA-LETI, FR
Pascal Vivet, CEA-LETI, FR

The growing variability and complexity of advanced CMOS technologies makes the physical design of clocked logic in large Systems-on-Chip (SoC) more and more challenging. Asynchronous logic has been studied for many years and become an attractive solution for a broad range of applications, from massively parallel multi-media systems to systems with ultra-low power consumption, energy autonomous systems, and sensor-network nodes.

The objective of this tutorial is to give a comprehensive overview of asynchronous logic. The tutorial covers the basic principles and advantages of asynchronous logic, as well as deeper insights such as high level modelling, synthesis methods, architecture issues such as arbitration or de-synchronisation techniques. The tutorial also presents the Globally Asynchronous and Locally Synchronous (GALS) design style as an intermediate design solution which is particularly adapted to Network-on-Chip (NoC) architectures. The tutorial finally provides an overview of state-of-the-art circuits and start-up companies.

This tutorial targets VLSI design engineers, technical managers, researchers and students working in the area of SoC design and all those who would like to know more about these technologies that are becoming more and more mature.

E2 (Room – Konferenz 3)

Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices

Organisers: Yiorgos Makris, Yale U, US
Dimitris Gizopoulos, Piraeus U, GR

Speakers: Srivaths Ravi, Texas Instruments, US
Mohammad Tehranipoor, Connecticut U, US
Rohit Kapur, Synopsys, US

The push for portable, battery-operated, and "cool-and-green" electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multi-site ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Furthermore, with power optimisation and power management techniques becoming "de-facto" in almost all emerging 45nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory.

This tutorial is intended to provide an in-depth and up-to-date understanding of low-power IC testing covering (a) dimensions of power-aware testing, (b) techniques for estimation and reduction of test power consumption and (c) test of power managed designs. Case-studies illustrating industrial design deployment practices and existing EDA vendor support will be outlined to illustrate capabilities and gaps in the state-of-the-art.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)

F2 (Room – Konferenz 4)

A Step-by-Step Guide to Advanced Verification

Organiser: Tom Fitzpatrick, Mentor Graphics, US

Speaker: Tom Fitzpatrick, Mentor Graphics, US

In order to improve verification productivity, engineers are faced with a classic choice: work harder or work smarter. Working harder means either putting in more hours or determining how to apply the same verification techniques you've been using to larger and more complex designs without going insane. Working smarter, on the other hand, involves adopting new techniques and advanced technologies that complement what you're used to doing, but rely on tools and automation to accomplish the necessary efficiencies.

This tutorial will demonstrate an advanced verification flow, showing how the latest verification technologies can be combined within an efficient methodology to provide a highly effective and productive verification of an SoC design. Beginning with a discussion of verification requirements, we will show how to create a verification plan that involves requirements beyond just random constraints and coverage, and to build a comprehensive verification environment to meet those requirements.

MONDAY 8 MARCH, 2010

0730 **TUTORIAL REGISTRATION**
0800 **Tutorial Welcome Refreshments**

0930-1800

B (Room – Konferenz 6) **Electronic Systems and Interfaces for Innovation in Life Sciences and Biomedical Applications**

C (Room – Konferenz 5) **State-of-the-Art and Challenges in ESL-Verification**

D (Room – Konferenz 1) **Chip-Package Co-Design Challenges for 3D Integration**

0930

A1 (Room – Konferenz 2) **AUTOSAR**

E1 (Room – Konferenz 3) **IC yield, Reliability and Prognostic Methods using Nanoscale Test Structures**

F1 (Room – Konferenz 4) **Application of the SystemC AMS Standard**

1430

A2 (Room – Konferenz 2) **Asynchronous Logic and GALS Design: Principles and State-of-the-Art**

E2 (Room – Konferenz 3) **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**

F2 (Room – Konferenz 4) **A Step-by-Step Guide to Advanced Verification**

Tutorial attendees should choose in advance one tutorial from A1, E1 or F1, which take place in the morning, and/or one tutorial from A2, E2 or F2, which take place in the afternoon. Those wishing to attend one of the full-day tutorials should choose in advance one of B, C or D. A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed.
All tutorials run in parallel in accordance with the timetable below.
Rooms will be signposted

0730 - 0930	**Registration and Tutorial Welcome Refreshments** (Terrace Level)
0930 – 1100	**Tutorials**
1100 – 1130	**Break**
1130 – 1300	**Tutorials**
1300 – 1430	**Lunch Break**
1330 – 1800	**REGISTRATION**
1430 – 1600	**Tutorials**
1600 – 1630	**Break**
1630 – 1800	**Tutorials**
1800 – 1930	**WELCOME RECEPTION** (Terrace Level)
1900 – 2100	**FRINGE TECHNICAL MEETINGS**

TUESDAY 9 MARCH, 2010

0730 **REGISTRATION and SPEAKERS' BREAKFAST**

Plenary: Opening and Keynote Addresses

Room Grosser Saal, Ground Floor

0830 **OPENING REMARKS AND AWARDS**
G De Micheli, General Chair, EPF Lausanne, CH
W Mueller, Programme Chair, Paderborn U / C-LAB, DE

Presentation of Distinguished Awards

0910 **ALL THINGS ARE CONNECTED**
Alberto Sangiovanni-Vincentelli, UC Berkeley and Cadence, US

Abstract: Design of complex system is essentially about connections: Connection of concepts, Connection of objects, Connection of teams. And products of the future will be connected seamlessly across physical and virtual domains. Connections can produce systems that offer more than the sum of the components but they can also yield to systems that are less powerful than the sum of the components or that are so compromised by their interactions that they do not work at all.

Collaboration is the name of the game for design, for production, for operation of multi-scale systems.

There is increasingly less distance between design and operation of systems. An efficient management of interactions among deployed parts of a larger systems requires principles that are common to the design methods developed at the bleeding edge of technology. I will examine the evolution of design principles and of multiscale systems and the challenges we are facing today. I will point to a number of exciting fields where advances are constantly made towards the mastering of connections.

0950 **WIRELESS COMMUNICATION – SUCCESSFUL DIFFERENTIATION ON STANDARD TECHNOLOGY BY INNOVATION**
Herman Eul, VP, Infineon and University of Hannover, DE

Abstract: The rise of the wireless internet is the megatrend in communication industry. Mobile communication devices will be the dominant platform for information access, gaming, music and spending time with distant friends. About 5 bn or three quarters of the world population is using mobile phones. Internet enabled mobile phones at affordable cost will be the most common internet access device in the near future. At the high end powerful and versatile smartphones need faster and more energy efficient semiconductors.

The presentation will start with a brief summary of the paradigm shifts in the "mobile world" from voice calls to data transmission and the current situation in the renascent mobile ecosystem. The entry of powerful internet and consumer brands and now even luxury designer brands into the mobile handset arena mark the start of a new era changing the dynamics in this field.

Today, fabless or fab-lite business models are common in the wireless semiconductor value chain. In this model vendors differentiate through services, architectures, design but also their capability to extract maximum product benefits in density, power consumption, performance, functionality and robustness/yield from a standard CMOS process. In the highly competitive mobile phone market growth and profit depends on differentiation by innovation. This requires technology know-how being effectively transferred into the design system and application specific device structures to create optimised circuits.

1030 **EXHIBITION BREAK**

Tracks 1, 2, 3, 4, 5, 6, 7 and 8 (except the executive sessions 2.1, 3.1 and 4.1) of the conference programme will present scientific papers that have been reviewed based on their contribution in scientific innovation. Long presentation papers are allocated a 30-minute time slot for presentation and questions. Short presentation papers are allocated a 15-minute time slot for presentation and questions. All papers are published in the DATE 10 Proceedings on DVD.

Track IP contains the interactive presentations which are scientific papers that have been reviewed based on the criteria of presenting work in progress.. The Interactive Presentation papers will be presented in 5 separate IP Sessions which will be held in the Exhibition Area of the ICC and will also each be introduced in a brief one-minute presentation during the relevant session prior to the IP Session. These papers are also published in the DATE 10 Proceedings on DVD.

IP = Interactive presentation

2.1 EXECUTIVE SESSION – How to Address Today's Growing System Complexity?

Room – Saal 5, Ground Floor **1130-1300**

Organiser:
Y Zorian,
Virage Logic, US,

Moderator:
Gary Smith
Gary Smith EDA, US

Executives:
Ron Collett,
President & CEO, Numetrics, US
Antun Domic,
Vice President & GM, Synopsys, US
Christoph Heer,
Vice President, Infineon, DE
Paul Greenfield,
CEO, Aspex Semiconductor, UK
Leon Stok,
Vice President, IBM, US
Raj Yavatkar,
Fellow, Intel, US

The widening gap between growing system complexity and designer productivity increasingly limits traditional design tools, methods and flows. This results in several new approaches that work to elevate the limitations of different aspects of system design. Executives from the IC value chain will present the technical and business challenges and the new opportunities in designing today's complex systems.

1300 **LUNCH BREAK**

2.2 EMBEDDED TUTORIAL – Embedded Systems and their Physical Environment – The 'Cyberphysical' View

Room – Konferenz 6 1130-1300

Organiser:
R Ernst, TU Braunschweig, DE

Moderator:
J Sztipanovits, Vanderbilt U, US

Speakers:
J Sztipanovits, Vanderbilt U, US
A Benveniste, INRIA, FR
L Thiele, ETH Zurich, CH

The session shall give an overview on the challenges and trends. The first talk by Janos Sztipanovits will give an overview on the field. The second talk by Albert Benveniste will introduce to modelling and analysis theory focusing on the important area of networked control. The third talk by Lothar Thiele will outline systematic verification and optimisation techniques using a challenging sensor network application.

1300 **LUNCH BREAK**

2.3 Power-Aware Technique for Real-Time Systems

Room – Konferenz 1 1130-1300

Moderators:
C Yiran, Seagate, US
J Henkel, Karlsruhe U, DE

This session includes three papers regarding the power optimisation and temperature-aware scheduling technique for real-time systems. The first paper presents a leakage power optimisation scheme with temperature consideration. The second paper illustrates a method to predict the energy and performance overhead of real-time operating systems. Finally, the third paper talks about how to distribute the idle time intelligently to optimise the working temperature of DVS systems.

1130 **ENERGY-EFFICIENT REAL-TIME TASK SCHEDULING WITH TEMPERATURE-DEPENDENT LEAKAGE**
C-Y Yang and T-W Kuo, National Taiwan U, ROC
J-J Chen and L Thiele, ETH Zurich, CH

1200 **PREDICTING ENERGY AND PERFORMANCE OVERHEAD OF REAL-TIME OPERATING SYSTEMS**
S Penolazzi, I Sander and A Hemani, Royal Institute of Technology (KTH), SE

1230 **TEMPERATURE-AWARE IDLE TIME DISTRIBUTION FOR ENERGY OPTIMIZATION WITH DYNAMIC VOLTAGE SCALING**
M Bao, P Eles and Z Peng, Linkoping University, SE
A Andrei, Ericsson, SE

IPs **IP1-1 AND IP1-2**

1300 **LUNCH BREAK**

2.4 System Level Design of Multicores

Room – Konferenz 2 1130-1300

Moderators:
V Zaccaria, Politecnico di Milano, IT
M Coppola, STMicroelectronics, FR

The session covers the design of NoC-based multicore architectures with emphasis on reliability, low-power and high performance.

1130 **MULTICORE SOFT ERROR RATE STABILIZATION USING ADAPTIVE DUAL MODULAR REDUNDANCY**
R Vadlamani, J Zhao, W Burleson and R Tessier, U of Massachusetts, Amherst, US

1200 **A FULLY-ASYNCHRONOUS LOW-POWER FRAMEWORK FOR GALS NoC INTEGRATION**
Y Thonnart, P Vivet and F Clermidy, CEA-LETI, MINATEC, FR

1230 **SUPPORTING DISTRIBUTED SHARED MEMORY ON MULTI-CORE NETWORK-ON-CHIPS USING A DUAL MICROCODED CONTROLLER**
X Chen, Z Lu and A Jantsch, Royal Institute of Technology (KTH), SE
S Chen, National U of Defense Technology, PRC

1245 **MEDEA: A HYBRID SHARED-MEMORY/MESSAGE-PASSING MULTIPROCESSOR NOC-BASED ARCHITECTURE**
S V Tota, M R Casu, M Ruo Roch, L Rostagno and M Zamboni, Politecnico di Torino, IT

IP **IP1-3**

1300 **LUNCH BREAK**

2.5 Reliability, Simulation, Yield and Enhancement

Room – Konferenz 3 1130-1300

Moderators:
R Aitken, ARM, US
V Singh, Indian Institute of Science (IISc), IN

This session covers some of the recent advances in reliable designs and chip yield improvements. The first paper presents a system level simulation framework to evaluate lifetime SoC reliability. The second and third papers discuss novel yield enhancements techniques. The last paper presents a methodology for improving the reliability of power gated designs.

1130 **AGESIM: A SIMULATION FRAMEWORK FOR EVALUATING THE LIFETIME RELIABILITY OF PROCESSOR-BASED SoCs**
L Huang and Q Xu, The Chinese U of Hong Kong, PRC

1200 **STATISTICAL SRAM ANALYSIS FOR YIELD ENHANCEMENT**
P Zuber, M Miranda, P Dobrovolny and K van der Zanden, IMEC, SSET/DC, BE
J-H Jung, System LSI Division, Samsung Electronics Co, KR

1230 **COST-EFFECTIVE IR-DROP FAILURE IDENTIFICATION AND YIELD RECOVERY THROUGH A FAILURE-ADAPTIVE TEST SCHEME**
M Chen and A Orialoglu, UC San Diego, US

1245 **SCAN BASED METHODOLOGY FOR RELIABLE STATE RETENTION POWER GATING DESIGNS**
S Yang, B Al-Hashimi and S Khursheed, Southampton U, UK
D Flynn, ARM, Cambridge, UK

IP **IP1-4 AND IP1-5**

1300 **LUNCH**

2.6 Advances in Embedded Software Development

Room – Konferenz 4 **1130-1300**

Moderators:
W Ecker, Infineon Technologies, DE
R Domer, UC Irvine, US

Since the complexity of embedded software is increasing even more strongly than HW complexity, methods and infrastructure for early SW development are of high importance. In this session, novel approaches for virtual prototyping, analysis, and debugging are presented. A paper on SW development application for highly parallel cores completes the session.

1130 **TLM+ MODELING OF EMBEDDED HW/SW SYSTEMS**
W Ecker, V Esen, R Schwenker, T Steininger and M Velten, Infineon Technologies, DE

1200 **SCENARIO EXTRACTION FOR A REFINED TIMING-ANALYSIS OF AUTOMOTIVE NETWORK TOPOLOGIES**
M Traub, T Streichert and O Krasovytskyy, Daimler, DE
J Becker, Karlsruhe U, DE

1230 **GRAPHICAL MODEL DEBUGGER FRAMEWORK FOR EMBEDDED SYSTEMS**
K Zeng, Y Guo and C K Angelov, Southern Denmark U, DK

1245 **IP ROUTING PROCESSING ON GPU**
S Mu and Y S Deng, Tsinghua U, PRC
X Zhang, Fudan U, PRC
N Zhang and J Lu, Wisconsin-Madison U, US
S Zhang, NVidia Corporation, US

IP **IP1-6**

1300 **LUNCH BREAK**

2.7 Memory Stacking and Cooling Solutions

Room – Konferenz 5 1130-1300

Moderators:
H Li, NYU, US
P Marchal, IMEC, BE

Stacking memory with logic provides fast and low power access to high density memories, thereby disruptively changing the basic assumptions of architecture and software design. The first paper introduces a wide DRAM architecture and its integration into a multiprocessor system. The impact of 3D Integration on multiprocessor software programming is highlighted in a second paper. Advanced cooling solutions are required to remove the heat from the 3D stacks. The last two papers respectively introduce a liquid cooling management technique and the use of thin film thermoelectric cooling.

1130 **AN EFFICIENT DISTRIBUTED MEMORY INTERFACE FOR MANY-CORE PLATFORM WITH 3D STACKED DRAM**
I Loi and L Benini, Bologna U, IT

1200 **EFFICIENT OPENMP DATA MAPPING FOR MULTICORE PLATFORMS WITH VERTICALLY STACKED MEMORY**
A Marongiu, M Ruggiero and L Benini, DEIS – Bologna U, IT

1215 **ENERGY-EFFICIENT VARIABLE-FLOW LIQUID COOLING IN 3D STACKED ARCHITECTURES**
A K Coskun and T Simunic Rosing, UC San Diego, US
D Atienza, EPF Lausanne, CH
T Brunschwiler, IBM Zurich, CH

1245 **OPTIMIZATION OF THIN-FILM THERMOELECTRIC COOLER BASED ON-CHIP ACTIVE COOLING SYSTEM**
J Long and S Ogrenci Memik, Northwestern U, US

IP **IP1-7**

1300 **LUNCH**

2.8 PANEL SESSION – Are we there yet? Has System Assembly from IP Blocks Become Like Connecting LEGO Blocks?

Room – Exhibition Theatre, Ground Floor 1130-1300

Organiser:
F Schirrmeister, Synopsys, DE

Moderator:
B Moyer, TechFocus Media, USA

Panellists:
J Kunkel, Synopsys, DE
C Rowen, Tensilica, US
E Haritan, CoWare, US
Y Tanurhan, Virage Logic, US

This panel will explore the trends in IP re-use and discuss where IP blocks end and systems start. Furthermore, it will also explore the trends in IP-reuse and assembly, assess the state of the art of IP assembly and co-simulation standards like IP-XACT and OSCI TLM-2.0. Starting from IP assembly approaches at the RT-level, the panel will chart the direction where IP assembly will go from here towards re-use and assembly at the transaction level.

1300 **LUNCH BREAK**

3.1 EXECUTIVE SESSION – The Impact of Nanometer Technologies on Manufacturability on Yield

Room – Saal 5, Ground Floor **1430-1600**

Organiser:
Yervant Zorian,
Virage Logic, US

Moderator:
Peggy Aycinena,
EDA Weekly, US

Executives:
C J Clark,
CEO & President, Intellitech, US
Pierre Garnier,
Vice President & GM, Texas Instruments, FR
Subi Kengeri,
Vice President, Globalfoundries, US
Joe Macri,
Vice President & CTO, AMD, US
Joe Sawiki,
VP & GM, Mentor Graphics, US
Naveed Sherwani,
President & CEO, Open Silicon, US

Today's nanometer semiconductor fabrication processes result in susceptibility levels that negatively impact process manufacturability and yield, and hence lengthen the SoC production ramp-up period, and affect profitability. To optimise manufacturability and reach acceptable yield levels, the industry needs advanced optimisation solutions. The executives in session will discuss such solutions and their economic impact.

1600 **BREAK/IP1**

3.2 Green and Emerging Technologies for Low Power

Room – Saal 5, Ground Floor **1430-1600**

Moderators:
F Kurdahi, UC Irvine, US
T Murgan, Infineon Technologies, DE

This session discusses new technologies for low power circuit and systems design. Three of the papers cover environmentally friendly approaches involving energy harvesting and data center energy consumption optimisation. Three other papers cover emerging techniques for phase shift memories, MEMS switches for power gating, and subthreshold circuits.

1430 **TEMPERATURE-AWARE DYNAMIC RESOURCE PROVISIONING IN A POWER-OPTIMIZED DATACENTER**
E Pakbaznia, M Ghasemazar and M Pedram, Southern California U, US

1500 **FROM TRANSISTORS TO MEMS: THROUGHPUT-AWARE POWER GATING IN CMOS CIRCUITS**
M Henry and L Nazhandali, Virginia Tech, US

1530 **ENERGY- AND ENDURANCE-AWARE DESIGN OF PHASE CHANGE MEMORY CACHE**
Y Joo, D Niu, X Dong, G Sun and Y Xie, Pennsylvania State U, US

1545 **EVALUATION AND DESIGN EXPLORATION OF SOLAR HARVESTED-ENERGY PREDICTION ALGORITHM**
M I Ali and B M Al-Hashimi, Southampton U, UK
J Recas Piorno, DACYA – Madrid Complutense U, ES
D Atienza, EPF Lausanne, CH

IP **IP1-8 and IP1-9**

1300 **LUNCH BREAK**

3.3 Game-Changing Technologies for System Design

Room – Konferenz 1 **1430-1600**

Moderators:
T Simunic Rosing, UC San Diego, US
D Atienza, EPF Lausanne, CH

This session discusses new technologies and design ideas for 3D chips, memories and atomic-scale computing. The first paper presents a self-reference sensing scheme for memories, resolving large bit-to-bit variations of magnetic tunneling junctions. The second paper proposes a Pseudo-CMOS design style for flexible electronics. It uses only mono-type thin-fin transistors, and has a comparable performance than complementary-type designs. The third paper proposes a redundancy scheme improving timing closure and fault tolerance of 3D stacked chips. Finally, the last paper explores the prospect of atomic-scale computing in nonferromagnetic lattices or spin-glasses.

1430 **A NONDESTRUCTIVE SELF-REFERENCE SCHEME FOR SPIN-TRANSFER TORQUE RANDOM ACCESS MEMORY (STT-RAM)**
Y Chen, X Wang and W Zhu, Seagate Technology, US
H Li, Polytechnic Institute of NYU, US
W Xu and T Zhang, Rensselaer Polytechnic Institute, US

1500 **PSEUDO-CMOS: A NOVEL DESIGN STYLE FOR FLEXIBLE ELECTRONICS**
T-C Huang, C-M Lo and K-T Cheng, UC Santa Barbara, US
K Fukuda, T Sekitani and T Someya, Tokyo U, JP
Y-H Yeh, EOL/ITRI, Hsinchu, Taiwan, ROC

1530 **SPINTO: A HIGH-PERFORMANCE SOLVER FOR ENERGY MINIMIZATION IN ISING SPIN-GLASSES**
H J Garcia and I L Markov, U of Michigan, US

1545 **TSV REDUNDANCY: ARCHITECTURE AND DESIGN ISSUES IN 3D IC**
A-C Hsieh and T T Hwang, National Tsing Hua U, ROC
M-T Chang, M-H Tsai, C-M Tseng and H-C Li, Global Unichip Corporation, ROC

IPs **IP1-10, IP1-11, IP1-12 and IP1-13**

1600 **BREAK/IP1**

3.4 Application Development for Multicores

Room – Konferenz 2 **1430-1600**

Moderators:
F Petrot, TIMA Laboratory, FR
G Kornaros, TEI, GR

This session addresses various aspects of energy management in nanometer technologies. From novel variability aware circuit design in sub-threshold region to robust design under ageing, manufacturing variations and noise impact.

1430 **A GPU BASED IMPLEMENTATION OF CENTER-SURROUND DISTRIBUTION DISTANCE FOR FEATURE EXTRACTION AND MATCHING**
A Rathi, M DeBole, W Ge, R Collins and V Narayanan, The Pennsylvania State U, US

1500 **PARALLEL SUBDIVISION SURFACE RENDERING AND ANIMATION ON THE CELL BE PROCESSOR**
R Grottesi, Lemon Team C B, ES
M Ruggiero, S Morigi and L Benini, Bologna U, IT

1515 **HETEROGENEOUS VS HOMOGENEOUS MPSOC APPROACHES FOR A MOBILE LTE MODEM**
C Jalier, D Lattard and A A Jerraya, CEA LETI, FR
G Sassatelli, P Benoit and L Torres, LIRMM, FR

1530 **RECURSION-DRIVEN PARALLEL CODE GENERATION FOR MULTI-CORE PLATFORMS**
R Collins, L Carloni and B Vellore, Columbia U, US

1545 **AN INDUSTRIAL DESIGN SPACE EXPLORATION FRAMEWORK FOR SUPPORTING RUN-TIME RESOURCE MANAGEMENT ON MULTI-CORE SYSTEMS**
G Mariani, ALaRI, Lugano U, CH
V Zaccaria, G Palermo and C Silvano, Politecnico di Milano, IT
P Avasare, G Vanmeerbeeck and C Ykman-Couvreur, IMEC, BE

IP **IP1-14**

1600 **BREAK/IP1**

3.5 Advanced System Chip Testing

Room – Konferenz 3 1430-1600

Moderators:
R Dorsch, IBM Deutschland Entwicklung GmbH, DE
E Larsson, Linkoping U, SE

The first paper describes an approach to test multi-gigahertz chips with an FPGA-based low-cost ATE extension. The second paper proposes a sophisticated core test scheduling technique to expose temperature- dependent defects. The last paper explores limitations of CPU-based memory BIST with respect to delay-fault testing.

1430 **STRETCHING THE LIMITS OF FPGA SERDES FOR ENHANCED ATE PERFORMANCE**
A Majid and D Keezer, Georgia Institute of Technology, US

1500 **MULTI-TEMPERATURE TESTING FOR CORE-BASED SYSTEM-ON-CHIP**
Z He, Z Peng and P Eles, Linkoping U, SE

1530 **MEMORY TESTING WITH A RISC MICROCONTROLLER**
A J van de Goor, CompTex and TU Delft, NL
G Gaydadjiev and S Hamdioui, TU Delft, NL

IPs **IP1-15 and IP1-16**

1600 **BREAK/IP1**

3.6 Real-Time Scheduling in Embedded Systems

Room – Konferenz 4 1430-1600

Moderators:
L Almeida, Porto U, PT
P Pop, TU Denmark, DK

This session addresses the problem of real-time scheduling in embedded systems. The first paper proposes a new utilisation-based schedulability bound for Deadline-Monotonic scheduling that supercedes existing bounds, thus reducing their level of pessimism. The second paper includes distance constraints in fixed priorities scheduling arising from tasks that are triggered by messages scheduled non-preemptively on a bus.

As a consequence, the pessimism of the computed upper bounds for the worst-case response times is reduced. The third paper addresses embedded systems composed of several reconfigurable units. In such case, the reconfiguration overhead must be considered in the tasks scheduling. The paper proposes taking into account the specific overhead associated to each transition and thus allows improving the schedulability levels when compared to when the maximum fixed transition overhead is considered.

1430 **CONSTANT-TIME ADMISSION CONTROL FOR DEADLINE MONOTONIC TASKS**
A Masrur, S Chakraborty and G Faerber, TU Munich, DE

1500 **EXPLOITING INTER-EVENT STREAM CORRELATIONS BETWEEN OUTPUT EVENT STREAMS OF NON-PREEMPTIVE SCHEDULED TASKS**
J Rox and R Ernst, TU Braunschweig, DE

1530 **REAL-TIME TASK SCHEDULING UNDER TRANSITION OVERHEADS WITH APPLICATION TO RECONFIGURABLE EMBEDDED SYSTEMS**
H Kooti, E Bozorgzadeh, S-H Liao and L Bao, UC Irvine, US

IP **IP1-17**

1600 **BREAK/IP1**

3.7 Architectural Techniques for Robust Design

Room – Konferenz 5 **1430-1600**

Moderators:
T Austin, U of Michigan, US
C Silvano, Politecnico di Milano, IT

This session presents architectural techniques for robust and efficient design. The first paper proposes a technique for characterising the vulnerability of microprocessor structures to intermittent faults in advanced CMOS processes. The second paper uses novel detection and correction circuits to achieve aging-resilience in pipelined architectures. The third paper proposes an integrated framework for joint design space exploration and co-optimisation of microarchitecture and circuits for digital systems.

1430 **IVF: CHARACTERIZING THE VULNERABILITY OF MICROPROCESSOR STRUCTURES TO INTERMITTENT FAULTS**
S Pan, Y Hu and X Li, Chinese Academy of Sciences, PRC

1500 **AGING-RESILIENT DESIGN OF PIPELINED ARCHITECTURES USING NOVEL DETECTION AND CORRECTION CIRCUITS**
H Dadgour and K Banerjee, UC Santa Barbara, US

1530 **AN INTEGRATED FRAMEWORK FOR JOINT DESIGN SPACE EXPLOREATION OF MICROARCHITECTURE AND CIRCUITS**
O Azizi, J P Stevenson, S J Patel and M Horowitz, Stanford U, US
A Mahesri, Illinois U, Urbana-Champaign, US

IP **IP1-18**

1600 **BREAK/IP1**

3.8 HOT TOPIC - AUTOSAR and Automotive Software Design

Room – Exhibition Theatre, Ground Floor **1430-1600**

Organiser/Moderator:
S Fuerst, BMW Group, DE

The first presentation will explain how BMW migrates to AUTOSAR Basic Software in its current and upcoming product lines. This includes also common functionality that is already today realized as AUTOSAR compliant extensions to the basic software. Further on, BMW's strategy on providing application software as ready-to-integrate AUTOSAR software components is described.

The second presentation will concentrate on the influence of the AUTOSAR methodology on the tools used for the development of automotive SW accordingly to AUTOSAR. To support the goal of AUTOSAR to exchange models between OEMs and suppliers, open source software gets of increasing interest. On the basis of an open tool platform "ARTOP" the application of the methodology will be shown.

The development of complex control unit needs mature and reliable basic software as well as integration support in particular in early phases of the project. In its presentation Elektrobit Automotive will focus on new AUTOSAR basic software features like multi core and functional safety. It will be shown how integration and validation will be enhanced by diagnostic logging and tracing functionalities.

1430 **AUTOSAR – CHALLENGES IN THE DESIGN OF AUTOMOTIVE SW**
S Fuerst, BMW Group, DE

1500 **AUTOSAR AND THE AUTOMOTIVE TOOL CHAIN**
S Voget, Continental Engineering Services, DE

1530 **AUTOSAR BASIC SOFTWARE FOR COMPLEX CONTROL UNITS**
D Diekhoff, Elektrobit Automotive, DE

1600 **BREAK/IP1**

IP1 Interactive Presentations

Room – Exhibition Area, Ground Floor

Each interactive presentation will run on a ten minute rotation (three presentations per session) and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP1-1 **HIGH-FIDELITY MARKOVIAN POWER MODEL FOR PROTOCOLS**
J Cao and A Nymeyer, New South Wales U, AU

IP1-2 **ENERGY-PERFORMANCE DESIGN SPACE EXPLORATION OF SMT ARCHITECTURES EXPLOITING SELECTIVE LOAD VALUE PREDICTIONS**
A Gellert, A Florea and L Vintan, Sibiu U, RO
G Palermo, V Zaccaria and C Silvano, Politecnico di Milano, IT

IP1-3 **ERROR RESILIENCE OF INTRA-DIE AND INTER-DIE COMMUNICATION WITH 3D SPIDERGON STNOC**
V Pasca, L Anghel and C Rusu, TIMA Laboratories, FR
R Locatelli and M Coppolak, STMicroelectronics, FR

IP1-4 **TOWARDS A CHIP LEVEL RELIABILITY SIMULATOR FOR COPPER/LOW-K BACKEND PROCESSES**
M M Bashir and L Milor, Georgia Institute of Technology, US

IP1-5 **NBTI MODELING IN THE FRAMEWORK OF TEMPERATURE VARIATION**
S Khan and S Hamdioui, TU Delft, NL

IP1-6 **RUNASSERT: A NON-INTRUSIVE RUN-TIME ASSERTION FOR PARALLEL PROGRAMS DEBUGGING**
C-N Wen, S-H Chou and T-F Chen, National Chung Cheng U, ROC
T-J Lin, ITRI STC, ROC

IP1-7 **AN RDL-CONFIGURABLE 3D MEMORY TIER TO REPLACE ON-CHIP SRAM**
M Facchini, IMEC and KU Leuven, BE
D Velenis and P Marchal, IMEC, BE
W Dehaene, KU Leuven, BE

IP1-8 **GENTLECOOL: COOLING AWARE PROACTIVE WORKLOAD SCHEDULING IN MULTI-MACHINE SYSTEMS**
R Ayoub, S Sharifi and T Rosing, UC San Diego, US

IP1-9 **TIMING MODELING FOR DIGITAL SUB-THRESHOLD CIRCUITS**
N Lotze, J Goeppert and Y Manoli, Freiburg U - IMTEK, DE

IP1-10 **POWER CONSUMPTION OF LOGIC CIRCUITS IN AMBIPOLAR CARBON NANOTUBE TECHNOLOGY**
M H Ben-Jamaa and G De Micheli, EPF Lausanne, CH
K Mohanram, Rice U, US

IP1-11 **REVERSIBLE LOGIC SYNTHESIS THROUGH ANT COLONY OPTIMIZATION**
M Li, Y Zheng, M S Hsiao and C Huang, Virginia Tech, US

IP1-12 **LOW -POWER FINFET CIRCUIT SYNTHESIS USING SURFACE ORIENTATION OPTIMIZATION**
P Mishra and N K Jha, Princeton U, US

IP1-13 **IMPLEMENTING DIGITAL LOGIC WITH SINUSOIDAL SUPPLIES**
K C Bollapalli, S P Khatri and L Kish, Texas A&M U, US

IP1-14 **A RECONFIGURABLE MULTIPROCESSOR ARCHITECTURE FOR A RELIABLE FACE RECOGNITION IMPLEMENTATION**
A Tumeo, G Palermo, F Ferrandi and D Sciuto, Politecnico di Milano, IT
F Regazzoni, Alari, IT

IP1-15 **A SYSTEMATIC APPROACH TO COMBINED HW/SW SYSTEM TEST**
A Krupp, W Mueller and A Elfeky Paderborn U/C-LAB, DE

IP1-16 **A NEW APPROACH FOR ADAPTIVE FAILURE DIAGNOSTICS BASED ON EMULATION TEST**
S Ostendorff, J Sachsse and H-D Wuttke, TU Ilmenau, DE
S Koehler, Goepel Electronic GmbH, DE

IP1-17 **INTEGRATED END-TO-END TIMING ANALYSIS OF NETWORKED AUTOSAR-COMPLIANT SYSTEMS**
K Lakshmanan, G Bhatia and R Rajkumar, Carnegie Mellon U, US

IP1-18 **SCALABLE STOCHASTIC PROCESSORS**
S Narayanan, J Sartori, R Kumar and D L Jones, U of Illinois at Urbana Champaign, US

4.1 EXECUTIVE SESSION – Impacts of Continuous Scaling on the Semiconductor Industry

Room – Saal 5, Ground Floor **1700-1830**

Organiser:
Y Zorian,
Virage Logic, US,

Moderator:
Nic Mockhoff,
EE Times, US

Executives:
Jack Harding,
Chairman, President & CEO, eSilicon, US
Sami Issa,
Director, ATIC, UAE
Maria Marced,
President, TSMC Europe, NL
Alex Shubat,
President & CEO, Virage Logic, US
Rene Penning de Vries,
Senior VP & CTO, NXP, NL
Cheng-Wen Wu,
Vice President, ITRI, Taiwan, ROC

The continuously scaling semiconductor technology with its 28nm and below can dramatically impact business performance of semiconductor industry. It can also significantly affect age-old IC development flows. The executives in this session will discuss future trends and upcoming changes in the semiconductor industry and their impact on the IC value chain.

1830 **CLOSE**

4.2 Variability Aware Low Power Design

Room – Konferenz 6 **1700-1830**

Moderators:
M Miranda, IMEC, BE
T Ishihara, Kyushu U, JP

This session presents novel low power circuit, architecture and system level design techniques for technology scaling induced problems. Challenging power critical components in todays SoCs are used as drivers such as FPGA, memories and power delivering networks.

1700 **AVGS-MUX STYLE: A NOVEL TECHNOLOGY AND DEVICE INDEPENDENT TECHNIQUE FOR REDUCING POWER AND COMPENSATING PROCESS VARIATIONS IN FPGA FABRICS**
B Kheradmand-Boroujeni and C Piguet, CSEM, CH
Y Leblebici, EPF Lausanne, CH

1730 **ON THE EFFICACY OF WRITE-ASSIST TECHNIQUES IN LOW VOLTAGE NANOSCALE SRAMS**
V Chandra, C Pietrzyk and R Aitken, ARM, US

1800 **OPTIMIZING THE POWER DELIVERY NETWORK IN DYNAMICALLY VOLTAGE SCALED SYSTEMS WITH UNCERTAIN POWER MODE TRANSITION TIMES**
H Jung and M Pedram, Southern California U, US

IPs **IP2-1 and IP2-2**

1830 **CLOSE**

4.3 Performance Estimation and Runtime Management of MPSoCs

Room – Konferenz 1 **1700-1830**

Moderators:
M Berekovic, TU Braunschweig, DE
A Pimentel, Amsterdam U, NL

This session addresses performance estimation and runtime management issues for MPSoCs. The first paper concerns resource allocation at run-time, allowing multiple real-time applications to run simultaneously on a heterogeneous MPSoC. The second paper proposes two methods to estimate the execution time of a pipelined MPSoC, minimising the use of slow cycle-accurate simulations. Finally, the third paper presents a compiler-based technique for automatic generation of workload models for performance evaluation by means of simulation.

1700 **RUN-TIME SPATIAL RESOURCE MANAGEMENT FOR REAL-TIME APPLICATIONS ON HETEROGENEOUS MPSoCs**
T D Ter Braak, P K F Hoelzenspies, J Kuper, J L Hurink and G J M Smit, Twente U, NL

1730 **RAPID RUNTIME ESTIMATION METHODS FOR PIPELINED MPSoCs**
H Javaid, A Janapsatya, M Shihabul Haque and S Parameswaran, New South Wales U, AU

1800 **AUTOMATIC WORKLOAD GENERATION FOR SYSTEM-LEVEL EXPLORATION BASED ON MODIFIED GCC COMPILER**
J Kreku and K Teinsyrja,
VTT Technical Research Center of Finland, FI

IP **IP2-3**

1830 **CLOSE**

4.4 Application of Reconfigurable and Adaptive Systems

Room – Konferenz 2 **1700-1830**

Moderators:
C Heer, Infineon Technologies AG, DE
M Huebner, Karslruhe U, DE

Starting from packet classification in NoC the session covers innovative memory and motion estimation architectures and concludes with a novel FPGA application in bio-chemistry.

1700 **A RAPID PROTOTYPING SYSTEM FOR ERROR-RESILIENT MULTI-PROCESSOR SYSTEMS-ON-CHIP**
M May and N Wehn, Kaiserslautern U, DE
A Bouajila, J Zeppenfeld, W Stechele and A Herkersdorf, TU Munich, DE
D Ziener and J Teich, Erlangen-Nuremberg U, DE

1715 **LEARNING-BASED ADAPTATION TO APPLICATIONS AND ENVIRONMENTS IN A RECONFIGURABLE NETWORK-ON-CHIP**
J-S Shen, C-H Huang and P-A Hsiung,
National Chung Cheng U, ROC

1730 **APPLICATION-SPECIFIC MEMORY PERFORMANCE OF A HETEROGENEOUS RECONFIGURABLE ARCHITECTURE**
S Whitty, B Hurlburt, H Sahlbach and R Ernst,
TU Braunschweig, DE
W Putzke-Roeming, Deutsche Thomson OHG, DE

1745 **A RECONFIGURABLE HARDWARE FOR ONE BIT TRANSFORM BASED MULTIPLE REFERENCE FRAME MOTION ESTIMATION**
A Akin, G Sayilar and I Hamzaoglu, Sabanci U, TR

1800 **ULTRA-HIGH THROUGHPUT STRING MATCHING FOR DEEP PACKET INSPECTION**
A Kennedy, X Wang and Z Liu, Dublin City U, IE
B Liu, Tsinghua U, PRC

1815 **A HMMER HARDWARE ACCELERATOR USING DIVERGENCES**
J F Eusse Giraldo, R Pezzuol Jacobi and A C Magalhaes Alves De Melo, Brasilia U, BR
N Moreano, Federal U of Mato Grosso Do Sul, BR

IP **IP2-4 and IP2-5**

1830 **CLOSE**

4.5 Wearout and Process Variation Mitigation and Modelling

Room – Konferenz 3 1700-1830

Moderators:
S Kundu, Massachusetts U, US
A El-Maleh, U of Petroleum and Minerals, SA

The first paper in this session discusses an effective technique that extends the MTTF by exploiting the idle time of functional units in microprocessors. The second paper presents new technique for predicting circuits propagation delay in the presence of process variation. The third paper discusses an accurate analytical model to predict the delay of combinational gates subject TDDB, and the last paper presents static and dynamic stability improvements to SRAMS that minimise the impact of process variation.

1700 **PROACTIVE NBTI MITIGATION FOR BUSY FUNCTIONAL UNITS IN OUT-OF-ORDER MICROPROCESSORS**
L Li, Y Zhang and J Yang, Pittsburgh U, US
J Zhao, Nanjing U, JP

1730 **CIRCUIT PROPAGATION DELAY ESTIMATION THROUGH MULTIVARIATE REGRESSION-BASED MODELING UNDER SPATIO-TEMPORAL VARIABILITY**
S Ganapathy, R Canal and A Rubio, UP Catalunya, ES
A Gonzalez,
UP Catalunya and Intel Barcelona Research Center, ES

1800 **ANALYTICAL MODEL FOR TDDB-BASED PERFORMANCE DEGRADATION IN COMBINATIONAL LOGIC**
M Choudhury and K Mohanram, Rice U, US
V Chandra and R Aitken, ARM, US

1815 **STATIC AND DYNAMIC STABILITY IMPROVEMENT STRATEGIES FOR 6T CMOS LOW-POWER SRAMS**
B Alorda, G Torrens, S Bota and J Segura,
Illes Balears U, ES

IP **IP2-6**

1830 **CLOSE**

4.6 Model Based Design of Embedded Systems

Room – Konferenz 4 1700-1830

Moderators:
C Kirsch, Salzburg U, AT
A Benveniste, INRIA, FR

Model-based foundations, methods, and tools for principled embedded system and software design addressing: modelling, testing, verification, validation, integration, and/or deployment. Model-based system and software architectures and infrastructure addressing: abstractions, composability and compositionality, and/or virtualisation.

1700 **TEST FRONT LOADING IN EARLY STAGES OF AUTOMOTIVE SOFTWARE DEVELOPMENT BASED ON AUTOSAR**
A Michailidis, U Spieth, T Ringler and B Hedenetz, Daimler AG, DE
S Kowalewski, RWTH-Aachen U, DE

1730 **A PROPOSAL FOR REAL-TIME INTERFACES IN SPEEDS**
P Bhaduri, Indian Institute of Technology Guwahati, IN
I Stierand, Oldenburg U, DE

1800 **SCENARIO-BASED ANALYSIS AND SYNTHESIS OF REAL-TIME SYSTEMS USING UPPAAL**
K G Larsen, S Li, B Nielsen, Aalborg U, DK

1830 **CLOSE**

4.7 Extraction and Model Order Reduction

Room – Konferenz 5 **1700-1830**

Moderators:
T Dhaene, Ghent U, BE
L M Silveira, INESC ID / IST – TU Lisbon, PT

The papers in this session deal with various problems in interconnect extraction and compression of the resulting models. The first two papers address important issues in extraction, presenting novel and efficient methods to account for the effect of variations and the presence of the substrate in 3D interconnects. The last two papers discuss improvements in sampling based order reduction and passivity enforcement in boundary element simulations of interconnect systems.

1700 **VARIATION-AWARE INTERCONNECT EXTRACTION USING STATISTICAL MOMENT PRESERVING MODEL ORDER REDUCTION**
T A El-Moselhy and L Daniel, MIT, US

1730 **EFFICIENT 3D HIGH-FREQUENCY IMPEDANCE EXTRACTION FOR GENERAL INTERCONNECTS AND INDUCTORS ABOVE A LAYERED SUBSTRATE**
N Srivastava, Mentor Graphics Corporation, US
R Suaya, Mentor Graphics Corporation, FR
K Banerjee, UC Santa Barbara, US

1800 **HORUS - HIGH-DIMENSIONAL MODEL ORDER REDUCTION VIA LOW MOMENT-MATCHING UPGRADED SAMPLING**
J Fernandez Villena, INESC ID / IST - TU Lisbon, PT
L M Silveira, INESC ID / IST - TU Lisbon / Cadence Research Labs, PT

1815 **ON PASSIVITY OF THE SUPER NODE ALGORITHM FOR EM MODELING OF INTERCONNECT SYSTEMS**
M Ugryumova, TU Eindhoven, NL
W H A Schilders, TU Eindhoven and NXP Semiconductors, NL

IP **IP2-7**

1830 **CLOSE**

COOL ELECTRONIC SYSTEMS DAY

WEDNESDAY 10 MARCH, 2010

0730 **REGISTRATION and SPEAKERS' BREAKFAST**

5.1 PANEL SESSION – The Road to Energy-Efficient Systems: From Hardware-Driven to Software-Defined

Room – Saal 5, Ground Floor **0830-1000**

Organiser/Moderator:
G Fettweis, TU Dresden, DE

Panellists:
H Meyr, RWTH Aachen, DE
J M Rabaey, UC Berkeley, US
G Teepe, Globalfoundries, DE
K Vissers, Xilinx, US
W Fichtner, ETH Zurich, CH

Innovations in micro and nano technology form the basis of modern ICT. However, the steady growth in the ICT sector has meanwhile a significant ecological footprint: 2% of global CO2 emissions are due to ICT systems already today - one fourth of the emissions caused by cars. The energy costs for running ICT infrastructure have turned into a significant economical factor. The most urgent challenge in the area of micro and nanotechnology is therefore to massively increase energy efficiency, in particular for ICT as a key sector for economic growth. Significant improvements in this area can only be achieved through disruptive innovations and new system approaches, which rely on a combination of excellent research & development and world leading know-how of semiconductor production.

But will hardware be the driver to fulfill these requirements and software has to adapt to whatever hardware concepts are developed? Or should the ability to program systems energy-efficiently define the design of the hardware architecture? This session will present the different perspectives on the problem and try to bring both sides together.

1000 **EXHIBITION BREAK/IP2**

5.2 Automating Verification with Simulation, Properties and Assertions

Room – Konferenz 6 **0830-1000**

Moderators:
V Bertacco, U of Michigan, US
M Lajolo, NEC Labs, US

The session is centered on fast and automatic solutions in functional validation and verification. The first presentation evaluates the quality of user-defined functional properties. The second work is a semi-formal solution for microprocessor verification. The following contribution improves SAT-based bounded model checking in verifying a pool of properties. The last paper provides a fast cache simulation technique.

0830 **VACUITY ANALYSIS FOR PROPERTY QUALIFICATION BY MUTATION OF CHECKERS**
L Di Guglielmo, F Fummi and G Pravadelli, Verona U, IT

0900 **AN ABSTRACTION-GUIDED SIMULATION APPROACH USING MARKOV MODELS FOR MICROPROCESSOR VERIFICATION**
T Zhang, T Lv, X-W Li, Chinese Academy of Sciences, PRC

0930 **EFFICIENT DECISION ORDERING TECHNIQUES FOR SAT-BASED TEST GENERATION**
M Chen, X Qin and P Mishra, Florida U, US

0945 **DEW: A FAST LEVEL 1 CACHE SIMULATION APPROACH FOR FIFO REPLACEMENT POLICY**
M Shihabul Haque, J Peddersen, A Janapsatya and S Parameswaran, New South Wales U, AU

IP **IP2-8 and IP2-9**

1000 **EXHIBITION BREAK/IP2**

5.3 Power Optimisation and Estimation for Flash and CMOS Technologies

Room – Konferenz 1 **0830-1000**

Moderators:
J Chen, ETH Zurich, CH
M Poncino, Politecnico di Torino, IT

This session first presents a power estimation framework for flash memories; the remaining papers deal with static and dynamic power optimisation for digital CMOS designs, and low-power design methodologies for analogue primitives.

0830 **FLASHPOWER: A DETAILED POWER MODEL FOR NAND FLASH MEMORY**
V Mohan, S Gurumurthi and M R Stan, Virginia U, US

0900 **POWER OPTIMIZATION DESIGN IN CMOS OP-AMPS WITH SUB-SPACE BASED GEOMETRIC PROGRAMMING**
W Gao, York U, Toronto, CA

0930 **POWER GATING DESIGN FOR STANDARD-CELL-LIKE STRUCTURED ASICS**
S-Y Chen, R-B Lin, H-H Tung and K-W Lin, Yuan Ze U, Taiwan, ROC

0945 **DUAL-VTH LEAKAGE REDUCTION WITH FAST CLOCK SKEW SCHEDULING ENHANCEMENT**
M Tie, H Dong, T Wang and X Cheng, Peking U, PRC

IPs **IP2-10 and IP2-11**

1000 **EXHIBITION BREAK/IP2**

5.4 Automotive Systems: Mastering Complexity and Uncertainty

Room – Konferenz 2 0830-1000

Moderators:
J Becker, U Karlsruhe (TH), DE
L Fanucci, Pisa U, IT

Modern automotive systems designs must deal with complexity and uncertainty at all levels, from system modeling to hardware design and optimisation. Featured papers present methods to optimise architecture design and to early catch specification and performance issues, avoiding large redesign cycles.

0830 **A HIGH VOLTAGE CMOS VOLTAGE REGULATOR FOR AUTOMOTIVE ALTERNATORS WITH PROGRAMMABLE FUNCIONALITIES AND FULL REVERSE POLARITY CAPABILITY**
G Pasetti and L Fanucci, Pisa U, IT
F Tinfena, R Serventi and P D'Abramo, austriamicrosystems AG, IT
P Tisserand, P Chassard and L Labiste, Valeo Equipements Electriques Moteur, FR

0900 **DESIGN OF AN AUTOMOTIVE TRAFFIC SIGN RECOGNITION SYSTEM TARGETING A MULTI-CORE SOC IMPLEMENTATION**
M Mueller, A Braun, J Gerlach and W Rosenstiel, Tuebingen U, DE
D Nienhuser, J M Zollner and O Bringmann, FZI Karlsruhe, DE

0915 **SIMULATION-BASED VERIFICATION OF THE MOST NETINTERFACE SPECIFICATION REVISION 3.0**
A Braun and O Bringmann, FZI Karlsruhe, DE
D Lettnin and W Rosenstiel, Tuebingen U, DE

0930 **HOLISTIC SIMULATION OF FLEXRAY NETWORKS BY USING RUN-TIME MODEL SWITCHING**
M Karner, C Steger and R Weiss, TU Graz, AT
E Armengaud, The Virtual Vehicle Competence Center, AT

0945 **COMPUTING ROBUSTNESS OF FLEXRAY SCHEDULES TO UNCERTAINTIES IN DESIGN PARAMETERS**
A Ghosal and H Zeng, General Motors R&D, US
Y Ben-Haim, Technion - Israel Institute of Technology, IL
M Di Natale, Scuola Superiore S Anna, IT

IP **IP2-12**

1000 **EXHIBITION BREAK/IP2**

5.5 EMBEDDED TUTORIAL – Adapting to Adaptive Testing

Room – Konferenz 3 0830-1000

Organiser:
E J Marinissen, IMEC, BE

Moderator:
J Rivoir, Verigy, DE

Speakers:
A Singh, Auburn U, US
D Glotter, M Esposito, Optimal Test, IL
J Carulli, A Nahar, K Butler, Texas Instruments, US
C Portelli, D Appello, ST Microelectronics, IT

Adaptive testing is a generic term for a number of techniques which aim at improving the test quality and/or reducing the test application costs. In adaptive tests, the test content or pass/fail limits are not fixed as in conventional tests, but dependent on other test results of the currently or previously tested chips. Part-average testing, outlier detection, and neighbourhood screening are just a few examples of adaptive testing. With this Embedded Tutorial, we are offering an introduction to this topic, which is hot in the test community, to the wider DATE audience.

1000 **EXHIBITION BREAK/IP2**

5.6 Virtualisation Technologies

Room – Konferenz 4 **0830-1000**

Moderators:
A Brinkmann, Paderborn U, DE
M Kreiten, AMD, DE

Virtualisation technology is winning traction, both in academia and industry. While it is already widely deployed in the context of server virtualisation, there are still a lot of open topics concerning its usage in embedded systems and the collaboration between server, network, and storage virtualisation. This topic presents recent results in storage virtualisation, building block-based simulation, virtualisation for embedded systems, and unified manageability.

0830 **USING FILE SYSTEM VIRTUALIZATION TO AVOID METADATA BOTTLENECKS**
E Artiaga, BSC-CNS - Barcelona Supercomputing Center, ES
T Cortes, BSC-CNS - Barcelona Supercomputing Center and UP Catalonia, ES

0900 **AN ACCURATE SYSTEM ARCHITECTURE REFINEMENT METHODOLOGY WITH MIXED ABSTRACTION-LEVEL VIRTUAL PLATFORM**
Z-M Hsu, J-C Yeh and I-Y Chuang, Industrial Technology Research Institute Hsinchu, Taiwan, ROC

0930 **NON-INTRUSIVE VIRTUALIZATION MANAGEMENT USING LIBVIRT**
M Bolte, M Sievers, G Birkenheuer, O Niehoerster and A Brinkmann, Paderborn U, DE

IP **IP2-13**

1000 **EXHIBITION BREAK/IP2**

5.7 Variability Reliability and Thermal Trade-Offs for Low-Power Design

Room – Konferenz 5 **0830-1000**

Moderators:
A Macii, Politecnico di Torino, IT
M Lopez-Vallejo, UP Madrid, ES

This session presents different approaches to deal with strong variability in current sub-micron low-power technologies, like process and temperature variations, circuit aging.

0830 **PROCESS VARIATION AND TEMPERATURE-AWARE RELIABILITY MANAGEMENT**
C Zhuo, D Blaauw and D Sylvester, U of Michigan, Ann Arbor, US

0900 **OPTIMIZED SELF-TUNING FOR CIRCUIT AGING**
E Mintarno, J Skaf, S Boyd, R W Dutton and S Mitra, Stanford U, US
R Zheng, J Velamala and Y Cao, Arizona State U, US

0930 **INVESTIGATING THE IMPACT OF NBTI ON DIFFERENT POWER SAVING CACHE STRATEGIES**
A Ricketts and V Narayanan, The Pennsylvania State U, US
J Singh and D Pradhan, Bristol U, UK

IPs **IP2-14 and IP2-15**

1000 **EXHIBITION BREAK/IP2**

IP2 Interactive Presentations

Room – Exhibition Area, Ground Floor

Each interactive presentation will run on a ten minute rotation (three presentations per session) and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP2-1 **ENERGY-ORIENTED DYNAMIC SPM ALLOCATION BASED ON TIME-SLOTTED CACHE CONFLICT GRAPH**
W Huan, Z Yang, M Chen and L Ming, Southeast U, PRC

IP2-2 **ENHANCED Q-LEARNING ALGORITHM FOR DYNAMIC POWER MANAGEMENT WITH PERFORMANCE CONSTRAINT**
W Liu, Y Tan and Q Qiu, Binghamton U, US

IP2-3 **PARALLEL SIMULATION OF SYSTEMC TLM 2.0 COMPLIANT MPSOC ON SMP WORKSTATIONS**
A Mello, I Maia, A Greiner and F Pecheux, LIP6, UPMC, FR

IP2-4 **HIGH SPEED CLOCK RECOVERY FOR LOW-COST FPGAS**
I Haller and Z F Baruch, TU Cluj-Napoca, RO

IP2-5 **DEMONSTRATION OF AN IN-BAND RECONFIGURATION DATA DISTRIBUTION AND NETWORK NODE RECONFIGURATION**
U Pross and S Goller, Core Mountains GmbH, DE
E Markert, M Juettner and U Heinkel, TU Chemnitz, DE
J Knaeblein and A Schneider, Alcatel-Lucent, DE

IP2-6 **PROGRAMMABLE AGING SENSOR FOR AUTOMOTIVE SAFETY-CRITICAL APPLICATIONS**
J C Vazquez and V Champac, INAOE, MX
I C Teixeira, M B Santos and J P Teixeira, INESC-ID/IST, Lisbon, PT

IP2-7 **PASSIVE REDUCED ORDER MODELING OF MULTIPORT INTERCONNECTS VIA SEMIDEFINITE PROGRAMMING**
Z Mahmood, B Bond, T Moselhy, A Megretski and L Daniel, MIT, US

IP2-8 **GOLDMINE: AUTOMATIC ASSERTION GENERATION USING DATA MINING AND STATIC ANALYSIS**
S Vasudevan, D Sheridan, D Tcheng, S Patel, T Tuohy and D Johnson, U of Illinois at Urbana Champaign, US

IP2-9 **ASSERTION-BASED VERIFICATION OF RTOS PROPERTIES**
M Oliveira, W Mueller and H Zabel, PaderbornU/C-LAB, DE

IP2-10 **POST-PLACEMENT TEMPERATURE REDUCTION TECHNIQUES**
W Liu and A Nannarelli, TU Denmark, DK
A Calimera, M Poncino and E Macii, Politecnico di Torino, IT

IP2-11 **CLOCK GATING APPROACHES BY IOEX GRAPHS AND CLUSTER EFFICIENCY PLOTS**
J Srinivas, Penn State U, US
S Jairam, Texas Instruments, IN

IP2-12 **TIMING MODELING AND ANALYSIS FOR AUTOSAR-BASED SOFTWARE DEVELOPMENT - A CASE STUDY**
K Klobedanz, C Kuznik, A Thuy and W Mueller, Paderborn U/C-LAB, DE

IP2-13 **DESIGN OF A REAL-TIME OPTIMIZED EMULATION METHOD**
T Kerstan and M Oertel, Paderborn U, DE

IP2-14 **BENCHMARKING OF PARAMETER EXTRACTION STRATEGIES FOR CAPTURING INTRINSIC STATISTICAL VARIABILITY IN BSIM4 AND PSP**
B Cheng, D Dideban, N Moezi, C Millar, G Roy, X Wang, S Roy and A Asenov, Glasgow U, UK

IP2-15 **POWER EFFICIENT VOLTAGE ISLANDING FOR SYSTEMS-ON-CHIP FROM A FLOORPLANNING PERSPECTIVE**
P Ghosh and A Sen, Arizona State U, US

6.1.1 Cool Sensor Networks

Room – Saal 5, Ground Floor **1100-1230**

Organiser:
G Fettweis, TU Dresden, DE

Moderator:
D Hentschel, Fraunhofer Institute for Non-Destructive Testing (ZFP), DE

Wireless sensor networks are becoming more and more prevalent in daily live applications and studies predict that there could be as many as 1000 sensors per person on the planet by 2020. Give that figure, making these systems energy-autonomous, scalable and secure are key design challenges. Each talk in this session will focus on these design aspects and present innovative approaches for next generation wireless sensor networks.

1100 **ALWAYS ENERGY-OPTIMAL MICROSCOPIC WIRELESS SYSTEMS**
J M Rabaey, UC Berkeley, US

1130 **HARDWARE/SOFTWARE DESIGN CHALLENGES OF LOW-POWER NODES FOR CONDITION MONITORING**
H AHLENDORF AND L GOEPFERT, ZMD AG, DE

1200 **SECURITY ASPECTS IN 6LOWPAN NETWORKS**
R Barker, Vodafone Group R&D, DE

1230 **LUNCH BREAK**

6.2 HOT TOPIC – Memristor: Device, Design and Application

Room – Konferenz 6 **1100-1230**

Organiser:
Y Chen, Seagate Technology, US

Moderator:
D Chen, UIUC, US

Speakers:
D Strukov, UC Santa Barbara, US
X Wang, Seagate Technology, US
H Li, NYU, US

In this hot topic session, three experts from both industry and academia will share their thoughts on the past research and development and the future directions of memristor technology, including 1) the new FPGA structure based on memristor technology (Prof. Dmitri Strukov from UC Santa Barbara); 2) some novel memristive devices and their application in data storage and logic, sensing, power management and information security (Dr. Xiaobin Wang from Seagate Technology; 3) and process variation-aware device model of memristor (Prof. Hai (Helen) Li from New York University).

1100 **MONOLITHICALLY STACKABLE HYBRID FPGA**
D Strukov, UCSB, US

1130 **SPINTRONIC MEMRISTOR DEVICES AND APPLICATIONS**
X Wang, Seagate Technology, US

1200 **COMPACT MODEL OF MEMRISTORS AND ITS APPLICATION IN COMPUTING SYSTEMS**
H Li, Poly-NYU, US

1230 **LUNCH BREAK**

6.3 Addressing the Challenge of Technology Scaling

Room – Konferenz 1 1100-1230

Moderators:
J Ahn, Seoul National U, KR
K Goossens, NXP Research, NL

Papers in this session report on problems that occur in future technologies, including those in explorative optical networks-on-chip. For silicon-based SoCs, the synchronisation concern is addressed in a paper by means of a GALS NoC leveraging mesochronous synchronisers. Moreover, a paper provides an overview of future process variation effects that NoCs have to deal with.

In the optical NoC domain, a simulator to study photonic interconnects at the physical, architecture and system layers is presented, as well as a novel technology to remove the bottleneck of light path establishment.

1100 **DESIGN SPACE EXPLORATION OF A COST-EFFECTIVE AND FLEXIBLE MESOCHRONOUS NOC ARCHITECTURE FOR GALS SYSTEMS**
D Ludovici and G N Gaydadjiev, TU Delft, NL
A Strano and D Bertozzi, ENDIF - Ferrara U, IT
L Benini, DEIS - Bologna U, IT

1130 **A METHODOLOGY FOR THE CHARACTERIZATION OF PROCESS VARIATION IN NOC LINKS**
C Hernandez, F Silla and J Duato, UP de Valencia, ES

1200 **PHOENIXSIM: A SIMULATOR FOR PHYSICAL-LAYER ANALYSIS OF CHIP-SCALE PHOTONIC INTERCONNECTION NETWORKS**
J Chan, G Hendry, A Biberman, K Bergman and L Carloni, Columbia U, US

IP **IP3-1**

1100 **LUNCH BREAK**

6.4 Analogue and Mixed-Signal System Implementations

Room – Konferenz 2 1100-1230

Moderators:
V Giannini, IMEC, BE
P D'Abramo, austriamicrosystems, IT

This session presents practical analogue/mixed-signal design experiences intended for wireless and sensor networks applications in CMOS technologies. Papers feature innovative architectures that enhance flexibility, increase power efficiency, and minimise silicon area and costs.

1100 **AN 11.6-19.3MW 0.375-13.6GHZ CMOS FREQUENCY SYNTHESIZER WITH RAIL-TO-RAIL OPERATION**
A Geis, IMEC and Vrije U Brussel, BE
P Nuzzo, UC Berkeley, US
J Ryckaert and J Craninckx, IMEC, BE
Y Rolain and G Vandersteen, Vrije U Brussel, BE

1130 **A COMPACT DIGITAL AMPLITUDE MODULATOR IN 90NM CMOS**
V Chironi, Salento Lecce U, IT
B Debaillie, J Craninckx and M Ingels IMEC, BE
A Baschirotto, Salento Lecce U and Milan-Bicocca U, IT

1145 **A 14 BIT, 280 KS/S CYCLIC ADC WITH 100 DB SFDR**
T Froehlich, V Sharma and M Bingesser, austriamicrosystems, CH

1200 **ULTRA-LOW POWER MIXED-SIGNAL DESIGN PLATFORM USING SUBTHRESHOLD SOURCE-COUPLED CIRCUITS**
A Tajalli and Y Leblebici, EPF Lausanne, CH

IP **IP3-2**

1230 **LUNCH BREAK**

6.5 On-Line Testing Techniques

Room – Konferenz 3 **1100-1230**

Moderators:
P Bernardi, Politecnico di Torino, IT
A Paschalis, Athens U, GR

Coding, circuit-level, and RT-level on-line testing techniques are investigated in this session.

1100 **CLOCK SKEW SCHEDULING FOR SOFT-ERROR-TOLERANT SEQUENTIAL CIRCUITS**
K-C Wu and D Marculescu, Carnegie Mellon U, US

1130 **HW/SW CO-DETECTION OF TRANSIENT AND PERMANENT FAULTS WITH FAST RECOVERY IN STATICALLY SCHEDULED DATA PATHS**
M Schoelzel, TU Brandenburg, DE

1145 **SCALABLE CODEWORD GENERATION FOR COUPLED BUSES**
K Karmarkar and S Tragoudas, Southern Illinois U, Carbondale, US

1215 **AN ADAPTIVE CODE RATE EDAC SCHEME FOR RANDOM ACCESS MEMORY**
C-Y Chen and C-W Wu, National Tsing Hua U, Taiwan, ROC

IPs **IP3-3 and IP3-4**

1230 **LUNCH BREAK**

6.6 Performance Analysis of Embedded Software for MPSoCs

Room – Konferenz 4 **1100-1230**

Moderators:
C Haubelt, Erlangen-Nuremberg U, DE
D Goehringer, Fraunhofer IOSB, DE

In this session, novel approaches in performance analysis of embedded software running on multi-processor systems are presented. The first paper proposes an analysis approach for complex memory access delays specifically for multi-processor systems. A throughput analysis for Kahn Process Networks used for process clustering is presented in the second paper. The third paper presents a composability analysis for applications specified as Kahn Process Networks. The approach presented in the last paper improves response time estimates for tasks that execute in multi-processor systems.

1100 **WORST CASE DELAY ANALYSIS FOR MEMORY INTERFERENCE IN MULTICORE SYSTEMS**
R Pellizzoni and M Caccamo, Illinois U, Urbana-Champaign, US
A Schranzhofer, J-J Chen and L Thiele, ETH Zurich, CH

1130 **THROUGHPUT MODELING TO EVALUATE PROCESS MERGING TRANSFORMATIONS IN KAHN PROCESS NETWORKS**
S Meijer, H Nikolov and T Stefanov, Leiden Institute of Advanced Computer Science (LIACS), NL

1200 **TRACE-BASED KPN COMPOSABILITY ANALYSIS FOR MAPPING SIMULTANEOUS APPLICATIONS TO MPSOC PLATFORMS**
J Castrillon, A Stulova, J Ceng, W Sheng and R Leupers, RWTH Aachen U, DE
R Velasquez, ALaRI, Lugano, CH

1100 **BOUNDING THE SHARED RESOURCE LOAD FOR THE PERFORMANCE ANALYSIS OF MULTIPROCESSOR SYSTEMS**
S Schliecker, M Negrean and R Ernst, TU Braunschweig, DE

IPs **IP3-5 and IP3-6**

1230 **LUNCH BREAK**

6.7 Advances in Logic Synthesis for Reliability and Matching

Room – Konferenz 5 **1100-1230**

Moderators:
M Fujita, Tokyo U, JP
T Villa, Verona U, IT

This session covers recent advances in logic synthesis which are focused on reliability and matching problems. The first paper provides a timing-robust asynchronous code and hardware support for global communication, which also supports fault tolerance. The second paper presents a methodology for large-scale Boolean matching under permutations of inputs and outputs. The third paper introduces a new cut scheme which supports bounded inputs and outputs. The final paper introduces a new data structure and applies it to reliability analysis.

1100 **AN ERROR-CORRECTING UNORDERED CODE AND HARDWARE SUPPORT FOR ROBUST ASYNCHRONOUS GLOBAL COMMUNICATION**
M Y Agyekum and S M Nowick, Columbia U, US

1130 **LARGE-SCALE BOOLEAN MATCHING**
H Katebi and I L Markov, U of Michigan, US

1200 **KL-CUTS: A NEW APPROACH FOR LOGIC SYNTHESIS TARGETING MULTIPLE OUTPUT BLOCKS**
O Martinello Junior, F De Souza Marques, A Inacio Reis and R Perez Ribas, UFRGS, BR

1215 **RALF: RELIABILITY ANALYSIS FOR LOGIC FAULTS - AN EXACT ALGORITHM AND ITS APPLICATIONS**
S Luckenbill, Y-Y Lee, Y Hu, R Majumdar and L He, UCLA, US

IPs **IP3-7 and IP3-8**

1230 **LUNCH**

6.8 PANEL SESSION – The Challenges of Heterogeneous Multi-Core Debug

Room – Exhibition Theatre, Ground Floor 1100-1230

Organiser:
G Martin, Tensilica, US

Moderator:
A Mayer, Infineon, DE

Panellists:
U Steeb, Blue Wonder, DE
D Sobe, NXP, DE
G Fettweis, TU Dresden, DE
S Lauterbach, Lauterbach, Munich, DE

In this panel, designers and researchers who have practical experience with heterogeneous multiprocessor systems, both commercial and research, will draw on those experiences and answer questions such as:

- What works in heterogeneous multiprocessor debug? What are the successful methods and approaches?
- What challenges are encountered in real life?
- Would new standards help meet the challenges? Are there new standards developments coming?
- How will the methods of today scale to the heterogeneous manycore systems that will come tomorrow?

1230 **LUNCH BREAK**

6.1.2 LUNCH-TIME KEYNOTE AND AWARDS

Room – Saal 5, Ground Floor - 1340-1400 Awards and 1400-1430 Keynote

1340 **Awards Moderator: Z Peng,** Linkoping U, SE

Awards: Presentation of the DATE 09 Best Paper Awards:

Track D - GATE SIZING FOR LARGE CELL-BASED DESIGNS
S Held, Bonn U, DE

Track T - ON LINEWIDTH-BASED YIELD ANALYSIS FOR NANOMETER LITHOGRAPHY
A Sreedhar and S Kundu, Massachusetts U, US

Best IP - ANALYSIS AND OPTIMIZATION OF NBTI INDUCED CLOCK SKEW IN GATED CLOCK TREES
A Chakraborty, G Ganesan, A Rajaram and D Z Pan,
U of Texas at Austin, US

Presentation of the EDAA Outstanding Dissertation Awards

1400

Organiser/Moderator:
G Fettweis, TU Dresden, DE

Keynote Speaker:
Mark Horowitz, Stanford U, US

WHY DESIGN MUST CHANGE: RETHINKING DIGITAL DESIGN

Abstract: The IC industry is facing a huge paradox. On one hand, with the slowing of the performance and power gains provided by scaling, designers need to find new ways of delivering value to their customers. Historically this has meant creating more application specialised chips and systems.

On the other hand the rising NRE costs for chip design (now over $10M/chip) has caused the number of chip design starts to fall. Everyone today seems to be talking about building programmable platforms to ensure the total available market is large enough to justify the chip design costs.

To get out of this paradox, we need to change the way we think about chip design. Reducing digital NRE costs requires moving the end user designers up a level in abstraction. For many reasons I don't believe that either the current SoC, or high-level language effort will succeed. Instead, we should acknowledge that working out the interactions in a complex design is complex, and will cost a lot of money, even when we do it well. The key is to leverage this work over a broader class of chips. This approach leads to the idea of building chip-generators and not chips. That is instead of building a programmable chip to meet a broad class of application needs, you create a virtual programmable chip, that is MUCH more flexible than any real chip. The application designer (the new chip designer) will then configure this substrate to optimise for their application. The generator will take this information and then create the desired chip. While there are many very hard problems that need to be addressed to make this work, but none of them seem insurmountable. In fact I will provide some examples which indicate the promise of this approach - like having the generator choose the core that is the most energy efficient for your application mix.

1430 **END OF SESSION**

7.1 Cool Communications Systems

Room – Saal 5, Ground Floor 1430-1600

Organiser/Moderator:
G Fettweis, TU Dresden, DE

Today's state of the art mobile communications systems already provide considerably high data rates, however, at the cost of rather high energy consumption. Provision of ubiquitous broad band wireless access in a economically and ecologically sustainable fashion creates a new challenge in terms of joint optimisation of spectral efficiency as well as energy efficiency of these systems. Several approaches to meet these new challenges will be presented in the session.

1430 **LOW POWER DESIGN OF THE X-GOLD® SDR 20 BASEBAND PROCESSOR**
W Raab, J Berthold, U Hachmann, D Langen and M Schreiner, Infineon Technologies AG, DE
H Eisenreich, J-U Schluessler and G Ellguth, TU Dresden, DE

1500 **FABULOUS, FRIGHTENING AND TRUE: STORIES OF MULTICORE SOC DESIGN FOR WIRELESS BASEBAND**
C Rowen, Tensilica, US

1530 **LOW POWER MOBILE INTERNET DEVICES USING LTE TECHNOLOGY**
V Aue, Blue Wonder Communications, DE

1600 **BREAK/IP3**

7.2 Statistical Validation at 45nm and Beyond

Room – Konferenz 6 1430-1600

Moderators:
S Verma, Conexant Systems, US
I Harris, UC Irvine, US

The papers in this session explore the impact of variability on circuit characterisation for shrinking device geometries. Monte-Carlo simulation is used to estimate device-level timing. Novel sampling techniques are proposed to reduce the complexity of timing, yield, and stability tradeoff analysis.

1430 **A BLACK BOX METHOD FOR STABILITY ANALYSIS OF ARBITRARY SRAM CELL STRUCTURES**
M Wieckowski, D Sylvester and D Blaauw, U of Michigan, US
V Chandra, S Idgunji, C Pietrzyk and R Aitken, ARM Ltd, US

1500 **LOOP FLATTENING & SPHERICAL SAMPLING: HIGHLY EFFICIENT MODEL REDUCTION TECHNIQUES FOR SRAM YIELD ANALYSIS**
M Qazi, M Tikekar, D Shah and A Chandrakasan, Massachusetts Institute of Technology, US
L Dolecek, UC Los Angeles, US

1530 **PRACTICAL MONTE-CARLO BASE TIMING YIELD ESTIMATION OF DIGITAL CIRCUITS**
J Jaffari and M Anis, Waterloo U, CA

1545 **STATISTICAL STATIC TIMING ANALYSIS USING MARKOV CHAIN MONTE CARLO**
Y Kanoria, S Mitra and A Montanari, Stanford U, US

IP **IP3-9**

1600 **BREAK/IP3**

7.3 Reconfigurable Architectures

Room – Konferenz 1 **1430-1600**

Moderators:
F Ferrandi, Politecnico di Milano, IT
E Bozorgzadeh, UC Irvine, US

This session focuses on architectural approaches exploiting runtime reconfigurability.

1430 **KAHRISMA: A NOVEL HYPERMORPHIC RECONFIGURABLE-INSTRUCTION-SET MULTI-GRAINED-ARRAY ARCHITECTURE**
R Koenig, T Stripf, J Becker, L Bauer, M Shafique and J Henkel, Karlsruhe U, DE

1500 **A RECONFIGURABLE CACHE MEMORY WITH HETEROGENEOUS BANKS**
D Benitez, Las Palmas de Gran Canaria U, ES
J C Moure, D Rexachs and E Luque,
U Autonoma de Barcelona, ES

1530 **EVALUATION OF RUNTIME TASK MAPPING HEURISTICS WITH RSESAME - A CASE STUDY**
K Sigdel, C Galuzzi and K Bertels, TU Delft, NL
M Thompson and A D Pimentel, Amsterdam U, NL

1545 **VAPRES: A VIRTUAL ARCHITECTURE FOR PARTIALLY RECONFIGURABLE EMBEDDED SYSTEMS**
A Jara-Berrocal and A Gordon-Ross, Florida U, US

IP **IP3-10 and IP3-11**

1600 **BREAK/IP3**

7.4 Secure Embedded Systems

Room - Konferenz 2 **1430-1600**

Moderators:
J Quevremont, Thales, FR
L Fesquet, TIMA Laboratory, FR

Making systems secure encompasses many levels of design, including attacks and countermeasures. This session gives a glimpse of the different levels.

It shows one paper on a scalable parallel architecture for asymmetric cryptography. It presents a circuit level countermeasure for side-channel attacks. It presents an application of fault attacks on a RSA implementation. At the system level, it shows attacks and countermeasures to protect the memory bus. It also presents a paper that shows the feasibility of privacy friendly road-tolling.

1430 **PSHS: A SCALABLE PARALLEL SOFTWARE IMPLEMENTATION OF MONTGOMERY MULTIPLICATION FOR MULTICORE SYSTEMS**
Z Chen and P Schaumont, Virginia Tech, US

1500 **BCDL: A HIGH PERFORMANCE BALANCED DPL FOR FPGA WITH GLOBAL PRECHARGE AND NO EARLY-EVALUATION**
M Nassar, Telecom ParisTech, CNRS LTCI (UMR-5141) and Bull TrustWay Division, FR
S Bhasin, J-L Danger, G Duc and S Guilley, Telecom ParisTech, CNRS LTCI (UMR-5141), FR

1515 **FAULT-BASED ATTACK OF RSA AUTHENTICATION**
A Pellegrini, V Bertacco and T M Austin, U of Michigan, US

1530 **DETECTING/PREVENTING INFORMATION LEAKAGE ON THE MEMORY BUS DUE TO MALICIOUS HARDWARE**
A Das, G Memik and A Choudhary, Northwestern U, US
J Zambreno, Iowa State U, US

1545 **AN EMBEDDED PLATFORM FOR PRIVACY-FRIENDLY ROAD CHARGING APPLICATIONS**
J Balasch and I Verbauwhede, KU Leuven, BE

IPs **IP3-12 and IP3-13**

1600 **BREAK/IP3**

7.5 Test Generation, Fault Simulation and Diagnosis

Room – Konferenz 3 **1430-1600**

Moderators:
M Sonza Reorda, Politecnico di Torino, IT
H Obermeir, Infineon, DE

A broad range of test issues is covered in this session: test generation with defect-aware X-filling, speeding-up X-fault simulation and multiple-fault diagnosis.

1430 **DEFECT AWARE X-FILLING FOR LOW-POWER SCAN TESTING**
S Balatsouka, V Tenentes and X Kavousianos, Ioannina U, GR
K Chakrabarty, Duke U, US

1500 **PARALLEL X-FAULT SIMULATION WITH CRITICAL PATH TRACING TECHNIQUE**
R Ubar, S Devadze, J Raik and A Jutman, TU Tallinn, EE

1530 **DIAGNOSIS OF MULTIPLE ARBITRARY FAULTS WITH MASK AND REINFORCEMENT EFFECT**
J Ye, Y Hu and X Li, Chinese Academy of Sciences, PRC

IP **IP3-14**

1600 **BREAK/IP3**

7.6 Applications and Principles for Embedded Multi-Core Systems

Room – Konferenz 4 **1430-1600**

Moderators:
A Hergenhan, Opensynergy, DE
M Hardt, Fraunhofer ISST, DE

The papers address various software issues related to scheduling and programming support for multi-core systems. The first paper proposes a novel parallelisation technique for the development of safety-critical systems in an industrial environment. The second paper suggests a complete algorithm based on constraint programming which solves the allocation and scheduling problem of synchronous data-flow graphs onto multi-core platforms.

The third paper describes a software update service with self-protection capabilities for software components in an embedded system. The last paper proposes an approach to use C++ meta- programming techniques in order to efficiently exploit custom architecture features.

1430 **SKEWED PIPELINING FOR PARALLEL SIMULINK SIMULATIONS**
A Canedo, T Yoshizawa and H Komatsu, IBM Research, JP

1500 **AN EFFICIENT AND COMPLETE APPROACH FOR THROUGHPUT-MAXIMAL SDF ALLOCATION AND SCHEDULING ON MULTI-CORE PLATFORMS**
A Bonfietti, L Benini, M Lombardi and M Milano, DEIS - Bologna U, IT

1530 **A SOFTWARE UPDATE SERVICE WITH SELF-PROTECTION CAPABILITIES**
M Neukirchner, S Stein, H Schrom and R Ernst, TU Braunschweig, DE

1545 **BITSTREAM PROCESSING FOR EMBEDDED SYSTEMS USING C++ METAPROGRAMMING**
R Klemm and G Fettweis, TU Dresden, DE

IP **IP3-15**

1600 **BREAK/IP3**

7.7 Innovative Memory Architectures

Room – Konferenz 5 **1430-1600**

Moderators:
N Hardavellas, Northwestern U, US
D Pnevmatikatos, TU Crete, GR

The session presents innovative memory technologies for non-volatile storage, caching, and networking. The first paper improves the lifetime of phase change memory (PCM) using a novel wear-leveling algorithm that eliminates unnecessary writes. The second paper simplifies cache management using an adaptive replacement algorithm inspired from operating systems. The third paper introduces an area efficient, hash-based TCAM for large-scale network routers.

1430 **INCREASING PCM MAIN MEMORY LIFETIME**
A Peixoto Ferreira, M Zhou, S Bock, R Melhem, B Childers and D Mosse, Pittsburgh U, US

1500 **DUELING CLOCK: ADAPTIVE CACHE REPLACEMENT POLICY BASED ON THE CLOCK ALGORITHM**
A Janapsatya, A Ignjavotic, J Peddersen and S Parameswaran, UNSW, AU

1530 **A MEMORY- AND TIME-EFFICIENT ON-CHIP TCAM MINIMIZER FOR IP LOOKUP**
H Yu and L Bhuyan, UC Riverside, US

IPs **IP3-16, IP3-17 and IP3-18**

1600 **BREAK/IP3**

7.8 PANEL SESSION - Who is Closing the Embedded Software Design Gap?

Room - Exhibition Theatre, Ground Floor **1430-1600**

Organisers/Moderators:
W Ecker, Infineon Technologies, DE
G Martin, Tensilica, US

Panellists:
P Bricaud, Synopsys, FR
R Doemer, UC Irvine, US
S Heinen, Infineon Technologies, DE
J Moessinger, Robert Bosch GmbH, DE
A von Schwerin, Siemens, DE
Y Veller, Mentor Graphics, IL

As pointed out in the ITRS roadmap, the level of embedded software complexity is greater than the pure HW complexity of SoCs when comparing, for example, lines of HDL and C code. Even worse, SW complexity grows faster than HW complexity (Moore's Law) and SW productivity increases more slowly than HW productivity. A new design gap - the gap of embedded software - has appeared.

EDA has now identified ESL as a field with sufficient revenue and revenue growth, but do they really approach the SW productivity challenge?

This panel gives the answer by presenting recent EDS products and solutions in the area of ESW, contrasting them with needs of industry, and discussing ways out of the ESL productivity crisis.

1600 **BREAK/IP3**

IP3 Interactive Presentations

Room – Exhibition Area, Ground Floor **1600-1630**

Each interactive presentation will run on a ten minute rotation (three presentations per session) and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP3-1 **BINARY-TREE WAVEGUIDE CONNECTED TIME/POWER EFFICIENT OPTICAL NETWORK-ON-CHIP**
B Fu, Y Han, H Li and X Li, Chinese Academy of Sciences, PRC

IP3-2 **HIGH-VOLTAGE LOW-POWER DC-DC BUCK REGULATOR FOR AUTOMOTIVE APPLICATIONS**
G Pasetti and L Fanucci, Pisa U, IT
R Serventi, austriamicrosystems AG, AT

IP3-3 **SIMTAG: EXPLOITING TAG BITS SIMILARITY TO IMPROVE THE RELIABILITY OF THE DATA CACHES**
J Kim and S Kim, Korea Advanced Institute of Science and Technology (KAIST), KR

IP3-4 **THE SPLIT REGISTER FILE**
J Abella, J Carretero, P Chaparro and X Vera, Intel Barcelona Research Center, Intel Labs Barcelona – UPC, ES

IP3-5 **MULTITHREADED CODE GENERATION FROM SYNCHRONOUS GUARDED ACTIONS**
K Schneider, J Brandt and D Baudisch, Kaiserslautern U, DE

IP3-6 **RMOT: RECURSION IN MODEL ORDER FOR TASK EXECUTION TIME ESTIMATION IN A SOFTWARE PIPELINE**
N Iqbal and J Henkel, Karlsruhe U, DE

IP3-7 **APPROXIMATE LOGIC SYNTHESIS FOR ERROR TOLERANT APPLICATIONS**
D Shin and S K Gupta, Southern California U, US

IP3-8 **AUTOMATIC MICROARCHITECTURAL PIPELINING**
M Galceran-Oms, J Cortadella and D Bufistov, UP Catalunya, ES
M Kishinevsky, Intel Corporation, US

IP3-9 **NON-LINEAR OPERATING POINT STATISTICAL ANALYSIS FOR LOCAL VARIATIONS IN LOGIC TIMING AT LOW VOLTAGE**
R Rithe and A Chandrakasan, MIT, US
J Gu, A Wang, S Datla, G Gramie and D Buss, Texas Instruments, US

IP3-10 **DYNAMICALLY RECONFIGURABLE REGISTER FILE FOR A SOFTCORE VLIW PROCESSOR**
S Wong, F Anjam and F Nadeem, TU Delft, NL

IP3-11 **FPGA-BASED ADAPTIVE COMPUTING FOR CORRELATED MULTI-STREAM PROCESSING**
M Liu, Justus-Liebig U Giessen, DE and Royal Institute of Technology, SE
Z Lu and A Jantsch, Royal Institute of Technology, SE
W Kuehn, Justus-Liebig U Giessen, DE

IP3-12 **EMA AT DISTANCE: WHAT IS POSSIBLE?**
O Meynard, TELECOM ParisTech and DGA / CELAR, FR
S Guilley, J-L Danger and L Sauvage, TELECOM ParisTech, FR

IP3-13 **IMPROVED COUNTERMEASURE AGAINST ADDRESS-BIT DPA FOR ECC SCALAR MULTIPLICATION**
M Izumi, J Ikegami, K Sakiyama and K Ohta, The University of Electro-Communications, JP

IP3-14 **ENABLE EFFICIENT POST-SILICON DEBUG BY CLUSTERING OF HARDWARE-ASSERTIONS**
M H Neishaburi and Z Zilic, McGill U, CA

IP3-15 **CONSTRAINED POWER MANAGEMENT: APPLICATION TO A MULTIMEDIA MOBILE PLATFORM**
P Bellasi, S Bosisio, M Carnevali and W Fornaciari, Politecnico di Milano, IT
D Siorpaes, STMicroelectronics, IT

IP3-16 **MAPPING SCIENTIFIC APPLICATIONS ON A LARGE-SCALE DATA-PATH ACCELERATOR IMPLEMENTED BY SINGLE-FLUX QUANTUM (SFQ) CIRCUITS**
F Mehdipour, H Kataoka, K Inoue and K Murakami, Kyushu U, JP
H Honda, Institute of Systems, Information Technologies and Nanotechnologies, Fukuoka, JP
I Kataveva, H Akaike and A Fujimaki, Nagoya U, JP

IP3-17 **MB - LITE : A ROBUST, LIGHT-WEIGHT SOFT-CORE IMPLEMENTATION OF THE MICROBLAZE ARCHITECTURE**
T Kranenburg and T G R M Van Leuken, TU Delft, NL

IP3-18 **AUTOMATIC PIPELINING FROM TRANSACTIONAL DATAPATH SPECIFICATIONS**
E Nurvitadhi and J C Hoe, arnegie Mellon U, US
T Kam and S-L L Lu, Intel Corporation, US

8.1 Cool Computing Platforms

Room – Saal 5, Ground Floor **1700-1830**

Organiser:
G Fettweis, TU Dresden, DE

Moderator:
S Krueger, Globalfoundries, DE

Computers are becoming increasingly powerful. But with improved processing power, energy consumption is also increasing. This is why the cost factor for energy consumption of computers cannot be neglected by businesses any longer. Energy preserving technologies are the future. The three talks in this session will present approaches to this problem.

1700 **INCREASING THE POWER EFFICIENCY OF PCS BY IMPROVING THE HARDWARE/OS INTERACTION**
C Schlaeger, AMD, DE

1730 **OPTIMIZE YOUR POWER AND PERFORMANCE YIELDS AND REGAIN THOSE SLEEPLESS NIGHTS**
K Flautner, ARM, US

1800 **DIGITAL STATISTICAL-ANALYSIS USING VHDL**
M Dietrich, Fraunhofer IIS/EAS Dresden, DE

1830 **CLOSE**

8.2 HOT TOPIC – Cross-Layer Optimisation to Address the Dual Challenges of Energy and Reliability

Room – Konferenz 6 **1700-1830**

Organiser/Moderator:
A DeHon, Pennsylvania U, US

This special session describes the vision and the need for new design automation. It summarises findings and vision from a 2009 Computer Community Consortium study of cross-layer reliability. It is organised into four talks.

1700 **A RESILIENCE ROADMAP**
S Nassif, IBM, US

1730 **VISION FOR CROSS-LAYER OPTIMIZATION TO ADDRESS THE DUAL CHALLENGES OF ENERGY AND RELIABILITY**
A DeHon, Pennsylvania U, US

1745 **DESIGN TECHNIQUES FOR CROSS-LAYER RESILIENCE**
N Carter, Intel, US

1815 **CROSS-LAYER RESILIENCE CHALLENGES: METRICS AND OPTIMISATION**
S Mitra, Stanford U, US

1830 **CLOSE**

8.3 System Modelling for Design Space Exploration and Validation

Room – Konferenz 1 **1700-1830**

Moderators:
E Villar, Cantabria U, ES
L Indrusiak, York U, UK

Increasing system complexity widens the design space and dynamic reconfiguration possibilities for embedded systems. The papers in this session present various modelling strategies to constrain and simplify the design space exploration and validate the solutions, in particular with applications to dataflow systems and wireless sensor networks.

1700 **PARETO EFFICIENT DESIGN FOR RECONFIGURABLE STREAMING APPLICATIONS ON CPU/FPGAS**
J Zhu, I Sander and A Jantsch,
Royal Institute of Technology, SE

1730 **AUTOMATED BOTTLENECK-DRIVEN DESIGN-SPACE EXPLORATION OF MEDIA PROCESSING SYSTEM**
Y Yang, M Geilen, T Basten, S Stuijk and H Corporaal,
TU Eindhoven, NL

1800 **USING TRANSACTION LEVEL MODELING TECHNIQUES FOR WIRELESS SENSOR NETWORK SIMULATION**
M Damm, J Moreno, J Haase and C Grimm, TU Vienna, AT

1815 **RTOS-AWARE REFINEMENT FOR TLM2.0-BASED HW/SW DESIGNS**
M Becker, T Xie and W Mueller, Paderborn U / C-LAB, DE
G Di Guglielmo, G Pravadelli and F Fummi, Verona U, IT

IP **IP4-1**

1830 **CLOSE**

8.4 Sensor Networks and Security Technology

Room – Konferenz 2 **1700-1830**

Moderators:
G Manes, Florence U, IT
R Bekkers, Brightsight, NL

This session presents enabling technology for sensor networks and security. Two papers are attack related: one describes a practical security attack, another provides a statistical tool. The other papers describe components: physical unclonable functions, an analogue-to-digital converter, components for UWB and CMOS based pressure sensors.

1700 **A PRACTICAL ATTACK AGAINST HALF-MASKED ASIC AES BASED ON A VARIANCE MODEL**
Y Li, K Sakiyama, D Nakatsu and K Ohta, The U of Electro-Communications, JP
L Batina, KU Leuven, BE and Radboud U, Nijmegen, NL

1730 **NOVEL PHYSICAL UNCLONABLE FUNCTION BASED ON PROCESS AND ENVIRONMENTAL VARIATIONS**
X Wang and M Tehranipoor, Connecticut U, US

1745 **ULTRA LOW-POWER 12-BIT SAR ADC FOR RFID APPLICATIONS**
D de Venuto, DEE - Politecnico di Bari, IT
E Stikvoort, NXP Semiconductors Eindhoven, NL
D Tio Castro and Y Ponomarev, NXP Semiconductors, BE

1800 **A FLEXIBLE UWB TRANSMITTER FOR BREAST CANCER DETECTION IMAGING SYSTEMS**
M Cutrupi, M Crepaldi, M R Casu and M Graziano, Politecnico di Torino, IT

1815 **A PORTABLE MULTI-PITCH E-DRUM BASED ON LARGE-AREA, FLEXIBLE PRINTED PRESSURE SENSORS**
C-M Lo, T-C Huang and K-T Cheng, UC Santa Barbara, US
J Hou and C-Y Chiang, EOL-ITRI, ROC

IP **IP4-2**

1830 **CLOSE**

8.5 Variability and Yield in Analogue and Mixed-Signal Design

Room – Konferenz 3 **1700-1830**

Moderators:
I O'Connor, EC Lyon, FR
M Olbrich, Hannover U, DE

The impact of process variations on analogue circuit performance is increasingly difficult to handle at advanced technology nodes. This session presents new approaches to increase the yield of analogue circuits in the presence of process variations, using deterministic and evolutionary optimisation.

Contributions to this session show how yield analysis can be improved through an efficient sampling approach or by a formal verification method.

A complementary approach shows an accurate method to incorporate reliability issues in circuit simulation. A technique to model and verify the robustness of probabilistic circuits is also presented.

1700 **COMPUTATION OF YIELD-OPTIMIZED PARETO FRONTS FOR ANALOG INTEGRATED CIRCUIT SPECIFICATIONS**
D Mueller-Gritschneder and H Graeb, TU Munich, DE

1730 **A QUASI-LINEAR DETERMINISTIC VARIATION-AWARE CIRCUIT RELIABILITY SIMULATION METHODOLOGY**
E Maricau and G Gielen, KU Leuven, BE

1800 **A GENERAL MATHEMATICAL MODEL OF PROBABILISTIC RIPPLE-CARRY ADDERS**
M S K Lau, K-V Ling, Y-C Chu and A Bhanu, Nanyang Technological U, SG

1815 **AN ACCURATE AND EFFICIENT YIELD OPTIMIZATION METHOD FOR ANALOG CIRCUITS BASED ON COMPUTING BUDGET ALLOCATION AND MEMETIC SEARCH TECHNIQUES**
B Liu and G Gielen, KU Leuven, BE
F V Fernandez, Seville U, ES

IPs **IP4-3 and IP4-4**

1830 **CLOSE**

8.6 Resource-Aware Embedded Code Optimisation

Room – Konferenz 4 **1700-1830**

Moderators:
R Leupers, RWTH Aachen U, DE
F Kienle, TU Kaiserslautern, DE

In this session new resource-aware optimisation approaches integrated into embedded software compilers are presented. The first paper proposes a scheduling algorithm that derives the optimal loop unrolling factor considering data reuse and variable renaming. A compilation technique for stream programs which models code overlay when using scratch pad memories is presented in the second paper. The third paper describes an allocation method of instruction scratch pad memory for preemptive real-time multi-tasking systems. The approach presented in the fourth paper achieves speedup and cost savings by a special purpose compiler for complex arithmetic functions.

1700 **REUSE-AWARE MODULO SCHEDULING FOR STREAM PROCESSORS**
L Wang and X Yang, National Laboratory for Parallel and Distributed Processing, PRC
J Xue, UNSW, AU

1730 **COMPILATION OF STREAM PROGRAMS FOR MULTICORE PROCESSORS THAT INCORPORATE SCRATCH PAD MEMORIES**
W Che and K S Chatha, Arizona State U, US

1800 **PARTITIONING AND ALLOCATION OF SCRATCH-PAD MEMORY FOR PRIORITY-BASED PREEMPTIVE MULTI-TASK SYSTEMS**
H Takase, H Tomiyama and H Takada, Nagoya U, JP

1815 **A SPECIAL-PURPOSE COMPILER FOR LOOK-UP TABLE AND CODE GENERATION FOR FUNCTION EVALUATION**
Y Zhang, P Yedlapalli, S Muralidhara, H Zhao and M Kandemir, Pennsylvania State U, US
L Deng and C Chakrabarti, Arizona State U, US
N Pitsianis and X Sun, Duke U, US

IPs **IP4-5 and IP4-6**

1830 **CLOSE**

8.7 Macromodelling for Thermal and Interconnect Systems

Room – Konferenz 5 **1700-1830**

Organisers/Moderators:
W Schilders, NXP Semiconductors, NL
R Suaya, Mentor Graphics, FR

The papers in this session discuss macromodeling techniques for a number of application domains, including thermal analysis of multi-processor systems, and several flavours of interconnect problems. The first and last paper address modelling and analysis of large linear networks, while the second and third paper discuss techniques for passitivity enforcement and delayed systems.

1700 **GENERAL BEHAVIORAL THERMAL MODELING AND CHARATERIZATION FOR MULTI-CORE MICROPROCESSOR DESIGN**
T Eguia and S Tan, UC Riverside, US
E H Pacheco and M Tirumala, Intel Corp, US

1730 **ON THE CONSTRUCTION OF GUARANTEED PASSIVE MACROMODELS FOR HIGH-SPEED CHANNELS**
A Chinea and S Grivet, Politecnico di Torino, IT
D Deschrijver, T Dhaene and L Knockaert, Ghent U, BE

1800 **EXTENDED HAMILTONIAN PENCIL FOR PASSIVITY ASSESSMENT AND ENFORCEMENT FOR S-PARAMETER SYSTEMS**
Z Ye, Tsinghua U, PRC
L M Silveira, TU Lisbon, IST/INESC-ID, PT
J R Phillips, Cadence Design Systems, US

1815 **EQUIVALENT CIRCUIT MODELING OF MULTILAYERED POWER/GROUND PLANES FOR FAST TRANSIENT SIMULATION**
T Watanabe and H Asai, Shizuoka U, JP

IPs **IP4-7, IP4-8 and IP4-9**

1830 **CLOSE**

Nanoelectronics Special Day

THURSDAY 11 MARCH, 2010

0730 **REGISTRATION and SPEAKERS' BREAKFAST**

9.1 NANOELECTRONICS TUTORIAL – Beyond CMOS

Room – Saal 5, Ground Floor 0830-1000

Organisers:
A M Ionescu, EPF Lausanne, CH
S Mitra, Stanford U, US

Moderators:
A M Ionescu, EPF Lausanne, CH

The Beyond CMOS tutorials encompass key advances in nanowire electronics, design with CMOS variability and advanced system design with CNTs. The first tutorial by Prof. Samuelson will address the rapidly developing field of one-dimensional electronics, where novel materials science and physics phenomena offer new and powerful applications. The second tutorial by Prof. Onodera wi will review recent trend of CMOS variability, including variability characterisation, minimisation and mitigation. Finally, Prof. Mitra will present the variability challenges raised by advanced system design based on novel CNT nanotechnology.

0830 **FUNDAMENTALS OF ONE DIMENSIONAL ELECTRONICS**
L Samuelson, Lund U, SE

0900 **UNDERSTANDING CMOS VARIABILITY FOR MORE MOORE**
H Onodera, Kyoto U, JP

0930 **SYSTEM DESIGN WITH NANO: THE VARIABIILTY CHALLENGE**
S Mitra, Stanford U, US

1000 **EXHIBITION BREAK/IP4**

9.2 Multi-Level, Multi-Domain System Simulation

Room – Konferenz 6 0830-1000

Moderators:
M Zwolinski, Southampton U, UK
P Sanchez, Cantabria U, ES

With ever-increasing system size and complexity, the challenge is to achieve accuracy and confidence in acceptable simulation times. In this session, the modelling abstraction ranges from thermal analysis in the first paper, through assertion-based verification of mixed-signal systems to hardware/software co-simulation in the second and third papers. In the final paper, the problem of parallel simulation for TLM is considered.

0830 **PROPERTIES OF AND IMPROVEMENTS TO TIME-DOMAIN DYNAMIC THERMAL ANALYSIS ALGORITHMS**
X Chen and R P Dick, University of Michigan, US
L Shang, Colorado U at Boulder, US

0900 **TOWARDS ASSERTION-BASED VERIFICATION OF HETEROGENEOUNS SYSTEM DESIGNS**
S Laemmermann, J Ruf, T Kropf and W Rosenstiel, Tuebingen U, DE
A Jesser and L Hedrich, Frankfurt U, DE
A Viehl, FZI Karlsruhe, DE

0930 **AUTOMATIC GENERATION OF SOFTWARE TLM IN MULTIPLE ABSTRACTION LAYERS FOR EFFICIENT HW/SW CO-SIMULATION**
M-H Wu, W-C Lee, C-Y Chuang and R-S Tsay, National Tsing Hua U, ROC

0945 **MODELLING CONSTRUCTS AND KERNEL FOR PARALLEL SIMULATION OF ACCURACY ADAPTIVE TLMS**
R Salimi-Khaligh and M Radetzki, Stuttgart U, DE

IP **IP4-10**

1000 **EXHIBITION BREAK/IP4**

9.3 Language Based Approaches to System Level Design

Room – Konferenz 1 **0830-1000**

Moderators:
J Haase, TU Vienna, AT
D Borrione, TIMA Laboratory, FR

The session is about the use of high level specifications to perform HW/SW co-design, co-generation and verification. The first paper presents extensions to an actor-based model of computation to make it more suitable to the networking domain. The second and third papers propose model transformation techniques to generate code or validate systems described in UML. In the last paper, PSL specifications are applied at the transaction level for design verification.

0830 **EFFICIENT HIGH-LEVEL MODELING IN THE NETWORKING DOMAIN**
C Zebelein, J Falk, C Haubelt and J Teich, Erlangen-Nuremberg U, DE
R Dorsch, IBM Research & Development GmbH, DE

0900 **UML DESIGN FOR DYNAMICALLY RECONFIGURABLE MULTIPROCESSOR EMBEDDED SYSTEMS**
J Vidal, F De Lamotte, G Gogniat and J-P Diguet, European U of Brittany, FR
P Soulard, SODIUS, FR

0930 **CLOSING THE GAP BETWEEN UML-BASED MODELING AND SIMULATION OF COMBINED HW/SW SYSTEMS**
F Mischkalla, D He and W Mueller, Paderborn U/C-LAB, DE

0945 **FORMAL SEMANTICS FOR PSL MODELING LAYER AND APPLICATION TO THE VERIFICATION OF TRANSACTIONAL MODELS**
L Ferro and L Pierre, TIMA Laboratory, FR

IPs **IP4-11 and IP4-12**

1000 **EXHIBITION BREAK/IP4**

9.4 Space and Aeronautics Avionics Application Design

Room – Konferenz 2 0830-1000

Moderators:
S Prudhomme, Airbus, FR
L Soderquist, Saab AB, SE

This session focuses on practical design experiences and innovative methodologies for applications in military or civil space and aeronautics. Presentations span from system level to component level with relevant applications from avionics and space domains. Invited papers highlight problems and possible solutions specific from these fields.

0830 **INVITED PRESENTATION – COTS BASED APPLICATION IN SPACE AVIONICS**
M Pignol, CNES, FR

0900 **WORST-CASE ANALYSIS OF AN INDUSTRIAL AFDX NETWORK**
H Bauer, Airbus Operations, FR
J-L Scharbarg and C Fraboul, IRIT/ENSEEIHT/INPT, Toulouse, FR

0915 **INVITED PRESENTATION – INTEGRATION, COOLING AND PACKAGING ISSUES IN AERONAUTICS AVIONICS PRODUCT**
C Sarno and C Tantolin, Aerospace Division, Thales, FR

0945 **A NEW PLACEMENT ALGORITHM FOR THE MITIGATION OF MULTIPLE CELL UPSETS IN SRAM-BASED FPGAs**
L Sterpone and N Battezzati, Politecnico di Torino, IT

IPs **IP4-13 and IP4-14**

1000 **EXHIBITION BREAK/IP4**

9.5 Design for Test, Diagnosis, and Yield

Room – Konferenz 3 0830-1000

Moderators:
G Mrugalski, Mentor Graphics, US
A Leininger, Infineon, DE

The papers in this session address issues in test compression and yield enhancement. The first paper presents a new method for compaction of functional test sequences, while the second one proposes a built-in self-diagnosis method using on-chip signatures. Finally, the third contribution enhances reconfigurability and yield by optimally inserting and logic in pipelines.

0830 **REDUCING THE STORAGE REQUIREMENTS OF A TEST SEQUENCE BY USING A BACKGROUND VECTOR**
I Pomeranz, Purdue U, US
S M Reddy, Iowa U, US

0900 **BISD: SCAN-BASED BUILT-IN SELF-DIAGNOSIS**
M Elm and H J Wunderlich, Stuttgart U, DE

0930 **ALGORITHMS TO MAXIMIZE YIELD AND ENHANCE YIELD/AREA OF PIPELINE CIRCUITRY BY INSERTION OF SWITCHES AND REDUNDANT MODULES**
M Mirza-Aghatabar, M A Breuer and S K Gupta, Southern California U, US

IP **IP4-15**

1000 **EXHIBITION BREAK/IP4**

9.6 High Level Synthesis

Room – Konferenz 4 0830-1000

Moderators:
F Kurdahi, UC Irvine, US
P Coussy, Bretagne-Sud U, FR

This session presents three different directions in high-level synthesis. The first paper extends pattern recognition to control and data flow graph. The second paper addresses Vth assignment at behavioural level. The last paper in the session introduces a synthesis flow for global area optimisation.

0830 **A GENERALIZED CONTROL-FLOW-AWARE PATTERN RECOGNITION ALGORITHM FOR BEHAVIOR SYNTHESIS**
J Cong, H Huang and W Jiang, UCLA, US

0900 **BEHAVIORAL LEVEL DUAL-VTH DESIGN FOR REDUCED LEAKAGE POWER WITH THERMAL AWARENESS**
J Yu, Z Zhou and J Bian, Tsinghua U, PRC
Q Qu, Maryland U, US

0930 **COORDINATED AREA MINIMIZATION FOR BEHAVIORAL SYNTHESIS UNDER PERFORMANCE CONSTRAINTS**
J Cong, B Liu and J Xu, UCLA, US

IPs **IP4-16 and IP4-17**

1000 **EXHIBITION BREAK/IP4**

9.7 Physical Design Potpourri: DFM, Delay Modelling and Floorplanning

Room – Konferenz 5 0830-1000

Moderator:
J Lienig, TU Dresden, DE
D Stroobandt, Ghent U, BE

Design of nanoscale circuits is becoming more challenging as it requires accurate models and must account for manufacturing issues. The authors of the first paper observe that timing slack can be exploited to allow greater lithography variations in polygonal shapes. Two other DFM optimisations are proposed in the second paper to enhance detailed routing for double patterning technology.

The third paper presents new compact waveform models for standard cells. The final paper reclusters floorplan blocks to optimise system throughput in latency-insensitive designs.

0830 **A METHODOLOGY FOR PROPAGATING DESIGN TOLERANCES TO SHAPE TOLERANCES FOR USE IN MANUFACTURING**
S Banerjee and M Orshansky, U of Texas, Austin, US
K B Agarwal, S R Nassif and C Sze, IBM Research, Austin, US

0900 **ENHANCING DOUBLE-PATTERNING DETAILED ROUTING WITH LAZY COLORING AND WITHIN-PATH CONFLICT AVOIDANCE**
X Gao and L Macchiarulo, U of Hawaii at Manoa, US

0930 **EFFICIENT REPRESENTATION, STRATIFICATION, AND COMPRESSION OF VARIATIONAL CSM LIBRARY WAVEFORMS USING ROBUST PRINCIPLE COMPONENT ANALYSIS**
S Hatami and M Pedram, Southern California U, US

0945 **EXPLOITING LOCAL LOGIC STRUCTURES TO OPTIMIZE MULTI-CORE SOC FLOORPLANNING**
C-H Li, IBM Research, US
S Sonalkar and L P Carloni, Columbia U, US

IPs **IP4-18, IP4-19 and IP4-20**

1000 **EXHIBITION BREAK/IP4**

IP4 Interactive Presentations

Room – Exhibition Area, Ground Floor

Each interactive presentation will run on a ten minute rotation (three presentations per session) and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP4-1 **COST MODELING AND CYCLE-ACCURATE CO-SIMULATION OF HETEROGENEOUS MULTIPROCESSOR SYSTEMS**
S Van Haastregt, E Halm and B Kienhuis, LIACS, Leiden U, NL

IP4-2 **DIFFERENTIAL POWER ANALYSIS ENHANCEMENT WITH STATISTICAL PREPROCESSING**
V Lomne, A Dehbaoui, P Maurine, L Torres and M Robert, LIRMM, FR

IP4-3 **CORRELATION CONTROLLED SAMPLING FOR EFFICIENT VARIABILITY ANALYSIS OF ANALOG CIRCUITS**
J Jaffari and M Anis, Waterloo U, CA

IP4-4 **FORMAL VERIFICATION OF ANALOG/RF CIRCUITS IN THE PRESENCE OF NOISE AND PROCESS VARIATION**
R Narayanan, B Akbarpour and S Tahar, Concordia U, CA
M H Zaki and L C Paulson, U of British Columbia, CA

IP4-5 **TOWARD OPTIMIZED CODE GENERATION THROUGH MODEL-BASED OPTIMIZATION**
A Charfi, C Mraidha, S Gerard and F Terrier, CEA LIST, FR
P Boulet, CNRS/INRIA, FR

IP4-6 **PATH-BASED SCHEDULING IN A HARDWARE COMPILER**
R Gu, U of Maryland College Park, US
A Forin and N Pittman, Microsoft Corporation, US

IP4-7 **OPTIMIZATION OF FIR FILTER TO IMPROVE EYE DIAGRAM FOR GENERAL TRANSMISSION LINE SYSTEMS**
Y-S Cheng, Y-C Lai and R-B Wu, National Taiwan U, ROC

IP4-8 **ON SIGNALLING OVER THROUGH-SILICON VIA (TSV) INTERCONNECTS IN 3-D INTEGRATED CIRCUITS**
R Weerasekera, M Grange and D Pamunuwa, Lancaster U, UK
H Tenhunen, KTH, SE

IP4-9 **INTERCONNECT DELAY AND SLEW METRICS USING THE BETA DISTRIBUTION**
J-K Zeng, National Taiwan U, ROC

IP4-10 **ACCURATE TIMED RTOS MODEL FOR TRANSACTION LEVEL MODELING**
Y Hwangm and D D Gajski, UC Irvine, US
G Schirner, Northeastern U, US
S Abdi, Concordia U, CA

IP4-11 **A MODELING METHOD BY ELIMINATING EXECUTION TRACES FOR PERFORMANCE EVALUATION**
K Ono, R Kawahara and T Nakada, IBM Research – Tokyo, JP
M Toyota and Y Sakamoto, IBM Japan Ltd, JP
N Fukuoka, KYOCERA Mita Corp, JP

IP4-12 **VERIFYING UML/OCL MODELS USING BOOLEAN SATISFIABILITY**
M Soeken, R Wille, M Kuhlmann, M Gogolla and R Drechsler, Bremen U, DE

IP4-13 **SCOC3: AN EXAMPLE OF SUCCESSFUL DEVELOPMENT OF A HIGHLY INTEGRATED INNOVATIVE COMPUTER CORE FOR SPACE**
J-F Coldefy, EADS Astrium, DE

IP4-14 **HIGH TEMPERATURE POLYMER CAPACITORS FOR AEROSPACE APPLICATIONS**
C K Landrock and B Kaminska, Simon Fraser U, CA

IP4-15 **A NOVEL ON-CHIP CLOCK GENERATION SCHEME FOR FASTER-THAN-AT-SPEED DELAY TESTING**
S Pei, H Li and X Li, Chinese Academy of Sciences, PRC

IP4-16 **CONSTRUCTION OF DUAL MODE COMPONENTS FOR RECONFIGURATION AWARE HIGH-LEVEL SYNTHESIS**
G Economakos, S Xydis, I Koutras and D Soudris, National Technical U, GR

IP4-17 **OPTIMIZING DATA-FLOW GRAPHS WITH MIN/MAX, ADDING AND RELATIONAL OPERATIONS**
J Perez, P Sanchez and V Fernandez, Cantabria U, ES

IP4-18 **OPTIMIZATION OF THE BIAS CURRENT NETWORK FOR ACCURATE ON-CHIP THERMAL MONITORING**
J Long S Ogrenci Memik, Northwestern U, US

IP4-19 **SAT BASED MULTI-NET RIP-UP-AND-REROUTE FOR MANUFACTURING HOTSPOT REMOVAL**
F Yang, Y Cai and Q Zhou, Tsinghua University, PRC
J Hu, Texas A&M U, US

IP4-20 **NIM - A NOISE INDEX MODEL TO ESTIMATE DELAY DISCREPANCIES BETWEEN SILICON AND SIMULATION**
E Alpaslan and J Dworak, Brown U, US
A Majhi, B Kruseman, W Heuvelman and P Van De Wiel, NXP Semiconductors, NL

10.1.1 NANOELECTRONICS TUTORIAL – More than Moore

Room – Saal 5, Ground Floor 1100-1230

Organisers:
A M Ionescu, EPF Lausanne, CH
S Mitra, Stanford U, US

Moderator:
S Mitra, Stanford U, US

The More than Moore tutorials will deal with energy efficiency CNT-based devices and systems, the emergence of organic electronics and recent advances in NEMS-CMOS for wireless communications and sensing. Prof. Pop will focus on power dissipation in carbon nanotubes and graphene, with applications to low-energy devices, interconnects and memory elements. The second tutorial by Dr. Klauk will present thin-film transistors (TFTs) and integrated circuits based on conjugated organic semiconductors for applications that require electronic functionality with low or medium complexity distributed over large areas on unconventional substrates, such as flexible plastic. Finally, Prof. Weinstein will introduce a merged NEMS-CMOS device that can function as a building block to enhance the performance of RF circuits enabling narrow-bandwidth low noise amplifier design for transceivers and low phase-noise oscillator arrays for clock generation and temperature sensing in microprocessors.

1100 **CARBON NANOELECTRONICS: TOWARDS ENERGY-EFFICIENT COMPUTING**
E Pop, U of Illinois, Urbana-Champaign, US

1130 **ORGANIC ELECTRONICS: MATERIALS, MANUFACTURING AND APPLICATIONS**
H Klauk, Max Planck Institute, Stuttgart, DE

1200 **HYBRID NEMS-CMOS DEVICES FOR WIRELESS COMMUNICATION, SIGNAL PROCESSING AND SENSING**
D Weinstein, MIT, US

1230 **LUNCH BREAK**

10.2 PANEL SESSION – First Commandment: At Least Do Nothing Well

Room – Konferenz 6 1100-1230

Organiser:
M Casale-Rossi, Synopsys, US

Moderator:
G De Micheli, EPF Lausanne, CH

Panellists:
E Macii, Politecnico di Torino, IT
A Domic, Synopsys, US

P Perlo, Centro Ricerche FIAT, I
A Wild, ENIAC, BE
R Zafalon, STMicroelectronics, IT

In a recent keynote speech, UCB Prof. Randy Katz defined power as the 21st century's most limited, as well as most wasted resource: not only we seem to be unable to generate "greener" power but, at all levels, we seem to be really poor even in making an efficient use of our precious power.

We waste while doing things, as well as while doing nothing! "Electronics is sized for peak power consumption, and designed for continuous activity."

1230 **LUNCH BREAK**

10.3 Characterising and Optimising NoC Performance

Room – Konferenz 1 **1100-1230**

Moderators:
F Angiolini, iNoCs, IT
D Bertozzi, Ferrara U, IT

Papers in this session deal with the characterisation and optimisation of network-on-chip performance. For use at design time, an analytical performance model of the NoC, and the use of multiple switch implementations belonging to different technology libraries are presented. For use at run time, the injection of traffic at the NoC's edge, including the use of control loops, and the reduction of traffic inside the NoC are presented.

1100 **SIGNET: ON-CHIP NETWORK FILTERING FOR COARSE VECTOR DIRECTORIES**
N Enright Jerger, Toronto, CA

1130 **FEEDBACK CONTROL FOR PROVIDING QOS IN NOC BASED MULTICORES**
A Sharifi, H Zhao and M T Kandemir, The Pennsylvania State U, US

1200 **EXPLOITING MULTIPLE SWITCH LIBRARIES IN TOPOLOGY SYNTHESIS OF ON-CHIP INTERCONNECTION NETWORK**
M Jun, S Yoon and E-Y Chung, Yonsei U, KR

IPs **IP5-1, IP5-2 and IP5-3**

1230 **LUNCH BREAK**

10.4 Architectures for Next Generation Wireless Communication

Room – Konferenz 2 **1100-1230**

Moderators:
F Kienle, TU Kaiserslautern, DE
F Clermidy, CEA-LETI, FR

The first part of the session focuses on MIMO detection with a long presentation, followed by an additional short presentation.

The second part of the session addresses two distinct approaches to on chip communication architectures: NoC and bus based architectures. The session concludes with a presentation of a 150Mbit/s LTE turbo code decoder for an industrial application.

1100 **LOW-COMPLEXITY AND HIGH THROUGHPUT VLSI ARCHITECTURE OF SOFT-OUTPUT ML MIMO DETECTOR**
T Cupaiuolo and M Siti, STMicrolectronics, IT
A Tomasoni, Politecnico di Milano, IT

1130 **LOW COST MULTI-STANDARD NEAR-OPTIMAL SOFT-OUTPUT SPHERE DECODER:ALGORITHM AND ARCHITECTURE**
O Paker, ST Ericsson, NL
S Eckert and A Bury, Blue Wonder Communications GmbH, DE

1145 **LEVERAGING APPLICATION-LEVEL REQUIREMENTS IN THE DESIGN OF A NOC FOR A 4G SOC - A CASE STUDY**
I Walter, I Cidon and A Kolodny,
Technion - Israel Institute of Technology, IL
R Beraha, Qualcomm, US

1200 **DOMAIN SPECIFIC ARCHITECTURE FOR NEXT GENERATION WIRELESS COMMUNICATION**
B Zhang, H Liu, H Zhao, FM and T Chen,
National U of Defense Technology, PRC

1215 **A 150MBIT/S 3GPP LTE TURBO CODE DECODER**
M May, T Ilnseher and N Wehn, Kaiserslautern U, DE
W Raab, Infineon Technologies, DE

IP **IP5-4**

1230 **LUNCH BREAK**

10.5 Advances in Delay Fault Testing

Room – Konferenz 3 **1100-1230**

Moderators:
B Vermeulen, NXP Semiconductors, NL
S Hellebrand, Paderborn U, DE

Delay defects affect the speed of the fabricated devices. This session contains advances in testing for small-delay defects and critical paths, and broadside testing.

1100 **HIGH-QUALITY PATTERN SELECTION FOR SCREENING SMALL-DELAY DEFECTS CONSIDERING PROCESS VARIATIONS AND CROSSTALK**
K Peng and M Tehranipoor, Connecticut U, US
M Yilmaz, AMD, US
K Chakrabarty, Duke U, US

1130 **LAYOUT-AWARE PSEUDO-FUNCTIONAL TESTING FOR CRITICAL PATHS CONSIDERING POWER SUPPLY NOISE EFFECTS**
X Liu, Y Zhang, F Yuan and Q Xu,
The Chinese U of Hong Kong, PRC

1200 **ON RESET BASED FUNCTIONAL BROADSIDE TESTS**
I Pomeranz, Purdue U, US
S M Reddy, Iowa U, US

IPs **IP5-5 and IP5-6**

1230 **LUNCH BREAK**

10.6 Optimisation of Fault Tolerant and Time Constrained Embedded and Cyber-Physical Systems

Room – Konferenz 4 1100-1230

Moderators:
P Eles, Linkoping U, SE
J Chen, ETH Zurich, CH

This session addresses key issues in the context of energy efficient fault tolerant systems and systems implemented as wireless sensor networks. The first paper presents a new approach for minimising the energy consumption of frame-based real-time systems under fault tolerance constraints. The following two papers deal with various aspects of wireless sensor networks. The first of these two addresses the issue of collecting diagnostic data in a wireless distributed embedded system, while the second one presents an approach to data aggregation for cyber-physical systems with time, precision, and resource constraints. The last paper of the session proposes a soft error- aware design optimisation technique considering both energy efficiency and reliability improvement.

1100 **SCHEDULING FOR ENERGY EFFICIENCY AND FAULT TOLERANCE IN HARD REAL-TIME SYSTEMS**
Y Liu and K Wu, U of Illinois at Chicago, US
H Liang, Trident Microsystem Inc, US

1130 **SCOPED IDENTIFIERS FOR EFFECINT BIT ALIGNED LOGGING**
R Shea and M Srivastava, UCLA, US
Y Cho, Southern California U, US

1200 **LINEAR PROGRAMMING APPROACH FOR PERFORMANCE-DRIVEN DATA AGGREGATION IN NETWORKS OF EMBEDDED SENSORS**
C Ferent, V Subramanian and A Doboli,
State U of New York at Stony Brook, US

1215 **SOFT ERROR-AWARE DESIGN OPTIMIZATION OF LOW POWER AND TIME-CONSTRAINED EMBEDDED SYSTEMS**
R A Shafik and B M Al-Hashimi, Southampton U, UK
K Chakrabarty, Durham U, US

IPs **IP5-7, IP5-8 and IP5-9**

1230 **LUNCH BREAK**

10.7 Advanced Clocking Strategies

Room – Konferenz 5 1100-1230

Moderators:
L Carloni, Columbia U, US
S Nowick, Columbia U, US

The papers in this session address several key challenges in the clocking of synchronous systems. The first two address skew minimisation, where the former develops a suite of physical optimisations for clock network synthesis while the latter targets multiple power modes.

The final paper deals with non-determinism in multi-clock systems and provides a general method to ensure deterministic clock-domain crossing.

1100 **CONTANGO: INTEGRATED OPTIMIZATION OF SOC CLOCK NETWORKS**
D J Lee and I L Markov, U of Michigan, US

1130 **CLOCK SKEW OPTIMIZATION CONSIDERING COMPILICATED POWER MODES**
C-L Lung, Z-Y Zeng, C-H Chou and S-C Chang, NTHU, ROC

1200 **A GENERAL METHOD TO MAKE MULTI-CLOCK SYSTEM DETERMINISTIC**
M Su, Y Chen and X Gao, Chinese Academy of Sciences, PRC

IP **IP5-10**

1230 **LUNCH BREAK**

10.8 PANEL SESSION – Embedded Software Testing: What Kind of Problem is This?

Room – Exhibition Theatre, Ground Floor **1100-1230**

Organiser:
E Cota, UFRGS, BR

Moderator:
C Rowen, Tensilica, US

Panellists:
A Nohi, CoWare, DE
B Douglass, IBM, US
F Schaefer, Research & Consulting, DE
H de Groot, IMEC, NL
F Fummi, Verona U, IT

There is a growing number of academic and industrial works on the topic of embedded SW testing, and this seems to be a good time for reflection: how exactly is embedded software testing different from traditional software testing? Is it an engineering or computer science problem? Does it need extra support from platform developers? What is the role of the SW engineer and of the designer in developing a high-quality software-based embedded application? The panellists will present their view on the challenges for the test of embedded software. Specifically, the panellists are invited to answer/discuss the following questions:

1. How exactly embedded SW testing differs from traditional SW testing? Which are the target points for testing in an embedded SW? Are current software testing techniques and tools sufficient?

2. Can the SW testing help the system test? Can the HW help the SW testing? How can HW and SW integration be tested?

1530 **BREAK/IP5**

10.1.2 LUNCH TIME KEYNOTE

Room – Saal 5, Ground Floor 1330-1400

Organisers:
A M Ionescu, EPF Lausanne, CH
S Mitra, Stanford U, US

Moderator:
A M Ionescu, EPF Lausanne, CH

Keynote Speaker:
Dimitris Antoniadis, MIT, US

NANOELECTRONICS CHALLENGES FOR THE 21ST CENTURY

Abstract: Leading edge CMOS technologies today are unique examples of nanoscale engineering at an industrial scale. As we celebrate this remarkable achievement of our industry that forms the ever-expanding technology basis of modern society we cannot help but ponder the question of how we can continue to push the envelope of nano-electronics. With the end of Si FET scaling appearing increasingly near, searching for more scalable transistor structures in Si and in "beyond-Si" solutions has become imperative; from relatively "easy" transitions to non-planar Si structures, to the incorporation of high mobility semiconductors, like Ge and III-V's, to even higher mobility new materials such as carbon nanotubes, graphene, or other molecular structures. And even further, there are searches for new information representation and processing concepts beyond charge in FETs, as for example, in spin-state devices. Of course, declaring silicon dead is premature at best, and with this in mind I will discuss the challenges and possible scenaria for the introduction of novel nano-electronic devices.

1400 **END OF SESSION**

11.1 NANOELECTRONICS HOT TOPIC – Life with and after CMOS

Room – Saal 5, Ground Floor 1400-1530

Organisers/Moderators:
A M Ionescu, EPF Lausanne, CH
S Mitra, Stanford U, US

This session includes some very hot topics in nanoelectronics such as the future evolution and extension of CMOS (More Moore and Beyond CMOS) by addressing the power constraints at technology and device levels with a clear system vision (Dr H Riel), the 3D heterogeneous integration for More than Moore applications (Dr A Klumpp) and some far looking projections dealing with the limits of computation where a role is foreseen for non-charge based nanoelectronics (Dr G Bourianoff). The selected topics, discussions and examples are of high relevance for both industrial and academic communities.

1400 **DEVICE AND TECHNOLOGY CHALLENGES FOR POWER-CONSTRAINED CMOS SCALING**
H Ries, IBM Research, Zurich, CH

1430 **3D HETEROGENEOUS INTEGRATION FOR MORE THAN MOORE**
A Klumpp, Fraunhofer IZM Munich, DE

1500 **LIMITS OF COMPUTATION: NON-CHARGE BASED NANOELECTRONICS**
G Bourianoff, SRC, US

1530 **BREAK/IP5**

11.2 HOT TOPIC – Cool MPSoC Programming

Room – Konferenz 6 **1400-1530**

Organiser:
R Leupers, RWTH Aachen U, DE

Moderator:
A Herkersdorf, TU Munich, DE

Speakers:
X Nie, Infineon Technologies, DE
M Weiss, Blue Wonder Communications, DE
L Thiele, ETH Zurich, CH
B Kienhuis, Compaan Design, NL
T Isshiki, Tokyo Institute of Technology, JP

The purpose of this session is to analyse the programming methodology requirements for heterogeneous MPSoC platforms and to outline new approaches. With emphasis on wireless applications, the session provides a blend of academia/industry presentations, including contributions from innovative startup companies in that domain. This way, it aims at consolidation of real life requirements and novel solutions, and stresses the need for intensified and cooperative research activities in MPSoC programming.

1530 **BREAK/IP5**

11.3 Industrially-Oriented Formal Verification

Room – Konferenz 1 **1400-1530**

Moderators:
M Wedler, Kaiserslautern U, DE
J Baumgartner, IBM Corporation, US

This track includes papers addressing state-of-the-art applications of formal verification technologies dealing with industrially-relevant problems. The first proposes several novel techniques to dramatically increase the scalability of initialisation logic validation. The second proposes enhancements to the process of behavioural synthesis verification. The third proposes mechanisms to validate and automate the derivation of module paths used for timing analysis of Verilog cell libraries. The fourth proposes a new scalable framework for the analysis of compositional linear hybrid systems.

1400 **FINDING RESET NONDETERMINISM IN RTL DESIGNS - SCALABLE X-ANALYSIS METHODOLOGY AND CASE STUDY**
H-Z Chou and S-Y Kuo, National Taiwan U, ROC
H Yu and D Dobbyn, Teradyne Inc, US
K-H Chang, Avery Design Systems Inc, US

1430 **OPTIMIZING EQUIVALENCE CHECKING FOR BEHAVIORAL SYNTHESIS**
K Hao and F Xie, Portland State U, US
S Ray, U of Texas at Austin, US
J Yang, Intel Corporation, US

1500 **CHECKING AND DERIVING MODULE PATHS IN VERILOG CELL LIBRARY DESCRIPTIONS**
M Raffelsieper and M R Mousavi, TU Eindhoven, NL
C Strolenberg, Fenix Design Automation, NL

1515 **BACH 2 : BOUNDED REACHABILITY CHECKER FOR COMPOSITIONAL LINEAR HYBRID SYSTEMS**
L Bu, Y Li, X Chen, L Wang and X Li, Nanjing U, PRC

1530 **BREAK/IP5**

11.4 Sensor Networks and Applications

Room – Konferenz 2 **1400-1530**

Moderators:
J Lukkien, TU Eindhoven,NL
A Bouffioux, NXP Semiconductors, NL

This session presents papers about applications of sensors and sensor networks, as well as some technologies and architectural concepts for building these applications. Some aspects of software and of different sensor algorithms are also discussed.

1400 **DVFS BASED TASK SCHEDULING IN A HARVESTING WSN FOR STRUCTURAL HEALTH MONITORING**
A Ravinagarajan, D Dondi and T Simunic Rosing, UC San Diego, US

1415 **POWER-ACCURACY TRADEOFFS IN HUMAN ACTIVITY TRANSITION DETECTION**
J Boyd, H Sundaram and A Shrivastava, Arizona State U, US

1430 **NON-INVASIVE BLOOD OXYGEN SATURATION MONITORING FOR NEONATES USING REFLECTANCE PULSE OXIMETER**
W Chen, I Ayoola, S Bambang Oetomo and L Feijs, TU Eindhoven, NL

1445 **AN ACTIVE VISION SYSTEM FOR FALL DETECTION AND POSTURE RECOGNITION IN ELDERLY HEALTHCARE**
G Diraco, A Leone and P Siciliano, CNR-IMM, IT

1500 **A SMART SPACE BASED APPLICATION FOR DYNAMICALLY RELATING MEDICAL AND ENVIRONMENTAL CONDITIONS**
F Vergari, F Spadini, A D'Elia, G Zamagni, S Bartolini, L Roffia and T S Cinotti, ARCES – Bologna U, IT

1515 **AN ARCHITECTURE FOR SELF-ORGANIZATION IN PERVASIVE SYSTEMS**
J Lukkien, TU Eindhoven, NL
R Frunza, TOPIC Embedded Systems, NL

IP **IP5-11**

1530 **BREAK/IP5**

11.5 Fault Tolerance

Room – Konferenz 3 1400-1530

Moderators:
G Dinatale, LIRMM, FR
J Abella, Barcelona Supercomputing Center (BSC), ES

This session explores fault tolerance techniques spanning different abstraction levels.

1400 **TIMBER: TIME BORROWING AND ERROR RELAYING FOR ONLINE TIMING ERROR RESILIENCE**
M Choudhury and K Mohanram, Rice U, US
V Chandra and R Aitken, ARM, US

1430 **ERSA: ERROR RESILIENT SYSTEM ARCHITECTURE FOR PROBABILISTIC APPLICATIONS**
L Leem, H Cho, J Bau and S Mitra, Stanford U, US
Q A Jacobson, Nokia Research Center, US

1445 **PERFORMANCE-ASYMMETRY-AWARE TOPOLOGY VIRTUALIZATION FOR DEFECT-TOLERANT NoC-BASED MANY-CORE PROCESSORS**
Y Yu and S Ren, Illinois Institute of Technology, US
L Zhang, J Dong, Y Han and X Li, Chinese Academy of Sciences, PRC

1515 **MULTIPLEXED REDUNDANT EXECUTION: A TECHNIQUE FOR EFFICIENT FAULT TOLERANCE IN CHIP MULTIPROCESSORS**
P Subramanyan and V Singh,
Indian Institute of Science, Bangalore, IN
K K Saluja, U of Wisconsin-Madison, US
E Larsson, Linkoping U, SE

IP **IP5-12**

1530 **BREAK/IP5**

11.6 Synthesis and Optimisation of MPSoCs

Room – Konferenz 4 1400-1530

Moderators:
P Marwedel, TU Dortmund, DE
D Gajski, UC Irvine, US

This session consists of papers looking at novel techniques for MpSoC synthesis and optimisation by taking into account emerging goals such as robustness of designs, reliability and longevity.

The main challenges being addressed include combining these goals with traditional ones such those stemming from energy and cost.

1400 **ROBUST DESIGN OF EMBEDDED SYSTEMS**
M Lukasiewycz, M Glass and J Teich, Erlangen-Nuremberg U, DE

1430 **ENERGY-EFFICIENT TASK ALLOCATION AND SCHEDULING FOR MULTI-MODE MPSoCS UNDER LIFETIME RELIABILITY CONSTRAINT**
L Huang and Q Xu, The Chinese U of Hong Kong, PRC

1500 **PM-COSYN: PE AND MEMORY CO-SYNTHESIS FOR MPSoCS**
Y-J Chen, C-L Yang and P-H Wang, National Taiwan U, ROC

1515 **COST-EFFECTIVE SLACK ALLOCATION FOR LIFETIME IMPROVEMENT IN NOC-BASED MPSoCS**
B H Meyer, A S Hartman and D E Thomas, Carnegie Mellon U, US

IP **IP5-13**

1530 **BREAK/IP5**

11.7 Mixed-Technology and Analogue Design

Room – Konferenz 5 **1400-1530**

Moderators:
T Kazmierski, Southampton U, UK
J Haase, Fraunhofer Institute for Integrated Circuits, DE

The first paper in this session presents a novel architecture for harvesting energy in integrated systems, enabling autonomous operation without batteries. The second paper describes a method to include analogue wire models in a SystemC simulation at transaction level.

A creative, novel method for optimisation of analogue circuits is presented in the third talk. The method uses homotopy between initial equations and introduced structures. An efficient macro modelling technique is demonstrated as an interactive presentation.

1400 **EFFICIENT POWER CONVERSION FOR MICRO-SCALE ENERGY HARVESTING**
C Lu, S P Park, V Raghunathan and K Roy, Purdue U, US

1430 **TRANSMITTING TLM TRANSACTIONS OVER ANALOGUE WIRE MODELS**
S Schulz, T Uhle, J Becker and K Einwich, Fraunhofer IIS-EAS, DE
S Sonntag, Infineon Technologies AG, DE

1500 **INTENT-LEVERAGED OPTIMIZATION OF ANALOG CIRCUITS VIA HOMOTOPY**
M Jeeradit, J Kim and M Horowitz, Stanford U, US
Carnegie Mellon U, US

IP **IP5-14**

1530 **BREAK/IP5**

11.8 PANEL SESSION – Reliability of Data Centers: Hardware vs. Software

Room – Exhibition Theatre, Ground Floor 1400-1530

Organiser/Moderator:
M Tahoori, Karlsruhe U, DE

Panellists:
D Alexandrescu, iRoc
K Granlund, EMC
A Silburt, Cisco
B Vinnakota, Intel

In today's life, data centers are integral part of daily life. From web search to online banking, online shopping to medical records, we rely on data centers for almost everything. Malfunctions in the operation of such data centers have become an inseparable part of our daily lives as well. Major malfunction causes include hardware and software failures, design errors, malicious attacks and incorrect human interactions. The consequences of such malfunctions are enormous: loss of human life, financial loss, fraud, wastage of time and energy, loss of productivity, and frustrations with computing. Therefore, reliability of these systems plays a critical role in all aspects of our day to day life.

1530 **BREAK/IP5**

IP5 Interactive Presentations

Room – Exhibition Area, Ground Floor

Each interactive presentation will run on a ten minute rotation (three presentations per session) and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP5-1 **OPTIMAL REGULATION OF TRAFFIC FLOWS IN NETWORKS-ON-CHIP**
F Jafari, Ferdowsi U of Mashhad, IR
and Royal Institute of Technology (KTH), SE
Z Lu and A Jantsch, Royal Institute of Technology (KTH), SE
M H Yaghmayee, Ferdowsi University of Mashhad, IR

IP5-2 **A METHOD TO REMOVE DEADLOCKS IN NETWORKS-ON-CHIPS WITH WORMHOLE FLOW**
C Seiculescu and G De Micheli, EPF Lausanne, CH
S Murali, INoCs and EPF Lausanne, CH
L Benini, Bologna U, IT

IP5-3 **AN ANALYTICAL METHOD FOR EVALUATING NETWORK-ON-CHIP PERFORMANCE**
S Foroutan, CEA-LETI and STMicroelectronics, FR
Y Thonnart and A Jerraya, CEA-LETI, FR
R Hersemeule, STMicroelectronics, FR

IP5-4 **A LOW AREA RECONFIGURABLE MIMO DETECTOR BASED ON K-BEST SPHERE DECODER**
N Moezzi-Madani, T Thorolfsson and W R Davis, North Carolina State U, US

IP5-5 **AN EMBEDDED WIDE-RANGE AND HIGH-RESOLUTION JITTER MEASUREMENT CIRCUIT USING JITTER AMPLIFICATION**
Y Lee and C-Y Yang, National Chung Hsing U, Taiwan, ROC
N-C D Cheng and J-J Chen,
Industrial Technology Research Institute, Taiwan, ROC

IP5-6 **VERIFYING ANALOG CIRCUITS BASED ON A DIGITAL SIGNATURE**
A Gomez, R Sanahuja, L Balado and J Figueras,
UP Catalunya, ES

IP5-7 **DAGS: DISTRIBUTION AGNOSTIC SEQUENTIAL MONTE CARLO SCHEME FOR TASK EXECUTION TIME**
N Iqbal and J Henkel, Karlsruhe U, DE

IP5-8 **TAMING THE COMPONENT TIMING: A CBD METHODOLOGY FOR REAL-TIME EMBEDDED SYSTEMS**
M G Dixit and S Ramesh, India Science Lab, GM R&D, IN
P Dasgupta, Indian Institute of Technology, Kharagpur, IN

IP5-9 **DETERMINISTIC, PREDICTABLE AND LIGHT-WEIGHT MULTITHREADING USING PRET-C**
S Andalam and P S Roop, Auckland U, NZ
A Girault, INRIA, Rhone-Alpes, FR

IP5-10 **INVERSED TEMPERATURE DEPENDENCE AWARE CLOCK SKEW SCHEDULING FOR SEQUENTIAL CIRCUITS**
J Long and S Ogrenci Memik, Northwestern U, US

IP5-11 **DYNAHEAL: DYNAMIC ENERGY EFFICIENT TASK ASSIGNMENT FOR WIRELESS HEALTHCARE SYSTEMS**
P Aghera, D Fang, A Coskun and T Rosing,
UC San Diego, US
D Krishnaswamy, Qualcomm Inc, US

IP5-12 **INSTRUCTION PRECOMPUTATION WITH MEMOIZATION FOR FAULT DETECTION**
D Borodin and B H H Juurlink, TU Delft, NL

IP5-13 **SIMULTANEOUS BUDGET AND BUFFER SIZE COMPUTATION FOR THROUGHPUT-CONSTRAINED TASK**
M H Wiggers and M C W Geilen, TU Eindhoven, NL
M J G Bekooij and T Basten,
NXP Semiconductors and Twente U, NL
T Basten, TU Eindhoven, and Embedded Systems Institute, Eindhoven, NL

IP5-14 **AN EFFICIENT TRANSISTOR-LEVEL PIECEWISE-LINEAR MACROMODELING APPROACH FOR MODEL ORDER REDUCTION OF NONLINEAR CIRCUITS**
X Pan, F Yang, X Zeng and Y Su, Fudan U, PRC

12.1 NANOELECTRONICS PANEL – Great Challenges in Nanoelectronics and Impact on Academic research: More than Moore or Beyond CMOS?

Room – Saal 5, Ground Floor 1600-1730

Organisers:
A M Ionescu, EPF Lausanne, CH
S Mitra, Stanford U, US

Moderator:
R De Keersmaeker, IMEC, BE

VLSI Nano-Electro-Mechanical Systems
M Roukes, Caltech, US

Panellists:
D Antoinadis, MIT, US
H De Man, KU Leuven and IMEC, BE
G Bourianoff, SRC and Intel, US
M Brillouet, CEA-LETI, FR
L Samuelson, Lund U, SE

This panel session will address the post-CMOS research great challenges and opportunities corresponding to the More Than Moore and Beyond CMOS domains. The opening talk of the panel will set the ground for discussion with some key examples placed at the intersection of these two domains. Especially the role of functional diversification and of new research and application drivers, different from scaling, will be critically discussed by a team of high level experts in the field. Moreover, the impact of post-CMOS era on the way the academic research and the education of engineers are conceived today and should be adapted in the future will be in the center of the debate.

1730 **CLOSE**

12.2 HOT TOPIC – 3D Stacked ICs: Technology, Design and Test

Room – Konferenz 6 1600-1730

Organisers:
P Girard, LIRMM, FR
E J Marinissen, IMEC, BE

Moderators:
Y Zorian, Virage Logic, US

3D integration is a key solution to the predicted performance increase of future electronic systems. It offers extreme miniaturisation and fabrication of More than Moore products. The session surveys basic knowledge and discusses challenges in the field of three dimensional stacked ICs (3D-SICs) based on Through-Silicon Vias (TSVs). The first presentation deals with 3D integration concepts at the technological level.

The second presentation explores application drivers, design, and CAD for 3D ICs. The last presentation focuses on the available solutions and still open challenges for testing 3D-SICs.

1600 **3D-INTEGRATION OF SILICON DEVICES: A KEY TECHNOLOGY FOR SOPHISTICATED PRODUCTS**
A Klumpp, P Ramm and R Wieland, Fraunhofer Institute for Reliability and Microintegration (IZM), DE

1630 **CREATING 3-D SPECIFIC SYSTEMS – ARCHITECTURE, DESIGN AND CAD**
P Franzon, North Carolina State U, US

1700 **TESTING TSV-BASED THREE-DIMENSIONAL STACKED ICS**
E J Marinissen, IMEC, BE

1730 **CLOSE**

12.3 Formal Methods: Advances in Core Technology

Room – Konferenz 1 **1600-1730**

Moderators:
J Marques-Silva, U College Dublin, IE
G Cabodi, Politecnico di Torino, IT

Despite advances in the strength of and application prevalence of formal methods, capacity limitations continue to be a a significant challenge to their reliability. This track presents papers to boost the capacity of core formal reasoning algorithms. The first proposes a preprocessing technique which leverages "dominators" in a circuit description to improve the scalability of the solution of Quantified Boolean Formulae. The second extends prior work in the verification of Network on Chip systems to cover flaws related to deadlocks and lost messages. The third presents several techniques to advances existing theory in the integration of BDDs with Satisfiability Modulo Theory techniques for substantial performance improvements.

1600 **LEVERAGING DOMINATORS FOR PREPROCESSING QBF**
H Mangassarian, B Le, A Goultiaeva, F Bacchus and A Veneris, Toronto U, CA

1630 **FORMAL SPECIFICATION OF NETWORKS-ON-CHIPS: DEADLOCK AND EVACUATION**
F Verbeek And J Schmaltz Radboud, Nijmegen U, NL

1700 **TIGHTER INTEGRATION OF BDD AND SMT FOR PREDICATE ABSTRACTION**
A Cimatti, A Franzen, K Kalyanasundaram and M Roveri, Fondazione Bruno Kessler, IT
A Griggio, Trento U, IT

1730 **CLOSE**

12.4 Video Encoding and Image Processing Techniques

Room – Konferenz 2 **1600-1730**

Moderators:
C Bouganis, Imperial College, UK
S Saponara, Pisa U, IT

The works presented in this session address challenging issues on video coding and image processing applications. More precisely, this session offers the following: recent advances on high performance and energy efficient H.264 encoding, an FPGA-based design for noise removal, a real- time 3D reconstruction platform, an area and power efficient JPEG approach, and a task execution time predictor for a H.264 multicore platform.

1600 **AN HVS-BASED ADAPTIVE COMPUTATIONAL COMPLEXITY REDUCTION SCHEME FOR H.264/AVC VIDEO ENCODER USING PROGNOSTIC EARLY MODE EXCLUSION**
M Shafique, B Molkenthin and J Henkel, Karlsruhe U, DE

1615 **SCHEDULING AND ENERGY-DISTORTION TRADEOFFS WITH ORIP**
D Anastasia and Y Andreopoulos, U College London, UK

1630 **ENBUDGET: A RUN-TIME ADAPTIVE PREDICTIVE ENERGY-BUDGETING SCHEME FOR ENERGY-AWARE MOTION ESTIMATION IN H.264/MPEG-4 AVC VIDEO ENCODER**
M Shafique, L Bauer and J Henkel, Karlsruhe, DE

1645 **A METHOD FOR DESIGN OF IMPULSE BURSTS NOISE FILTERS OPTIMIZED FOR FPGA IMPLEMENTATIONS**
Z Vasicek, L Sekanina and M Bidlo, TU Brno, CZ

1700 **EXPLORATION OF HARDWARE SHARING FOR IMAGE ENCODERS**
S Lopez and R Sarmiento, Las Palmas de Gran Canaria U, ES
P G Potter, W Luk and P Y K Cheung, Imperial College, London, UK

1715 **TOWARDS HARDWARE STEREOSCOPIC 3D RECONSTRUCTION: A REAL-TIME FPGA COMPUTATION OF THE DISPARITY MAP**
S Hadjitheophanous, C Ttofis, A S Georghiades and T Theocharides, Kios Research Center for Intelligent Systems and Networks, GR

1730 **CLOSE**

12.5 Testing and Diagnosis of Analogue and Mixed-Signal Circuits

Room – Konferenz 3 **1600-1730**

Moderators:
S Sattler, Erlangen U, DE
S Mir, TIMA Laboratory, FR

The papers in this session deal with ADC BIST, test generation for equalisers in high-speed serial links, and fault diagnosis techniques for analogue and mixed-signal circuits.

1600 **A ROBUST ADC CODE HIT COUNTING TECHNIQUE**
J-L Huang, M-H Lu and X-L Huang, National Taiwan University, ROC
K-Y Chou, National Taipei U, ROC

1630 **AN AUTOMATIC TEST GENERATION FRAMEWORK FOR DIGITALLY-ASSISTED ADAPTIVE EQUALIZERS IN HIGH-SPEED SERIAL LINKS**
M Abbas, S Komatsu and K Asada, Tokyo U, JP
K-T Cheng, UC Santa Barbara, US
Y Furukawa, Advantest Corporation, JP

1645 **FAULT DIAGNOSIS OF ANALOG CIRCUITS BASED ON MACHINE LEARNING**
K Huang, H-G Stratigopoulos and S Mir, TIMA Laboratory, FR

1715 **BLOCK-LEVEL BAYESIAN DIAGNOSIS OF ANALOGUE ELECTRONIC CIRCUITS**
S Krishnan, TNO, Zeist, NL
K D Doornbos and R Brand, NXP Semiconductors, NL
H G Kerkhoff, Twente U, NL

1730 **CLOSE**

12.6 Timing Aspects in System Synthesis

Room – Konferenz 4 1600-1730

Moderators:
J Cong, UCLA, US
T Stefanov, Leiden U, NL

This session consists of three papers investigating various timing issues - starting from latency insensitive designs to multi-rate DSP algorithms - in high-level synthesis.

1600 **CONTROL NETWORK GENERATOR FOR LATENCY INSENSITIVE DESIGNS**
E Kilada and K S Stevens, Utah U, US

1630 **USING SPECULATIVE FUNCTIONAL UNITS IN HIGH LEVEL SYNTHESIS**
A A Del Barrio, M C Molina, J M Mendias and R Hermida, Madrid Complutense U, ES
S Ogrenci Memik, Northwestern U, US

1700 **RETIMING MULTI-RATE DSP ALGORITHMS TO MEET REAL-TIME REQUIREMENT**
X-Y Zhu, Chinese Academy of Sciences, PRC

1730 **CLOSE**

12.7 Reliability and Power Optimisations for FPGAs

Room – Konferenz 5 1600-1730

Moderators:
J Becker, Karlsruhe U, DE
K Bertels, TU Delft, NL

This session focuses on power aware and reliability aware design tools and architectures for FPGA devices.

1600 **COMBINING OPTIMIZATIONS TO AUTOMATE LOW POWER DESIGN**
Q Liu, T Todman, J G De F Coutinho, W Luk and G Constantinides, Imperial College, UK

1630 **A NEW QUATERNARY FPGA BASED ON VOLTAGE-MODE MULTI-VALUED CIRCUITS**
C Lazzari, INESC-ID, PT
P Flores and J Monteiro, INESC-ID / IST, TU Lisbon, PT
L Carro, UFRGS, BR

1700 **AN EVALUATION OF A SLICE FAULT AWARE TOOL CHAIN**
A Gupte and P Jones, Iowa State U, US

1715 **RELIABILITY- AND PROCESS VARIATION-AWARE PLACEMENT FOR FPGAS**
A Bsoul and N Manjikian, Queen's U, CA
L Shang, U of Colorado, Boulder, US

1730 **CLOSE**

friday workshops

Co-Chairs:
Nicola Nicolici, McMaster U, Hamilton, CA
Peter Y K Cheung, Imperial College London, UK

The DATE Friday Workshops initiative was first introduced in 2003 and, since then, the workshops topics and participation have increased to over 250 researchers and designers attending eight workshops at DATE 09.
This initiative has now become an integral part of the conference, offering workshops on current and emerging important issues in design, test, EDA and software to complement the regular conference programme running throughout the week. They provide an unique opportunity for the various research and design communities to spend a day discussing the latest and the best, sharing their experiences and visions.

This year's programme includes six workshop themes. Three workshops are related to architecture and technology, ranging from multi/many-core parallel platforms, 3D integration and silicon debugging. Two other workshops themes examine the fruits of large publicly funded consortia research into reconfigurable computing and process variability. The intention is that lessons learned would help in promoting new research consortia for future proposals. The final workshop is concerned with model-based engineering methods applied to embedded systems design.

Friday Workshop attendees should choose in advance one of W1, W2, W3, W4, W5 or W6. The Friday Workshops run from 0830 in the morning until 1700 in the afternoon. The individual timetables for each Friday Workshop vary and are as listed below. For the detailed version of the programme, visit - www.date-conference.com

W1 The European Landscape of Reconfigurable Computing: Lessons Learned, New Perspectives and Innovations

Room – Konferenz 1

Organisers:
Michael Huebner and Juergen Becker,
Karlsruhe Institute of Technology (KIT), DE
Jean-Marc Philippe and Christian Gamrat, CEA LIST, FR
Philippe Bonnot, Thales, FR

Description: Several projects like e.g. 4S, MORPHEUS, AETHER, ANDRES and HARTES funded by the European Commission, developed complex heterogeneous and reconfigurable SoC architectures. Furthermore, the EC-funded HiPEAC Network of Excellence includes a research cluster on reconfigurable computing. The run-time optimal functional execution was a strong motivation for heterogeneous architectures and the possibility of dynamic and partial hardware reconfiguration enables a higher degree of flexibility and run-time adaptivity.

The hardware architectures of such systems must be optimised for allowing a self-adaptive behavior of the system with a high degree of flexibility while still allowing a simplified programmability. The architecture must be designed to be emergent (with redundant components) and dynamically self-optimised in terms of power consumption, performance resource utilisation etc.

In many cases the complete architecture includes reconfigurable analogue tiles, reconfigurable digital processing accelerators and run-time adaptive controllers. Of course, the memory architecture in such a system will become a critical point and innovative memory constellations for reconfigurable systems are also investigated within the research programs. Since reconfigurable systems require storing functional descriptions for dynamic configuration, minimising the time to fetch and configure a function dynamically will be important for the system real-time response.

Another important consideration is the programmability of such heterogeneous architectures. The application developer should be able to model the applications on a high level without a detailed knowledge about the underlying hardware/software architecture. The tools and possibilities for run-time adaptation should then enable the most optimal run-time system configuration. This was a major focus in the European projects called 4S, MORPHEUS, AETHER, HARTES and ANDRES. The highlights of the results will be presented and discussed also in relation to the challenges within the novel EU projects presented in the workshop.

This Friday workshop aims to bring together the representatives of the EU projects which recently finished, and the ones who represent projects which were recently accepted like e.g. REFLECT, ERA and CRISP, in order to discuss the final results and experiences which were achieved and how this can be exploited in novel projects. Furthermore, this workshop is an outstanding source of importance for the leader and participants of the next generation EU projects in this domain. The goal is to exchange experience on technical and administrative level and to establish and extend the network between researchers.

0830 **SESSION 1 - Invited Talks**

Welcome and Introduction by the Organisers

Panagiotis Tsarchopoulos, Project Officer
"European Research Prospects for Reconfigurable Computing Systems"

Discussion on "Future of reconfigurable computing in EU Projects: Expectations and reality"

Juergen Teich, Erlangen U, DE
"German Research Foundation's Priority Program on Reconfigurable Computing Systems – Achievements and Lessons Learned"

1030 **BREAK**

1045 **SESSION 2 – RECENT EU PROJECTS: RECONFIGURABLE MULTICORE ARCHITECTURES**

Project MORPHEUS
Philippe Bonnot, Thales, FR
"Exploitation of reconfiguration for increased run-time flexibility and self-adaptive capabilities in future SoCs"

Project HARTES
Koen Bertels, TU Delft, NL
"hArtes: an holistic Approach to heterogeneous, reconfigurable real time embedded systems"

Project 4s
Eberhard Schueler, PACT, DE,
Juergen Becker, U of Karlsruhe (TH), DE
"The 4S heterogeneous multi-tiled reconfigurable hardware and dynamic task allocation for data-flow oriented applications"

1200 **LUNCH BREAK**

1300 **SESSION 3 – RECENT EU PROJECTS : DESIGN AND PROGRAMMING OF RECONFIGURABLE COMPUTING SYSTEMS**

Project AETHER
Christian Gamrat, CEA LIST, FR
"Self-Adaptive Networked Entities: Autonomous computing elements for future pervasive applications and technologies"

Project ANDRES
Kim Gruettner, Frank Oppenheimer, DE
"Analysis and Design of run-time Reconfigurable, heterogeneous Systems"

Poster and Discussion Session
(extended to break)
(Posters will be announced in the workshop)

1430 **BREAK & POSTER SESSION**

1500 **SESSION 4 – RECENT EU FUNDED PROJECTS: PERSPECTIVES AND INNOVATIONS**

Project REFLECT
Joao Cardoso, Universidade do Porto/FEUP, PT
Pedro Diniz, Insituto Superior Ténico / INESC-ID, PT
"Rendering FPGAs to Multi-Core Embedded Computing"

Project CRISP
Paul Heysters, Recoresystems, NL
"Cutting Edge Reconfigurable ICs for Stream Processing"

Project ERA
Stephan Wong, Georgi Gaydadjiev, TU Delft, NL
"Embedded Reconfigurable Architectures"

HiPEAC vision/roadmap
"Results of the reconfigurable cluster discussions in the past two years"

1630 **PANEL DISCUSSION – THE EUROPEAN LANDSCAPE OF RECONFIGURABLE COMPUTING**

1700 **Conclusions and Close**

W2 The Fruits of Variability Research in Europe

Room – Konferenz 2

Organisers:
Scott Roy, Glasgow U, UK
Mark Zwolinski, Southampton U, UK

Description: It is impossible to realise billions of devices which are completely identical at the atomic scale. Fluctuations induced by process tolerances and material granularity are now a major industrial issue. Important questions associated with such variability are: What are the major causes of fluctuations at device level? How do fluctuations affect the functionality, operating frequency and reliability of devices, circuits and systems? What countermeasures are possible and which are best taken at each level?

This workshop is prompted by the confluence of a recent upsurge in academic interest in the area and because of the presence of a number of EU and UK consortia presently producing results:

- UK EPSRC Meeting the design challenges of nano-CMOS electronics
- EU FP7 Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
- EU ENIAC MOdeling and DEsign of Reliable, process variation-aware nanoelectronic devices, circuits and systems

The Workshop will cover recent significant results from these EU projects and point to future research directions. A keynote from a recognised Japanese expert will pave the way for sessions on: the measurement, simulation and modelling of device variability in today's and end-of-roadmap devices; progress in simulation tools to analyse the effects of device variability on circuit and systems level manufacturability, design, reliability and circuit performance; techniques for creating variability-resilient solutions in circuit and systems design. A concluding think tank will discuss future research and knowledge transfer to industry.

A Poster session will give attendees a focal point for sharing new developments in the field. Poster abstracts should be e-mailed to <S.Roy@elec.gla.ac.uk> or <mz@ecs.soton.ac.uk> and accept/reject decisions on posters will be made within a week of submission. Final deadline for submission of poster abstracts is 11th February 2010.

0845 **SESSION 1 - PERSPECTIVE**

0845 **Welcome and Introduction by the Organisers**

0900 **Keynote:**
Toshiro Hiramoto, Tokyo U, JP
Variability research: accomplishments and future directions – a Japanese perspective

1000 Asen Asenov, Glasgow U, UK
Device variability and reliability: towards the end of the roadmap

1030 **BREAK & POSTER SESSION**

1100 **SESSION 2 – SIMULATION STRATEGIES & TOOLS**

1100 Scott Roy, Glasgow U, UK
Statistical compact model strategies: efficiently bridging the gap between devices and circuits

1130 Miguel Miranda, IMEC, BE
Hierarchical, variability aware circuit and system simulation

1200 **LUNCH BREAK**

1300 **SESSION 3 - SOLUTIONS**

1300 Andy Tyrrell, York U, UK
Evolutionary algorithms as an aid to synthesis in the presence of variability.

1330 Georges Gielen, KU Leuven, BE
Variability and degradation resilient analogue and digital circuit design: techniques and solutions

1400 Luca Benini, DEIS - Bologna U, IT
System-level variability countermeasures in many-core computing - a vertically integrated view

1430 **BREAK & POSTER SESSION**

1500 **SESSION 4 – THE FUTURE**

1500 Steve Furber, Manchester U, UK
SpiNNaker: a large scale SoC design as a test vehicle for variability modelling

1530 Enrico Macii, Politecnico di Torino, IT
MODERN, a European flagship project in variability and it's impact on design – overview and goals

1600 **PANEL DISCUSSION - VARIABILITY RESEARCH: OUR PLACE IN THE WORLD? WHERE NEXT?**

1700 **Conclusions and Close**

W3

Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications

Room – Konferenz 3

Organisers:
Cristina Silvano, Giovanni Agosta, Politecnico di Milano, IT
Juergen Becker, Michael Huebner,
Karlsruhe Institute of Technology, DE
Chantal Ykman-Couvreur, IMEC, BE
Diana Goehringer, Fraunhofer IOSB, DE

Description: The future of embedded computing is shifting to multi-core designs to boost performance due to the unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence embedded system designers are increasingly faced with the following new big challenges: the support for a variety of concurrent applications, and the platform heterogeneity.
These challenges lead to the following significant issues:

- How can we write applications that can exploit the underlying (parallel) architecture, without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the process should be automated?
- How should we design the underlying architectures?

These and other questions will be central to this workshop, which will bring together researchers actively working on architectures, design tools, and applications for embedded parallel computing platforms.

This workshop will have three main sessions:

- Architectures: presenting and discussing the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- Design tools: focusing on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- Applications: discussing the analysis, development, modification and integration of applications with respect to parallel computing platforms.

0830 **OPENING**

0830 **Welcome and Introduction by the Organisers**

0845 **Introduction to Poster Sessions**

0900 **SESSION 1 - ARCHITECTURES**

0900 Trevor Mudge, U of Michigan, US
"Near threshold computing: A new paradigm for low power"

0930 Alex Orailoglu, UC San Diego, US
"Application Specific Architectures"

1000 Koen Bertels, TU Delft, NL
"An integrated design flow for HW/SW co-design for reconfigurable, heterogeneous multi-core platforms: the hArtes view"

1030 **BREAK & POSTER SESSION**

1100 **SESSION 2 - DESIGN TOOLS**

1100 Roel Wuyts, IMEC, BE
"Adaptive Run-Time Resource Management to Map Dynamic Software on Heterogeneous Resources"

1130 William Fornaciari, Politecnico di Milano, IT
"Design Space Exploration for Run-time Resource Management: the MULTICUBE view"

1200 **LUNCH BREAK**

1300 **SESSION 2 – DESIGN TOOLS** (continued)

1300 Elio Guidetti, STMicroelectronics, IT
"Energy Management Complexity for Ultra Lo Power Multi-Processor System-on-Chip: an Industrial Perspective about System Architectures, Technology and Design Methodology"

1330 **SESSION 3 – APPLICATIONS**

1330 Alba Cristina de Melo, U. of Brasilia, BR
"Exploiting Parallel Computing Systems for Bioinformatic Algorithms"

1400 Thierry Collette, CEA LIST, FR
"MPSOC Architectures for Image and Video Processing"

1430 **BREAK & POSTER SESSION**

1500 **SESSION 3 – APPLICATIONS** (continued)

1500 Torsten Kempf, RWTH Aachen, DE
"The Nucleus concept - A Design Methodology for Efficient SDR Development"

1530 **PANEL DISCUSSION – Multicore Technologies in Research, Education and Innovation: A New Mainstream Activity?**

1630 **Conclusions and Close**

W4 SDD – Silicon Debug-and-Diagnosis

Room – Konferenz 4

Organisers:
Bart Vermeulen, NXP Semiconductors, NL
Christian Boit, Berlin U, DE
Al Crouch, ASSET, US

Description: Silicon Debug-and-Diagnosis is the understanding of the methods, techniques, silicon architectures and tools to discover why silicon fails. This topic includes understanding design modelling and implementation errors, silicon fabrication issues, process variability and defectivity, lifecycle failures, and electrical margin versus specification mismatches so that failures found at design, implementation, fabrication, and end use can more efficiently be driven to root cause. The continual march of Moore's Law and state-of-the art packaging technology is also providing more and more complex ways that silicon chips can fail, and requires more advances in debug and diagnosis technology to stay within time-and-budget efficiency windows.
The goal of this workshop is to bring together researchers, practitioners, and others interested in this ever-evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

The workshop program contains the following elements.

- One opening session with a keynote address
- Three technical sessions with a total of nine regular presentations
- Two embedded tutorials
- A panel session addressing the controversial topic "Formalized Debug-Diagnosis versus Ad Hoc Methods"

0830 **SESSION 1 - OPENING**

0830 **Welcome Address and Opening Remarks**

0840 **Past, Present, and Future of Debug"**
Magdy Abadir, Freescale, US

0915 **SESSION 2 - Post Silicon Validation**

Building a Bridge: From Pre-Silicon Verification to Post-Silicon Validation
Amir Nahir, Allon Adir, Charles Meissner, Gil Shurek – IBM Research, Haifa U, IL

0935 **Post-Silicon Debug of Complex Multi Clock and Power Domain SoCs**
Bradley R Quinton, Andrew M Hughes, Steven J E Wilton – British Columbia U, US

0955 **Guaranteeing Coverage in Post-silicon Validation**
Amir Nahir, Allon Adir, Avi Ziv, Charles Meissner, John Schumann – IBM Research, Haifa U, IL

1015 **EMBEDDED TUTORIAL 1**

JTAG-Based Data Collection
John Potter - ASSET, Texas, US

1030 **BREAK**

1100 **SESSION 3 - Test and Debug Algorithms**

Automated Silicon Debug Analysis Techniques for a Hardware Data Acquisition Environment
Yu-Shen Yang, Brian Kang, Andreas Veneris, Hratch Mangassarian – Toronto U, CA, Nicola Nicolici, McMaster U, Hamilton, CA

1120 **Efficient Methods for Debug of ATPG Scan Chain Failures on ATE**
Ernst Aderholz - Freescale Semiconductor, Munich, DE

1140 **A Cumulative Memory Failure Bitmap Display & Analysis SW Tool**
P Bernardi, A Panariti, M Sonza Reorda, T Kerekes, D Appello, M Barone – Politecnico di Torino, IT

1200 **LUNCH BREAK**

EMBEDDED TUTORIAL 2

1300 **Advances in ASIC Fault Isolation for Automotive Applications**
Antonino Barna, Andrea Bogliolo, Carlo Caimi, Alberto Pintus – STMicroelectronics, IT

1330 **SESSION 4 - Physical Root-Cause**

Physical Fault Isolation on Large Designs using a Hybrid Logical-to-Physical Cross Mapping Solution
Cathy Kardach, Hitesh Suri - DCG Systems Inc, Fremont, CA, US
Puneet Gupta, Tung Ton - NVIDIA Corp., Santa Clara, CA, US

1350 **Fault Localization on Scan Designs using Analog Simulation**
Christian Burmer, Andreas Altes, Markus Gruetzner, Thomas Schweinboeck - Infineon Technologies, Munich, DE

1410 **Local IC Speed Trimming, Nanoscale CE and Analysis Based upon a Coaxial Optical and Ion Beam Approach**
C Boit, R Schlangen, U Kerst, T Lundquist - Berlin U, DE

1430 **BREAK**

1500 **PANEL SESSION -**
"Formalized Debug-Diagnosis versus Ad Hoc Methods"

Description: The panel will wrestle with the question of "has the debug-diagnosis problem reached, or is it about to reach, a level of complexity that requires a formal industry-wide standard solution – or can it continue with each chip from each chip provider having none, some, or a different mix of DFT and DFD solutions?" If a standard solution is needed, what are the requirements and who drives those requirements? If each chip provider or core provider can support its own DFT and DFD solutions, how do these solve the "mixed-resource" problem that exists in complex SoCs and 3D chips? How can end users with No Trouble Found (NTF) and Cannot-Repeat (CNR) replicate problems if the resources are not easily operated concurrently? The panel members will each take a stance and will justify that stance against the issues and requirements of their own industry sector.

Moderator: **Al Crouch – ASSET, Texas, US**

Panellists: **Invited Panellists**
EDA Representative • SoC Representative • ATE Representative • Microprocessor Representative • 3D Stacked-Die Representative

1630 **Conclusion and close**

W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test

Room – Konferenz 6

Organiser:
Erik Jan Marinissen, IMEC, BE
Yann Guillou, ST-Ericsson, FR
Geert Van der Plas, IMEC, BE

Description: 3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. But in order to produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges. The first edition of this workshop took place in conjunction with DATE 2009 (see http://www.date-conference.com/conference/date09-workshop-W5).

The workshop program contains the following elements.

- Two invited keynote addresses
- Two sessions with in total six regular presentations
- Two poster sessions
- A panel session

For the detailed version of the program, please check http://www.date-conference.com/conference/date10-workshop-W5.

0830 **SESSION 1: OPENING**
Moderator: Peter Schneider - Fraunhofer Institute, DE

0830 **Welcome Address**

0850 **Keynote Address: What We Have Learned From SOC Is What Is Driving 3D Integration**
Cheng-Wen Wu - STC, ITRI, TW / Natl. Tsing-Hua U, TW

0925 **Keynote Address: OSAT - Role as Partner in 3D Integration**
Jacky Seiller - Amkor Technology, FR

1000 **SESSION 2: POSTERS**
Posters (see list on web) - coffee + tea break

1030 **SESSION 3: PAPERS**
Moderator: Herb Reiter - eda2asic, US

1030 **3D-PIC: An Error-Tolerant 3D CMOS Imager**
Hsiu-Ming (Sherman) Chang, Kwang-Ting (Tim) Cheng – UC Santa Barbara, US
Jiun-Lang Huang – Natl. Taiwan U, TW
Ding-Ming Kwai – ITRI, TW
Cheng-Wen Wu – ITRI, TW / Natl. Tsing-Hua U, TW

1100 **An Analytical Study on the Role of Thermal TSVs in a 3D-IC Chip Stack**
Min Ni, Qing Su, Zongwu Tang, Jamil Kawa - Synopsys, US

1130 **A Novel NOC Architecture Framework for 3D Chip MPSoC Implementations**
Konstantinos Tatas, Costas Kyriacou – Frederick U, Cyprus
Alexandros Bartzas, Kostas Siozios, Dimitrios Soudris – Natl. Techn. U. of Athens, GR

1200 **LUNCH BREAK**

1300 **SESSION 4: PAPERS**
Moderator: Stojan Kanev - Süss MicroTec, DE

1300 **High Aspect-Ratio Through-Silicon Vias: How Molecular Engineering Impacts the 3D-IC Design Space**
Claudio Truzzi, Frederic Raynal, Vincent Mevellec – Alchimer, FR

1330 **Debonding of Temporary Bonded Wafers with Topography for 3D Integration**
Peter Bisson, Sumant Sood, Jim Hermanowski, Wilfried Bair – Süss MicroTec, US

1400 **Modeling TSV Open Defects in Three-Dimensional Memory**
Li Jiang, Yuxi Liu, Qiang Xu – Chinese U of Hong-Kong, HK

1430 **SESSION 5: POSTERS**
Posters (see list on web) - coffee + tea break

1500 **SESSION 6: PANEL DISCUSSION**

"3D: A Reality?"
Moderator:
Jérôme Baron – Yole Developpement, FR

Panellists:
Stuart Ainslie – Advantest, DE
Eric Cirot – ST-Ericsson, FR
Vassilios Gerousis - Cadence Design Systems, US
Rajiv Maheshwary – Synopsys, US
Ian Phillips – ARM, UK
Jochen Reisinger – Infineon Technologies, DE

1600 **CLOSE**

W6

1st Workshop on Model Based Engineering for Embedded Systems Design (M-BED 2010)

Room – Konferenz 5

Organisers:
Pierre Boulet, Lille U, FR
Daniela Cancila, CEA LIST, FR
Huascar Espinoza, ESI-Tecnalia, ES
Adam Morawiec, ECSI, FR

Steering Committee:
Sebastien Gerard, CEA LIST, FR
Wolfgang Mueller, Paderborn U/C-LAB, DE
Laurent Rioux, Thales RT, FR
Bran Selic, Malina Software Corp., CA

The workshop is supported by MARTE Users' Group (www.marte-ug.org) the Adams support action (www.adams-project.org).

Description: The application of model-based engineering (MBE) methods for software and systems development in industry is increasing. Moreover, the integration of component-based approaches with MBE has further accelerated its adoption along with providing it with a sound theoretical foundation. The focus of this workshop is on the use of MBE for embedded systems development for example in the industrial transport sector for applications such as railway systems, automotive, aerospace, and related domains. In this context, special focus is given on MARTE, the UML profile for Modeling and Analysis of Real-Time and Embedded systems, which has been successfully adopted in several projects.

In particular, the intent is to concentrate on the following topics:

- The infrastructure that supports MBE, that is, the requisite languages, tools, and standards as well as the combination of design and V&V activities, and the diverse engineering disciplines involved in embedded system design.
- Process-related issues, such as guidelines for deciding when and where to use domain-specific languages, appropriate integration of process descriptions and tool mentors, and advanced methods to assist on criteria design and on performance and impact assessing.
- MARTE returns on experiences

The aim of the workshop is to bring together researchers and tool developers from industry and academia to discuss on applications of model-based engineering to industrial application domains as well as on MARTE usage and on safety and MARTE.

0830 **Workshop Introduction**

0835 **MARTE, Version 1**
Bran Selic*, Malina Software Corporation, CA

0900 **Invited Talk: Industrial motivation on the use of MARTE and retour on industrial experiences**
Laurent Rioux, Thales Research and Technologies, FR

0930 **SESSION 1: MARTE & POWER MODELING**

0930 **Extension to MARTE Profile for Modeling Dynamic Power Management of Embedded Systems**
Tero Arpinen, Erno Salminen, Timo D Hamalainen and Marko Hannikainen, TU Tampere, FI

0950 **Using MARTE for Designing Power Supply Section of WSNs**
Marcello Mura and Mauro Prevostini,
ALaRI - Faculty of Informatics – USI, CH

1010 **Modeling of Configurations for Embedded System Implementation in MARTE**
Imran Rafiq Quadri, Abdoulaye Gamatie, Pierre Boulet and Jean-Luc Dekeyser,
LIFL – univ. Lille 1, CNRS and INRIA Lille - Nord Europe, FR

1030 **COFFEE BREAK AND TOOL DEMOS**

1100 **SESSION 2: SAFETY ENGINEERING & INDUSTRIAL APPLICATIONS**

1100 **Invited Talk: Railway Industrial Requirements for Model-Based Safety Engineering**
F Belmonte, Alstom Transport Information Solution, FR

1120 **Integrating a SysML-based system modeling process with Safety Engineering**
Sven Scholz , Department of Ing., DE,
and Kleanthis Thramboulidis, Patras U, GR

1140 **Using MARTE in Code-centric Real-time Projects Providing Evolution Support**
Peter Ulbrich, Christoph Elsner, Martin Hoffmann, Reiner Schmid and Wolfgang Schroder-Preikschat, Friedrich-Alexander U, Erlangen-Nuremberg, DE

1200 **LUNCH BREAK**

1300 **SESSION 3: AUTOMOTIVE APPLICATION DOMAIN & Invited Talk: OMG MARTE V1**

1300 **Invited Talk: MARTE in Action**
Sebastien Gerard, CEA LIST, FR

1330 **Model-based approach for performance assessment of a video transmission application for automotive**
Sebastien Le Nours and Olivier Pasquier, IREENA, FR

1350 **Using MARTE in Code-centric Real-time Projects Providing Evolution Support**
Niklas Mellegard and Miroslaw Staron, TU Chalmers, SE

1410 **Model-based virtual prototyping for early automotive software systems evaluation**
Jochen Zimmermann, Michael Pressler, Alexander Vieh and Oliver Bringmann, FZI Karlsruhe, DE
Wolfgang Rosenstiel, Tuebingen U, DE

1430 **COFFEE BREAK AND TOOL DEMOS**

1500 **SESSION 4: HARDWARE AND SOFTWARE DESIGN, VALIDATION AND SYNTHESIS**

1500 **Novel Model Driven Design and validation techniques for Adaptive Cruise Control**
Wah Man Cheung, Essex U, UK
Gareth Howells, Kent U at Canterbury, UK
Klaus D McDonald-Maier, Essex U, UK
Andrew B. T. Hopkins, Essex U, UK
Tughrul Arslan, Edinburgh U, UK
and John Derrick, Kent U, UK

1520 **A UML Profile for SysML based comodeling, -simulation and -synthesis Of embedded Systems**
Fabian Mischkalla, Da He and Wolfgang Mueller,
University of Paderborn, DE

1540 **Managing Hardware Verification Complexity with Aspect-Oriented Model-Driven Engineering**
Eamonn Linehan and Siobhan Clarke,
Trinity College Dublin, IE

1550 **From idea to modeling workbench and executable code: Rapid Prototyping of innovative modeling concepts for embedded systems with Eclipse and Open Source**
Andreas Graf and Miriam Brueckner, itemis GmbH, DE

1600 **SESSION 5: METHODOLOGY AND TOOLS**

1600 **Are you aware of the design decisions? On how modeling should support design**
Hristina Moneva, Roelof Hamberg and Teade Punter,
Embedded Systems Institute, NL

1620 **Increasing Reliability of Embedded Systems in a SysML Centered MBSE Process: Application to LEA Project**
Robin Cressent, prisme / ensi bourges, FR
Pierre David, Heudiasyc UMR 6599, FR
Vincent Idasiak, prisme / ensi bourges, FR
and Frederic Kratz, prisme / ensi bourges, FR

1640 **Automatic Layout and Structure-Based Editing of UML Diagrams**
Hauke Fuhrmann, Miro Sponemann, Michael Matzen
and Reinhard von Hanxleden,
Christian-Albrechts-U, Kiel, DE

* To be confirmed. Otherwise, the OMG chair for MARTE v1, S. Gerard, will introduce MARTE v1.

fringe technical meetings

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – **www.date-conference.com**

Day	Time	Meeting & Contact	Room	Type
Mon	1800-2100	**EUROPRACTICE IC/MEMS and Software Service** Wayne McKinley <mckinley@iis.fraunhofer.de>	Konferenz 2	Open
Mon	1900-2100	**EDAA PhD Forum** Peter Marwedel <peter.marwedel@tu-dortmund.de>	Terrace	Open
Tues	1830-1930	**EDAA General Assembly** Norbert Wehn <wehn@eit.uni-kl.de>	Seminar 2	Open
Tues	1830-2030	**ETTTC Meeting** Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Konferenz 3	Open
Tues	1830-2130	**European SystemC Users Group Meeting** Axel Braun <abraun@informatik.uni-tuebingen.de>	Konferenz 2	Open
Thu	1400-1700	**Cadence-Europractice Technical Update Meeting** Patrick Haspel <phaspel@cadence.com>	Seminar 1	Open

PhD forum

Monday: Room – Terrace – 1900-2100

Organiser:
Peter Marwedel, TU Dortmund, DE

The EDAA/ACM PhD Forum at the Design, Automation and Test in Europe (DATE) Conference is a poster session and a buffet dinner organised and hosted by ACM SIGDA and the European Design and Automation Association (EDAA). The EDAA Best Dissertation Awards will be presented during the Wednesday lunch-time keynote session.

The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work. More information is available on the web – **www.date-conference.com**

Tool Seminars

Location: Seminar Level

New for DATE 10! Tool Seminars presented by leading tool vendors will be taking place in rooms on the Seminar Level of the ICC throughout DATE. Synopsys, Mentor Graphics and Artisan are among the vendors who will be giving a seminar. These are open to all attendees and exhibition visitors. As places are limited they will be available on a first-come, first-served basis and entrance vouchers will be available from the Conference Registration Desk located on the Terrace Level of the ICC.

Please see <www.date-conference.com> for details of the programme as it develops.

If your company is interested in booking a Tool Seminar please contact Claire Cartwright <claire.cartwright@ec.u-net.com>

This is a programme of free events open to all attendees at DATE 10 at the Exhibition Theatre

exhibition theatre

Chair:
Juergen Haase, edacentrum, DE

In addition to the conference programme during DATE 10, there will be a presentation theatre from Tuesday 9 March to Thursday 11 March 2010 on the exhibition floor: the DATE 10 Exhibition Theatre. Attendees will profit from having an industry forum in the midst of Europe's leading electronic system design event. The theatre is located on the show floor to thus afford easy access for conference delegates during the morning, lunchtime and afternoon exhibition breaks.

For the second time, six open Special Conference Sessions from Track 8 (full details are contained in the main conference programme pages) will take place in the Exhibition Theatre. These sessions are open to conference delegates as well as to exhibition visitors and are as follows:

2.8	**Panel Session**	**Tuesday 1130-1300**
	Are we there yet? Has System Assembly from IP Blocks Become Like Connecting LEGO Blocks?	
3.8	**Hot Topic**	**Tuesday 1430-1600**
	AUTOSAR and Automotive Software Design	
6.8	**Panel Session**	**Wednesday 1100-1230**
	The Challenges of Heterogeneous Multi-Core Debug	
7.8	**Panel Session**	**Wednesday 1430-1600**
	Who is Closing the Embedded Software Design Gap?	
10.8	**Panel Session**	**Thursday 1100-1230**
	Embedded Software Testing	
11.8	**Panel Session**	**Thursday 1400-1530**
	Reliability of Data Centers: Hardware vs. Software	

Additionally, expert panels of users, vendors and analysts will discuss industrial and business topics in the Exhibition Theatre. Engineering managers from leading electronics manufacturers will relate their own first-hand design experiences of commercial design tools.

The programme will focus on business and industry, providing managers and designers with valuable information in the fields of semiconductor and system design. Research reviews complete the picture by presenting an overview of the latest results of research work which is ready for application to industrial applications. Highlight topics include: Analogue & Mixed Signal Design, Embedded Software, ESL Design, Automotive Systems, Design for Manufacture, Multiprocessor Designs and "More than Moore" Designs.

Please see presented overleaf information on confirmed first-class panels as highlights of the initial Exhibition Theatre Programme. The full programme containing details of all other exhibition session slots is available on the DATE web portal and will be regularly updated.

Panel Session - Exhibition Theatre

Tuesday March 9, 1615-1745

Microelectronics is an important technological mainspring of the car industry – but does the trend towards fabless semiconductors really suppose a breakthrough with respect to the factors, currently under examination, that link microelectronics and the vehicle sector?

Organisers: Thomas Hoetzel, Atmel Automotive GmbH, DE
Gerd Teepe, Globalfoundries, DE

Moderator: Hans-Christian Reuss, FKFS Stuttgart, DE

Panellists: Wolfgang Breuer, Continental, DE
Christoph Hammerschmidt, EETimes, DE
Frank Kessler, BMW, DE
Reinhard Ploss, Infineon Technologies, DE
Thilo von Selchow, ZMDI, DE
Hans-Juergen Straub, X-FAB, DE

Abstract: Microelectronics is the technological mainspring of many different business sectors that have reached the ultimate stage in optimisation evolution. Innovation is increasingly driven by the supply industry, while businesses that actually apply the technology to consumer products, are actually undergoing a process of consolidation.

Developments in the automotive industry are following a similar track. As far as genuine innovation is concerned, car manufacturers are being faced with the challenge of proactively bringing new systems to bear for individual use. More than a few of the emerging megatrends, such as safety, electrical mobility or increased efficiency in the use of natural resources, are based on technical solutions that originally stem from the field of microelectronics.

When we consider the value chain of the car industry, this is not an altogether new or easily measurable phenomenon. There are, however, linking elements that the operational interplay of factors between sectors has in common. Among the unresolved questions in respect to measuring efficiency in increased productivity, one remains paramount: "How can the required cost reductions be applied without using 'design shrinks to new technology nodes' and without a negative outcome in terms of quality"? We also must consider the question of long-term availability and the ongoing concerns relating to the interaction between the vehicle-manufacturing and semiconductor sectors.

Tackling these issues in a forum of top experts drawn from the car-manufacturing, fabless semiconductor and foundry sectors is the goal of this panel, which shall convene on DATE 10. This endeavour is based on the conviction that any progress can only be achieved if the best concepts from all three sectors are combined.

Panel Session - Exhibition Theatre

Wednesday March 10, 1615-1715

European EDA SMEs team up

Organiser/ Moderator: Juergen Haase, edacentrum GmbH, DE

Panellists: TBD

Abstract: This panel will provide a comprehensive overview of the European EDA (Electronic Design Automation) start-up scene. With 25+ companies and a work force of over 450 highly skilled technical and management specialists, they are a very important source of innovation for the semiconductor industry. European EDA SMEs provide unique capabilities and therefore add substantial value to all phases of the design, development and manufacturing processes of integrated circuits and electronic systems – a key force to staying competitive in the global economy.

Now these companies have organised themselves in a "European EDA SMEs" group and join forces for enabling even more innovation. This panel will give an overview about the companies of the group and discuss the solutions that are enabled by this group. Special focus will be on the advantages of acting them as a group and how users can benefit from their innovations and their solutions.

Panel Session - Exhibition Theatre

Thursday March 11, 1245-1345

Lots of Foundries and Fabless Companies do exist – what about standards for their interface?

Organisers: Manfred Dietrich, Fraunhofer IIS/EAS, DE
Rene Schueffny, TU Dresden, DE

Moderator: Dirk Friebel, Fraunhofer IIS/EAS, DE

Panellists: Andreas Foglar, LANTIQ GmbH, DE
Thomas Hoetzel, Atmel Automotive GmbH, DE
Jens Kosch, X-FAB AG, DE
Joachim Mueller, Globalfoundries, DE
Reimund Wittmann, IPGEN GmbH, DE

Abstract: Companies like Broadcom and Nvidia have shown that the Fabless model conquers the semiconductor market. Today all IDM's use foundries as second source or use it as part of their volume production because of the high cost of new manufacturing facilities IDM's become Fablight and concentrate with their production on highly sophisticated processes. How is it possible to handle even more complex circuits if their processes cannot any more be deeply influenced by the internal design team? Today the value chain of the semiconductor market isolates and dominates more and more the vertical companies like EDA, Design house, Fabless, IP provider, Foundry Test & Packaging. Do we have already enough standards or do we need more and where do we need more standards and how can we make it happen? Who will be the driver or who should be the driver? This panel should offer some answers or even create more questions!

It is fact – Fabless companies will have more and more impact in the whole IC logic market and Foundries increase their market share every year! It's time for standards.

university booth demonstrations

DATE 10 will feature the University Booth where system and VLSI CAD tools developed in Universities and Research Institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists.

The University Booth will be located in the Exhibition Hall and will be furnished with popular workstations. A rotating schedule will operate throughout the three days.

Any University interested should contact:

Jens Lienig <jens@ieee.org>

Volker Schoeber <schoeber@edacentrum.de>

vendor exhibition

DATE 10 Exhibitors and Sponsors include:

Access Project

AIT Austrian Institute of Technology GmbH

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Coconut Project

Cool Silcon

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DOCEA Power

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EDA Tech Forum

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EE Times

Elektronik i Norden

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ICT 2020

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Springer

Tanner EDA

Target

The Next Silicon Valley

TU Dresden

University booth

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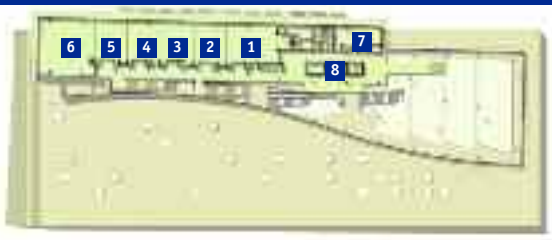
Conference level

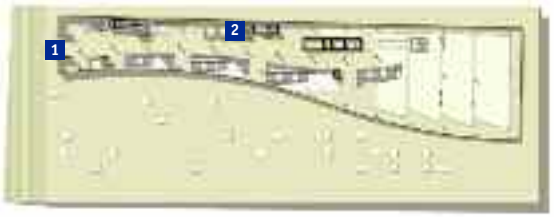


1 - 6 Conference Rooms 7 AV HQ/Practice 8 Press Lounge

Seminar level

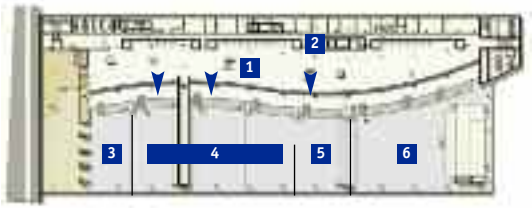
1 - 7 Seminar/Meeting Rooms

Terrace level



1 Main Entrance 2 Registration/Bags

Ground (Saal) floor



1 IP Sessions 2 Cloaks 3 Conference Room (Saal 5)
4 Exhibition/Exhibition Theatre/Delegate Coffee 5 Speakers' Breakfast
6 Opening Session (Tues)

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DATE 10

Design, Automation & Test in Europe

ICC, Dresden Map

By car

Motorway A4 Take the exit “Dresden Altstadt” and follow the signage towards the downtown area / Congress Center on the B6 highway.

By train

Take a train (IC or ICE) to the main Dresden railway station, then take the tram number 11 towards Bühlau and get off at the "Kongresscenter" station. Walk on the "Könneritzstraße" towards the "Marienbrücke" bridge and turn right into "Devrientstraße." The first street on your left is "Ostra-Ufer."

Take a train (IC or ICE) to the main Dresden railway station, then travel one stop on the S-Bahn towards Meissen-Triebischtal until the railway station "Bahnhof Dresden Mitte." Walk in the direction of the tram on the "Könneritzstraße" until you reach the "Marienbrücke" bridge. Right before the bridge, turn right into "Devrientstraße." The first street on your left is "Ostra-Ufer."

Take a train (IC or ICE) to the "Bahnhof Dresden Neustadt" railway station, then take the tram number 11 towards Zschertnitz and travel two stops until "Kongresszentrum". When crossing the "Marienbrücke" bridge, you see the MARITIM Hotel & International Congress Center on your left. Walk on "Könneritzstraße" back to the "Marienbrücke" bridge and turn right into "Devrientstraße." The first street on your left is "Ostra-Ufer."

By plane

From the Dresden Klotzsche airport, take the tram (S-Bahn, in the basement of the terminal) to the "Bahnhof Dresden Neustadt" railway station. From there switch to the tram number 6 towards Gorbitz and travel two stops until "Kongresszentrum" or Take the tram number 11 towards Zschertnitz and travel two stops until "Kongresszentrum". When crossing the "Marienbrücke" bridge, you can see the MARITIM Hotel & International Congress Center on your left. Walk on "Könneritzstraße" until the "Marienbrücke" bridge