PinHaT – A Tool for the automatic generation of Multiprocessor Systems-on-Chip

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Abstract

The PinHaT software allows the automatic generation of an FPGA-based multiprocessor systems from a parallel program. Therefore, Integer Linear Programming and the FPGA vendor tool-chain are used.

1. Introduction

As apparent in current developments the reduction of transistor size and the exploitation of instruction-level parallelization can not longer be continued to enhance the performance of processors. Instead, multi-processor systems are a common way of enhancing performance by exploiting parallelism of applications. This project deals with the automated design of multiprocessor systems from applications using combinatorial optimazation.

2. The Synthesis Flow

In figure 1 the underlying design methodology of PinHaT is shown. The flow currently starts with a MPI applications and ends with a bit-stream used for the configuration of an FPGA [1].

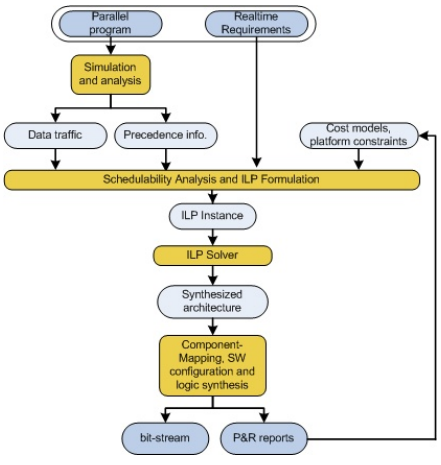

Figure 1: Architectural Synthesis Flow

In this flow, the communication between processing elements shall be described with MPI. The application is then simulated and analyzed to obtain information about task precedence and inter-task data traffic. This information is used to specify an instance of an Integer Linear Program (ILP) problem. Additionally, constraints of processing elements and communication networks for a target platform are needed. That is, in the case of Xilinx for instance the actual size of the FPGA, costs for the processing elements, like MicroBlaze or PowerPC processor or the bandwidth and latency of a communication networks

3. The PinHaT software

The current version of the PinHaT software is written in JAVA and integrates the described synthesis flow in an easy to use environment (see figure 2) [2].

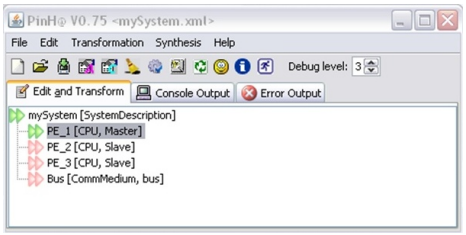

Figure 2: PinHaT

4. Conclusion & Outlook

PinHaT eases the design of multiprocessor-systems on chip by allowing the automated architecture synthesis from a parallel application and the connection to the FPGA vendor tool-chain for the creation of the bit-file. Currently, the flow is extended to allow (semi-)automatic parallelization of C programms. A first work in this direction was presented in [3].

5. References

[1] H. Ishebabi and C. Bobda. *"Automated architecture synthesis for adaptive multiprocessors on chip systems"*, Journal of Microprocessors and Microsystems. Elsevier Science, August 2008.

[2] P. Mahr, H. Ishebabi, B. Andres, C. Lörchner, M. Metzner and C. Bobda, *"Automated Design Approach for on-Chip Multiprocessor Systems"*, FPGAworld Conference 2008, 11.09.2008, Sweden.

[3] P. Mahr, B. Andres, H. Ishebabi and C. Bobda, *"A Design Methodology for Reconfigurable Heterogeneous Architectures"*, MRSC'09, Berlin, Germany, March 25-26, 2009.