Call for Papers

Test Track at DATE 2010

Dresden, Germany
March 8-12, 2010

The **Design, Automation and Test in Europe conference and exhibition** is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test, and manufacturing of electronic systems and circuits. One of the tracks of DATE is devoted to **Methods, Tools and Innovative Experiences in Testing Electronic Circuits and Systems**. You are invited to submit your research contributions to the test track.
This five-day event consists of a **conference** with plenary keynotes, regular papers, interactive presentations, panels and hot-topic sessions, tutorials, master courses and workshops, as well as a Designers' Forum. The DATE conference and the exhibition, together with the many user group meetings, fringe meetings, university booth and social events offer a wide variety of opportunities to meet and exchange information.

TEST TOPIC AREAS

The test track is organised in six topics. These topics together with their chairs and area descriptions are given as follows.

T1 System and Industrial Test
Chairs: Erik Jan Marinissen, IMEC, Belgium; Peter Harrod, ARM Ltd, UK

Testing at various levels of a system: embedded core, System-on-Chip, System-in-Package, board, system; testing 3D (TSV-based) chips; Network-on-Chip test; system-level debug and validation; hardware/software system test; processor-based test; infrastructure IP; industrial test: test equipment, including ATE hardware and software, probe stations, handlers; multi-site testing; economics of test; case studies.

T2 Design for Test and BIST
Chairs: Krishnendu Chakrabarty, Duke Univ., USA; Sandeep Kumar Goel, USA

Design for test, debug and manufacturability; built-in self-test and built-in diagnosis; synthesis for testability; test resource partitioning, embedded test; test data compression; scan-based test and diagnosis; BIST for memories and regular structures, low power DfT techniques, DfT for secure systems, Dft economics.

T3 Test Generation, Simulation and Diagnosis
Chairs: Nicola Nicolici, McMaster University, Canada; Bart Vermeulen, NXP, The Netherlands
Test pattern generation; high-level TPG; delay TPG; fault simulation; test generation for validation, debug and diagnosis; low-power TPG; TPG for memories and FPGAs.

T4 On-Line Testing and Fault Tolerance
Chairs: Dimitris Gizopoulos, University of Piraeus, Greece; Davide Appello, STMicroelectronics, Italy

Transient fault evaluation; soft error susceptibility; on-line testing and fault tolerance for signal integrity; concurrent monitors and diagnosis; coding techniques; in-field testing and diagnosis; on-line testing; high availability systems; secure and safe circuits and systems design; dependability evaluation, dependable system design; redundant systems design; hardware/software recovery; self-repair; fault tolerance; on-line testing and fault tolerance for industrial applications.

T5 Test for Variability, Reliability and Defects
Chairs: Sandip Kundu, Massachusetts Univ., USA; Rob Aitken, ARM, USA

Identification, characterization and modeling of defects, faults and degradation mechanisms; Defect based fault analysis, Simulation and ATPG of defect based faults; Reliability analysis and modeling techniques, FMEA and Physics of failure; Test for noise and uncertainty; Design for Reliability and Design for Variability and their impact on test; Test and reliability of redundant systems; Test and reliability issues in the presence of leakage; Challenges of ultra low-power design on test and reliability; Modeling and test techniques for physical sources of errors such as process, voltage and temperature variations; Error-resilient nano design systems.

T6 Analog, Mixed-Signal, RF and Mixed-Technology Test
Chairs: Hans Kerkhoff, University of Twente, The Netherlands; Abhijit Chatterjee, Georgia Institute of Technology, USA

Test techniques for mixed-signal, RF and multi-GHz electronics; Test techniques for embedded MEMS/bioMEMS/MOEMS sensors and actuators; assembly engineering for SiP/SoC/SoP/PoP; Failure modelling and analysis techniques; Defect characterization and fault modelling; Fault simulation and test generation algorithms; DfT/DfM/DfY/DfR (DfX) techniques; BIST; Test coverage metrics and statistical modeling; Effective defect screening techniques; Diagnosis and self-repair.

SUBMISSION INSTRUCTIONS

All manuscripts must be submitted electronically before **September 6th, 2009**, following the instructions on the conference Web page:

www.date-conference.com

The accepted file format is PDF Manuscripts received in hard-copy form will not be processed.
Papers can be submitted for either standard oral presentation or for interactive presentation. Standard oral presentations require novel and complete research work supported by experimental results, and are held in front of a full audience. Besides these, DATE will again include interactive presentations of novel ideas that may require additional research or lack experimental data. Presentations are given on a laptop in a face-to-face discussion area.
Submissions should not exceed 6 pages in length for oral-presentation and 4 pages in length for interactive-presentation papers, and should be formatted as close as possible to the final format: A4 or letter sheets, double column, single spaced, Times or equivalent font of minimum 10pt (templates are available on the DATE Web site for your convenience). To permit blind review, submissions should not include the author names. Any submission not in line with the above rules will be discarded.
All papers will be evaluated with regard to their suitability for the conference, originality and technical soundness. The Programme Committee reserves the right to accept interesting contributions that do not meet the criteria for standard oral presentations, as interactive presentations.

INFORMATION

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