Call for Papers

D Track: Design Methods, Tools, Algorithms and Languages

Dresden, Germany
March 8-12, 2010

The **Design, Automation and Test in Europe conference and exhibition** is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test, and manufacturing of electronic systems and circuits.

The classical D track on **Design Methods, Tools, Algorithms and Languages** is devoted to design automation and design tools for electronic and embedded systems. Emphasis is on methods, tools, algorithms and languages related to the use of computers in designing products. This includes designer feedback on existing design methods and tools as well as to initiate discussions on requirements of future system architectures, design flows and environments. You are invited to submit your research contributions as regular papers or as interactive presentations.

TOPICS

The D track is organised in seventeen topics. These topics together with their chairs and area descriptions are given as follows.

D1 System Specification and Modeling
Chairs: Eugenio. Villar, Universidad de Cantabria, Spain; Grant Martin, Tensilica Inc., USA

Modeling and specification methodologies for complex, HW-SW embedded systems; system modeling and specification languages; Model-Driven Engineering; metamodelling; executable specifications; analog-mixed signal and heterogeneous modeling and specification, models of computation; formal specification and semantics.

D2 MPSoC and System Design Methods
Chairs: Andy Pimentel,University of Amsterdam, The Netherlands; Wido Kruijtzer, NXP, The Netherlands

Multi-core SoC architecture, simulation and design of multi-core SoC; electronic design methods, tool flows and their practical application; application-specific design methodologies, particularly for embedded systems hardware and software; targeted specification, modelling, and validation flows; design reuse and platform design support tools;

D3 System Synthesis and Optimization
Chairs: Peter Marwedel, University of Dortmund, Germany; Samarjit *Chakraborty, Technical University Munich, Germany*

Synthesis of complete systems, application- and domain-specific synthesis techniques; system-level models for design, optimization and synthesis; hardware/software co-design and partitioning issues; hardware/software interface and communication synthesis; interface-based and correct-by construction designs; system-level scheduling techniques; protocol synthesis and optimization; system optimization for all cost functions (timing, electrical, non-functional); multi-objective, classical and nature-inspired optimization techniques for system level design; large-scale and industrial case studies involving full system optimization and synthesis.

D4 Simulation and Validation
Chairs: Ian Harris, University of California Irvine, USA; Valeria Bertacco, University of Michigan, USA

Advanced simulation and emulation techniques from system to circuit level; simulation accelerators; multi-domain simulation techniques for mixed systems; transaction-level validation, hardware/software co-simulation and validation, ATPG for validation; testbench generation; simulation-based verification; semi-formal verification techniques, design error debug and diagnosis

D5 Design of Low Power Systems
Chairs: Miguel Miranda, IMEC, Belgium; Alberto Macii, Politechnico di Torino*, Italy*

Design methods, techniques and case studies of low power systems, covering aspects from specification, mapping, system architecture to circuit, including HW, SW, power management, batteries, energy harvesting, thermal aware computation and technology aware design aspects in nanometer technologies (i.e., leakage, variability, reliability, 3D stacking, etc)

D6 Power Estimation and Optimization
Chairs: Jörg Henkel, University of Kaiserslautern, Germany; *Kaushik Roy, Purdue University, USA*

Algorithms, techniques and tools for power modelling, estimation and optimization of electronic systems applicable at all levels of the design hierarchy, from system-level specification to layout, including software and run-time management.

D7 Emerging Technologies, Systems and Applications
Chairs: Pol Marcal, IMEC, Belgium; Yuan Xie, Penn State University, USA

System design methods, models of computation, and case studies for emerging applications: ambient intelligence, ubiquitous computing, wearable computing, sensor networks, bio-inspired computation; Design automation flows and case studies for upcoming and future technologies: MEMS, BIOMEMS, Lab-on-a-chip, 3D integration, nanoscale and molecular scale circuits and systems.

D8 Formal Methods and Verification
Chairs: Jason Baumgartner, IBM, USA; Joao Marques-Silva, University College Dublin, Ireland

Formal verification and specification techniques (including equivalence checking, model checking, symbolic simulation, theorem-proving, abstraction and refinement techniques, and real time verification); technologies supporting formal verification (including SMT, SAT, BDD, ATPG, and related work); semi-formal verification techniques; applications and case studies; formal verification of IPs, SoCs, cores and real-time/embedded systems; verification in practice, namely the integration of verification into the design flow.

D9 Network on Chip
Chairs: Lin-Shiuan Peh, Princeton University, USA; Davide Bertozzi, University of Ferrara, Italy

Architecture, modelling and design techniques for network on chip; design methods for the on-chip interconnection network: interconnect topology, routing and flow control methods; architecture and design for fault-tolerance, quality of service, dynamic voltage and frequency scaling, GALS synchronization in networks on chip; physical design techniques and methodologies; hardware/software communication abstraction, component-based modelling, platform-based design and methodologies, NoC exploration frameworks; design for on-chip networks based on alternative technologies such as photonics, wireless, 3D stacking, etc.

D10 Architectural and Microarchitectural Design
Chairs: Dionisios Pnevmatikatos, Forth-ICS, Greece; Christos Kozyrakis, Stanford University, USA

Architectural and microarchitectural design Techniques, memory systems, power and energy efficient architectures, pipelining, caching, branch prediction, multithreading techniques, modelling and performance analysis, advanced computer architecture for application-specific applications, special purpose processors and accelerators, arithmetic architectures.

D11 Architectural and High-Level Synthesis
Chairs: Paolo Ienne, EPFL, Switzerland; Philippe Coussy, Université de Bretagne-Sud, France

Synthesis of hardware systems from high-level descriptions; hardware-centric system-level synthesis, analysis, and optimization; high-level language hardware description, parsing and compilation; scheduling, allocation, and binding of operations, variables, and transfers; automatic design and optimization of datapaths, dedicated memory and communication structures, and controllers; performance, cost, and power driven architectural-level optimisations; application-specific processor generation, automatic processor customization, and accelerator synthesis.

D12 Reconfigurable Computing
Chairs: Jürgen Becker,University of Karlsruhe, Germany ; *Patrick Lysaght, Xilinx, USA*

Statically and dynamically reconfigurable and reprogrammable systems and components: platforms and architectures, FPGAs, reconfigurable processors, design methods and tools for reconfigurable computing and communication, applications.

D13 Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
Chairs: Steven Nowick, Columbia University, USA; Michel Berkelaar, Delft University of Technology, The Netherlands

Combinational and sequential synthesis; data structures for synthesis; technology mapping; hierarchical and non-hierarchical controller synthesis; state assignment; methods for FSM optimization, synthesis and analysis; asynchronous and mixed synchronous/asynchronous circuits; performance and timing driven synthesis; PLD and FPGA synthesis; combined logic synthesis and layout design, statistical timing analysis, timing closure; arithmetic circuits

D14 Physical Design and Verification
Chairs: Igor Markov, University of Michigan, USA; Jens Lienig, Techical University of Dresden, Germany

Floorplanning; automatic place and route; module generation; design rule checking and layout characterization; electrical verification; problems in deep sub-micron and high-speed design; interconnect-driven and performance-driven layout; process technology developments; design for manufacturability.

D15 Virtualization Technologies
Chairs: Andre Brinkmann, University of Paderborn, Germany; Mike Kreiten, AMD, Germany

Architectures, systems, tools, methodologies, and algorithms for platform and resource virtualization like server virtualization, IO virtualization, and storage virtualization; (embedded) hardware architectures and instruction sets, single/multi root IOV, address translation and DMA remapping, binary translation and emulation, migration and checkpointing, consolidation, isolation, encapsulation, interposition, security.

D16 Analogue and Mixed-Signal Systems and Circuits
Chairs: Tom Kazmierski, University of Southampton, UK; Christoph Grimm, Technical University of Vienna, Austria

CAD for analogue and mixed-signal circuits and systems: Layout, Topology generation, Architecture and System Synthesis, Modelling of AMS circuits and systems, Modelling strategies, Modelling of complex analogue mixed-signal systems, Model generation, Formal and Symbolic Techniques; Languages for AMS circuits and systems: VHDL-AMS, Verilog-AMS, SystemC-AMS, Matlab/Simulink, Ptolomy; Innovative circuit topologies and architectures: Topologies/architectures that increase robustness, Topologies/architectures that increase re-usability; Modelling and Synthesis of Multi-Domain systems: MEMS, Energy Harvesting Systems.

D17 Interconnect, EMC and Packaging Modelling
Chairs: Wim Schilders,NXP, The Netherlands; Tom Dhaene, University of Ghent, Belgium

Modelling, characterisation and analysis of on and off chip interconnects and packaging; modelling and analysis of noise due to electromagnetic interaction on signal, power/ground and substrate; electromagnetic emission, susceptibility and compatibility.

SUBMISSION INSTRUCTIONS

All manuscripts must be submitted electronically before **September 6th, 2009**, following the instructions on the conference Web page:

www.date-conference.com

The accepted file format is PDF Manuscripts received in hard-copy form will not be processed.
Papers can be submitted for either standard oral presentation or for interactive presentation. Standard oral presentations require novel and complete research work supported by experimental results, and are held in front of a full audience. Besides these, DATE will again include interactive presentations of novel ideas that may require additional research or lack experimental data. Presentations are given on a laptop in a face-to-face discussion area.

Submissions should not exceed 6 pages in length for oral-presentation and 4 pages in length for interactive-presentation papers, and should be formatted as close as possible to the final format: A4 or letter sheets, double column, single spaced, Times or equivalent font of minimum 10pt (templates are available on the DATE Web site for your convenience). To permit blind review, submissions should not include the author names. Any submission not in line with the above rules will be discarded.

All papers will be evaluated with regard to their suitability for the conference, originality and technical soundness. The Programme Committee reserves the right to accept interesting contributions that do not meet the criteria for standard oral presentations, as interactive presentations.

INFORMATION

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