Predictive Parallel Event-driven HDL Simulation with A New Powerful Prediction Strategy

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Abstract— **Traditional parallel event-driven HDL simulation methods suffer heavy synchronization & communication overhead for timely transferring the signal data among local simulators, which could easily nullify most of the expected simulation speed-up from parallelization. A new predictive parallel event-driven HDL simulation as a new promising approach had been proposed for enhancing simulation performance. In this paper, we have further enhanced this noble parallel simulation method for a series of not only timing, but also function oriented design changes with a new powerful prediction strategy. Experimentation with real SOC designs from industry has been performed for actual design changes, and shown the effectiveness of the enhanced approach.**

Keywords—parallel event-driven simulation; simulation; verification; SOC; EDA

I. INTRODUCTION

Event-driven Hardware Description Language (HDL) simulation suffers from very low performance for complex designs because of its inherently sequential nature. Especially, this has gotten much worse in gate-level simulation than Register Transfer Level (RTL) simulation because the number of simulation objects to be dealt with is much larger at gate-level than at RTL. But, the use of gate-level functional or timing simulation is still quite active and even increasing nowadays for many important reasons [1]. Parallel event-driven HDL simulation has been proposed to alleviate the low performance of sequential simulation [2][3][4]. Unfortunately, it had been not successful because of; i) difficulty in design partitioning, ii) heavy synchronization and communication overhead among partitioned modules, especially in gate-level timing simulation, and iii) load balancing among the distributed simulation jobs [5]. Recently, a new noble distributed parallel event-driven simulation method based on the prediction had been proposed [6]. Afterward, the successive papers published had shown the effectiveness of the method [7][8]. In this paper, we have further enhanced this predictive parallel event-driven HDL simulation method for a series of not only timing, but also function oriented design changes with a new powerful prediction strategy. Experimentation with real System On Chip (SOC) designs from industry has been performed for actual design changes, and has shown the effectiveness of the approach.

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II. PREDICTIVE PARALLEL EVENT-DRIVEN HDL SIMULATION

We will call each of the simulations for a partitioned module in parallel event-driven simulation as *local simulation*. Unlike to apply actual input vales in traditional parallel event-driven simulation, predictive parallel event-driven HDL simulation method applies the predicted input values to the input ports of a partitioned module assigned to a given simulator. Then, the actual output values at the output ports of that module are compared on the fly with the predicted output values. Note that, when a partitioned module uses its actual inputs supplied from other partitioned modules, synchronization and communication overhead incurs.

In this method, however, as long as the prediction is correct, communication and synchronization among local simulations is completely eliminated. We call this phase of parallel simulation the *prediction phase*. Only when the prediction fails, the actual input values, coming from the other local simulation, are used in simulation; we call this phase of parallel simulation the *actual phase*. When prediction fails, each local simulation must roll back to the nearest checkpoint and is restarted from that point. This is possible by generating *checkpoint,* i.e., saving simulation state or design state, during the simulation in the prediction phase. Note also that, when this predictive parallel simulation enters the actual phase, it should try to return to the prediction phase as early as possible to attain the maximal speed-up. This is done by continuously comparing the actual outputs of all local simulations with their predicted outputs and counting the number of matches on the fly. If the number of matches exceeds a predetermined value, the simulation is switched back to the prediction phase. Therefore, it is obvious that prediction accuracy is the most critical factor in this approach. How to accurately predict input and output values is explained in the next section.

III. PREDICTIVE PARALLEL EVENT-DRIVEN HDL SIMULATION WITH MORE POWERFUL PREDICTION STRATEGY

Having an accurate prediction data is imperative in the predictive parallel event-driven HDL simulation, e.g. as the 100% accurate prediction data results in the zero communication and synchronization, the linear speed-up becomes possible.

Simulation is the highly repeated activity from high abstraction level to low one (e.g. from RTL simulation to gate-level simulation), and also before and after a series of continuous design changes at the same abstraction level. In other words, except the very 1st simulation, there are three kinds of earlier simulation prior to the current simulation; i) higher-level simulation, ii) same-level simulation before a design change, and iii) same-level simulation without any design changes. There are three cases to obtain the accurate prediction data, the first from the earlier simulation with the more abstractive model at the higher abstraction level (Case I), the second from the earlier simulation before a design change at the same abstraction level (Case II), and the third, although trivial, from the earlier simulation without any design changes at the same abstraction level (Case III). The dump data on the input ports (for the prediction input) and the output ports (for the prediction output) of the partitioned modules is saved during the earlier simulation, and is used as the prediction data in the predictive parallel HDL simulation for the later simulation. It already had been shown that the prediction accuracy is near to 100% for Case I [7]. For Case II, there are two types of design changes, function-oriented and timing-oriented. It had been discovered that the timing-oriented design changes result in the high prediction accuracy, also more than 95% [8]. However, there is no guarantee of high prediction accuracy for function oriented design changes as they could drastically alter the behavior of design. So far, the prediction scheme for predictive parallel event-driven HDL simulation is pretty simple so that the actual phase of simulation must be immediately invoked after possible rollback as soon as a prediction fails.

In this paper, we have further enhanced the predictive parallel event-driven HDL simulation for both function and timing oriented design changes. Our idea for providing the high prediction accuracy even for function oriented design changes is to utilize *a pair of prediction data simultaneously,* one from the earlier simulation before the design change at the same abstraction level and the other from the earlier simulation with a simulation model at the higher abstraction level *after the design change*. With a pair of prediction data, we could deploy not only the primary prediction, but also the secondary prediction when the primary prediction fails. When there is no such higher-level model available, the secondary prediction data could be alternatively collected from another faster simulation only for the small sub-module, which contains the design change. The primary prediction input data is used as the input stimuli for this small sub-module simulation. Also, we propose one more prediction strategy, *the self-prediction*, in which a local simulation predicts the necessary simulation data *for itself on the fly* during the execution of simulation. The self-prediction is especially powerful for signals whose values are changed to periodic, or constant from design changes. It is obvious that the predictive parallel event-driven HDL simulation equipped with our enhanced prediction strategy could stay longer at the prediction phase of simulation, as ours should increase the prediction accuracy.

IV. EXPERIMENTATION

For experimentally proving the effectiveness of our new prediction strategy, we compare the prediction accuracy of ours to that of the original simple prediction strategy. We use two real large SOC designs from industry. The first design is a RTL design for RTL functional simulation, and the second design is a gate-level netlist with SDF (Standard Delay Format) annotated for gate-level timing simulation. A major commercial Verilog simulator from one EDA vendor is used in the experiment. The experimentation procedure is following; (i) while the 1st simulation is being executed, the profiling collects the simulation event activities for major Verilog modules in design for an sub-optimal partition, (ii) an sub-optimal partition for balancing the simulation event activities evenly among local simulations is chosen, (iii) while executing the 2nd simulation, the primary prediction data is collected, (iv) a function design change is made, (v) while executing the 3rd simulation, the secondary prediction data is collected, (vi) while executing the 4th simulation, the actual data is saved, and (vii) the prediction accuracy of new strategy is compared to that of original. Note that steps (i) and (iii) could be merged, followed by step (ii). Also, note that simulation at step (v) is the higher-level simulation after a function-oriented design change. As this simulation is higher-level simulation, it is much faster than those simulations at steps (i) and (ii). For our gate-level timing simulation experiment with the second design, this higher-level simulation is zero-delay gate-level simulation, which is an order of magnitude faster on average. Also, for our RTL functional simulation with the first design we have performed the faster sub-module simulation for collecting the secondary prediction data, as the higher-level model such as cycle-accurate transactional level model was not available during the experiment.

Table 1. Prediction Accuracy of Two Strategies

Design	SOC1*	SOC2**	SOC3**
Simple prediction	49.3 %	4.0 %	98.0 %
Proposed prediction	92.7 %	99.9 %	98.0 %

*: gate level, **: RTL

As shown in Table 1, the new prediction strategy has increased the prediction accuracy by 46 % on average. From the increased prediction accuracy, much faster predictive parallel event-driven HDL simulation is definitely anticipated. We are currently developing a prototype of our predictive parallel event-driven HDL simulator.

V. CONCLUSION

High prediction accuracy is a critical factor in the predictive parallel event-driven HDL simulation. However, some function oriented design changes could result in low prediction accuracy. In this paper, we have proposed a new prediction strategy of the predictive parallel event-driven HDL simulation method for a series of not only timing, but also function oriented design changes. Experimentation with real designs from industry has shown the effectiveness of our approach.

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