Resistive Memories: Which Applications?

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***Abstract*— Recent announcement of 16Gbits Resistive memory from Sony shows the trend to quickly adopt resistive memories as an alternative to DRAM. However, using ReRAM for embedded computing is still a futuristic goal. This paper approaches two applications based on ReRAM-devices for gaining area, performance or power consumption. The first application is FPGA, one of the first architecture that can benefit the most from ReRAM integration to reduce footprint and save energy. The second application relates to ultra-low-power systems and the way to obtain an instantaneous "freeze" mode in devices for Internet of Things.**

***Keywords*— NVM, ReRAM, FPGA, FlipFlop, Memristors**

I. INTRODUCTION

The wireless communication field has experienced phenomenal growth during the last decade and has been a strong driver for semiconductor products. This growth has resulted in a large and steady increase in data and computing centers, with billions of mobile devices connected to them. This trend is not going to decline in the future with trillions of ultra-low power (ULP) embedded systems (smart devices, Internet of Things) expected, culminating in creation of smart environments and self-aware things for digital society targeting climate, food, energy, mobility, and health applications.

Improving energy efficiency has become a major concern and research challenge for all the microelectronic systems from servers to ULP embedded systems. On one side, servers get more energy hungry as they become more powerful, increasing operating expenses and investments in datacenters to manage the power dissipation. Then, the industry is considering using mobile technologies for power saving. On the other side, mobile applications and ULP embedded systems have highlighted the need for circuit operating over a wide voltage range. The uniqueness of these applications is that their computing power requirement varies considerably over time (e.g. from standby mode to video for mobile phones). Therefore, the circuit design has to be efficient even in standby and as well as at normal operating mode. Moreover, ULP embedded system will operate frequently at a very low duty cycle in burst mode. The applications in question will often require running permanently for at least 10 years on a small battery or harvested energy. Minimizing drastically the standby power is a primary concern in order to enable a long field time without battery replacement or energy replenishments.

CMOS technology scaling does not provide enough power saving and require extensive power management design tricks to optimize power saving. Design techniques like Power Gating (PG) and Adaptive Voltage and Frequency Scaling (AVFS) are commonly used to dynamically tune the voltage between 0V and its maximum value with several intermediate stages in order to: (i) dynamically switch-off any unused sub-circuit; (ii) dynamically track the optimal point according to on-going application requirements. However, these solutions do not guarantee zero leakage, when data must be kept for future usage, with memories being the weak link of the low-power strategy, leading to relatively high sleep-mode leakage.

Hence, increasing effort towards Non-Volatile Memories (NVM) for the next generation device applications is aggressively pursued. Emerging memristor technologies such as magnetic RAM (MRAM or STT-RAM), Phase-change Memory (PCM), and Resistive RAM (ReRAM) are actively pursued, due to the advantages of low writing voltage, high density, non-volatility, zero standby power from memory cells and a back end of Line integration (BE) with no impact on the front end (FE). Among these memory technologies, ReRAM appear as the most promising candidate due to a lower consumption compared to PCM and a simpler and smaller cell structure compared to MRAM (TABLE I.). ReRAM has been demonstrated with excellent scalability down to a 10nm cell size [1] and with the capability of very high density using cross-point array structures [2]. Even if the endurance is higher than standard Flash technology, it remains limited for high DRAM and cache replacement. Therefore, memory suppliers are considering ReRAM as replacement for Flash memory in Solid State Disk and use it as storage class memory [2], which require dense memory with a low access rate.

TABLE I. NVM ELECTRICAL CHARAC. VS. DRAM CELL (ISSCC, IEDM)

Features	DRAM	FLASH	MRAM	PCM	ReRAM	
		Nand	STT		OxRAM	CBRAM
Integration	FE	FE	BE	BE	BE	BE
Scalability	32nm	15nm	20-30nm	10-20 nm	10 nm	10-20 nm
Density	4-6f^2	4f^2	35-40f^2	6-8f^2	4-6f^2	4-6f^2
Write voltage	V_{NOM}	>10V	1V	3-5V	1-2.5V	1-2.5V
Write time	50ns	0.1ms	20ns	10ns	10-50ns	100-1000ns
Write energy	90fJ/bit		2.5pJ/bit	20pJ/bit	10-100fJ/bit	10-100fJ/bit
Endurance	1E^{+15}	1E$^{+4\text{-}5}$	1E$^{+12\text{-}15}$	1E^{+9}	1E$^{+6\text{-}10}$	1E$^{+5\text{-}6}$

However ReRAM devices hold promise for a complete renewal of the IC landscape if ReRAM integration in embedded systems becomes a reality. This paper discusses about design opportunities for embedded computing. It first takes the example of Field-Programmable-Gate-Arrays (FPGA), devices currently used in embedded systems but highly suffering from leakage power. We then extend the idea towards ULP devices. The remainder of this paper is organized

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as follows: Section II introduces ReRAM technologies. Section III addresses FPGA design. Section IV extends this view towards “non-volatile” zero leakage microcontrollers using non-volatile flip-flop and hybrid memory design for freeze mode. Finally, section V underlines scaling challenges.

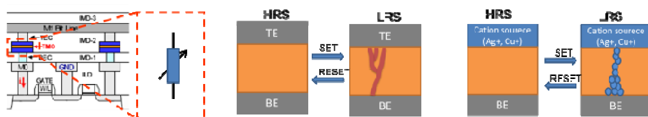
II. ReRAM Technologies

The concept of memristors was originally envisioned by Leon Chua in 1971 [4] and was demonstrated for the first time by a team of HP labs in 2008 [5]. A memristor is basically a two terminal resistor device with varying resistance. The resistance value changes according to the charge passed through the memristor over its entire history. The resistance does not change when the power is down making it nonvolatile. From design aspects, memristor is an analog device that can be used digitally where the resistance value can refer to a binary value. A low resistance is typically considered as a logical ‘1’ and a high resistance as a logical ‘0’. This device includes a large variety of oxides for ReRAM. MRAM and PCM are also considered as memristors since these devices are nonvolatile two-terminal devices with varying resistance.

a) ReRAM principle

ReRAMs are considered among the most promising solutions for future generation of low-cost embedded non-volatile memories. In the following, an overview of our recent research work on conductive-bridge memory (CBRAM) and on metal oxide resistive switching memory (OxRRAM) is given.

A ReRAM cell is generally built by a capacitor-like Metal-Insulator-Metal (MIM) structure, composed of an insulating or resistive material ‘I’ sandwiched between two electron conductors ‘M’ as illustrated in Fig. 1.a. Based on regular materials, these MIM cells can be easily integrated in the back end of line (BEOL) with conventional CMOS technology. The basic working principle is the reversible formation and disruption of a conductive filament which shunts the top and the bottom electrodes through the resistive layer. In the most studied configurations, the filament can be obtained by migration of oxygen vacancies in transition metal oxides (OXRAM) (Fig. 1.b) or by the dissolution of an active electrode (Cu or Ag) in an oxide- or chalcogenide-based electrolyte (CBRAM) (Fig. 1.c). Proper material selection, memory stack optimization and integration scheme are key points for the success of these technologies.



a) BEOL integration b) Oxide-based RAM c) CBRAM

Fig. 1. a) ReRAM BEOL integration; b) OxRAM: Chain of oxygen vacancies migration; c) CBRAM: Chain of metal atom migration

b) Conductive-Bridge RAM

Among CBRAM technologies, GeS_2-based devices have demonstrated large programming window (R_{OFF}/R_{ON}) and low power consumption [6]. Fig. 2.a shows measured current–voltage (I/V) curves for a W/GeS_2/Ag based CBRAM device. The figure shows the bipolar switching behavior through the set/reset processes under positive and negative polarity, respectively. The memory switches to the ON (SET) state when a positive bias is applied on the Ag top electrode, forming by electro-deposition an Ag-based conductive filament in the electrolyte, while a negative voltage leads to the filament dissolution and thus to the OFF (RESET) state (Fig. 2.b). The kinetic of programming operations depends on the amplitude of the applied voltage as well as the pulse width. The required SET time is about 10µs at 1.5V. As shown in Fig. 2.a for a compliance current of about 100µA an ON/OFF resistance ratio of about two/three orders of magnitude was obtained.

The memory window can be further improved by engineering of the interface. As shown in Fig. 3, by addition of a 2nm thick HfO_2 layer between the electrolyte and the W bottom electrode a memory window of about six decades can be achieved. The Ag-rich CF is formed/dissolved only in the chalcogenide layer. The role of the HfO_2 layer is to suppress the leakage current in the HRS due to residual conductive paths in the GeS_2 after the reset process.

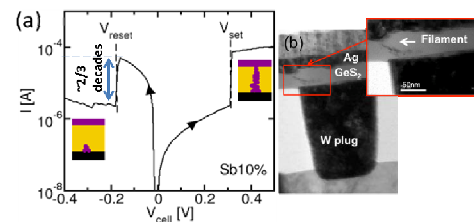


Fig. 2. (a) Typical I-V characteristics of GeS_2 CBRAM. (b) TEM cross section of a CBRAM device with GeS_2 electrolyte.

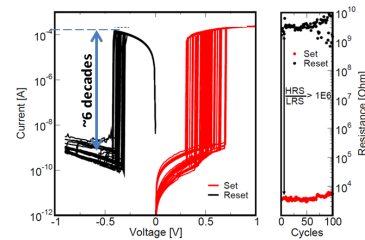


Fig. 3. DC I-V characteristics for CBRAM devices.

c) Oxide-based RAM

OxRAM technologies, such as Ti/ HfO_2 based devices, provide higher write/erase speed at the expense of a smaller memory window. Fig. 4.a shows the switching kinetics for a wide range of positive voltages of the two samples with different HfO_2 thicknesses [7]. The required SET voltage for the 5nm HfO_2 sample is ~100ns at 1V. Fig. 4.b demonstrates the extracted cell behavior up to more than 10^8 cycles for the 5nm HfO_2 sample without failure, demonstrating their potential high endurance [8]. The memory window is about 1 decade.

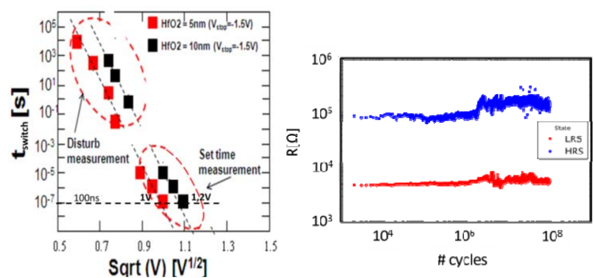


Fig. 4. (a) Exponential relationship of switching with $V^{1/2}$ for 5nm-HfO_2 and 10nm-HfO_2. (b) Resistance as a function of cycle number.

Based on the defined stack, compared to OxRAM, CBRAM brings higher off state resistance and memory window at the expense of a longer switching time for a given applied voltage.

III. TOWARDS NV-FPGA

FPGA have experienced dramatic increases in speed, size, flexibility, performance and commercial impact since the early 1990's. With increasing costs of advanced technologies, FPGAs are even more becoming a better alternative for a large number of medium-volume applications than in the past due to their non-recurring engineering cost and ease of design. However, to support reconfigurability FPGAs must use more transistors than fixed-logic ICs to perform the same function, leading to higher leakage power consumption. Consequently, FPGAs are generally not well suited for mobile and ULP embedded applications. This section addresses challenges and opportunities regarding ULP ReRAM-based FPGA design from technology optimization to design integration.

a) FPGA background

In regular island style FPGAs, the logical operations are carried out in Logic Blocks (LB), the I/Os of LBs are connected to the channels in connection boxes (CB) and the communication on different routing channels are performed in switch boxes (SB) as shown in Fig. 5. The connection box and switch box are the routing resources. The LBs are surrounded by vertical and horizontal routing channels (or tracks) which are uniform throughout the entire FPGA. The logic functionality is stored in memory inside the LBs, and the routing information is in memory of the SB and CB. Memories can occupy almost half of the total chip area in the SRAM-based FPGA landscape.

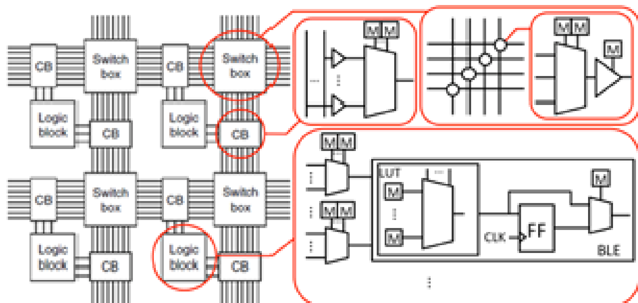


Fig. 5. Island style FPGA

Therefore, the performance characteristics of FPGAs are directly related to the memory technology used to design them due to their fundamental nature as configurable devices. They can be classified according to the type of memory used to store configuration data. Among them, SRAM-based FPGAs are extensively used because they offer high computing capacities compared to other FPGAs. They utilize SRAM for routing and programming computational functions, usually through the use of Look-Up Tables (LUT) and multiplexers. SRAM-based FPGAs are fast, but the volatile nature of SRAM requires to reload configuration data at power-up or to maintain a data retention voltage. The configuration process can require high current, while data voltage retention leads to standby-power consumption. To overpass SRAM volatility issues, Flash-based FPGAs have been proposed. All configuration and routing data are store in Flash-based switches that retain their states when the power is off. Nonetheless, the use of a hybrid CMOS-Flash technology results in higher fabrication cost and slower performance. Besides, anti-fuse-based FPGAs offer the lowest cell size and can deliver fast performance in addition to non-volatility, but they are programmable only once.

b) ReRAM-based FPGA

Considering emerging NVM technologies many new FPGA architectures recently have been proposed demonstrating significant improvements on density of integration (40%) and energy efficiency (28%) [10]. Indeed shifting the configuration memory to the top of the FEOL helps to merge the advantages of the previously mentioned FPGA memory technologies (i.e. fast reconfigurability, low standby leakage and high density integration).

The 1T2R has been the most reported configuration memory cell design, driven by its very high-density integration compared to a regular 6T SRAM bit-cell. It consists of two programmable resistors in voltage divider configuration and a shared select transistor [11]. However that resistance pair gives a severe requirement to really have a benefit in implementing this architecture. Even if the 1T-2R solution eliminates stand-by power consumption, if the high resistive state (HRS) is not sufficient, leakage current through the ReRAM can be important during run time, which in turn compromises the operating power consumption.

In [12], a novel dual layer HfO_2/GeS_2 based CBRAM device has been investigated. A record high R_{off} resistance (Fig. 6) has been achieved with a solid electrolyte consisting of a 2 nm HfO_2 layer that suppresses leakage current through a 30nm thick GeS_2 layers.

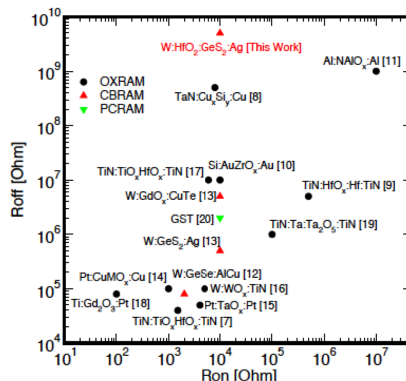


Fig. 6. Benchmark of LRS (Ron) and HRS (R_{off}) for several ReRAMs reported in the literature obtained with endurance test [11]

The 1T1R cell also suffers from unbalancing voltage conditions to set/reset the ReRAM devices due to the single select transistor. This issue can be easily overcome by replacing the select transistor with a transfer gate, as proposed in Fig. 7. The operation modes of the configuration 2T2R cell are illustrated in Fig. 7 and sum up in TABLE II. The bitline is connected to programming voltages. After the word lines (WL, WL_B) are asserted the dual X and Y lines are swing. In read

mode, X is tied to the supply voltage while Y is pulled to the ground.

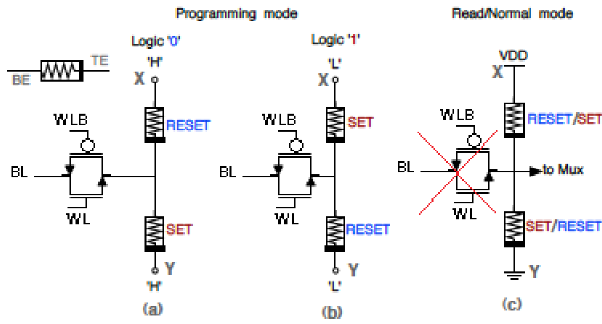


Fig. 7. Proposed circuit scheme for programming and reading of CBRAM cells in resistor-divider configuration.

TABLE II. PROGRAMMING SCHEMES FOR TOP AND BOTTOM RERAM

	Top and Bottom	
	'0'	'1'
BL: '0'	Set Bottom	Reset Top
BL: '1'	Set Top	Reset Bottom

c) Performance gains

The 2T2R cell was characterized for area and leakage during operating mode as shown in TABLE III. The obtained results are compared to a classical 6T-SRAM cell implemented in 130nm technology design. The 2T2R cell brings an area gain of /2.6 with a leakage current of 182pA at 1.5V [13] due to the HfO_2/GeS_2 technology optimization. The next sub-section explains a favorable power management strategy for using CBRAM based technology exploiting the non-volatility feature of this type of ReRAM.

TABLE III. AREA COMPARISON BETWEEN 6-T SRAM AND 2T-2R

130 nm Bulk	Cell	Area (μm^2)	Leakage (pA)	Volatile
SRAM	6T	11,28	25 [13]	Yes
CBRAM	2T/2R	4.32	182	No

d) FPGA benchmarking

In order to evaluate the overall impact of the proposed memory cell on total area, critical path delay and power consumption, the tool flow described in [14] is used. First, SRAM-based FPGA is evaluated. After that, all the SRAM cells are replaced with the proposed non-volatile memory cell. In comparison to SRAM-based FPGA, NV-FPGA has reduced area by 32%. The smaller area leads to shorter and less capacitive wires. Therefore, improvements in critical path delay and power consumption are observed by 9% and 10% accordingly. The most important feature of the proposed FPGA is the non-volatility. As described before, the ULP goal is achieved by turning off, the FPGA when not in use. Consequently, taking advantage of the non-volatility, NV-FPGA can save the leakage power, which is otherwise wasted. Based on the activity ratio between on and off times, duty cycle can be defined. As shown in Fig. 8, decreasing the duty cycle, results in increased power gains. For applications having an activity of 50%, the total power consumption can be reduced by 24% and more than 90% of power reduction is achieved for applications with 1% activity.

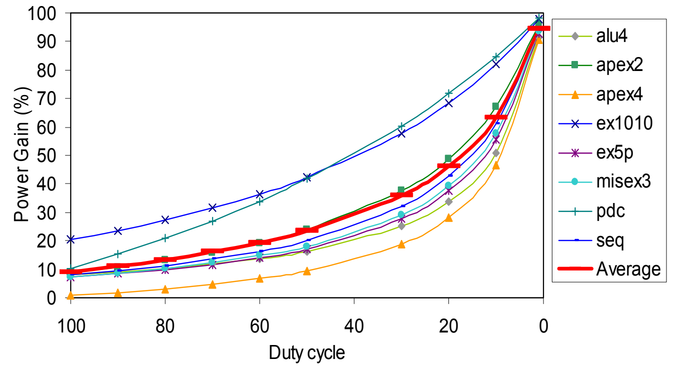


Fig. 8. Power gain according to different duty cycle values for NV-FPGA.

IV. TOWARDS ZERO LEAKAGE SYSTEMS

The previous section underlined the benefits of using ReRAM for the FPGA configuration memory. This section relates to ReRAM-based IC design toward zero standby leakage and rapid power on/off operations to extend battery life of mobile devices and ULP embedded systems.

The key idea is to design an efficient freeze state system being able to restart from the logic state when the system was powered-off. In this framework, ReRAM is employed in memory and combination logic to back up the data from the SRAM, register files down to Flip-Flops to the ReRAMs and switch the power off. This way the leakage is totally suppressed with no data loss.

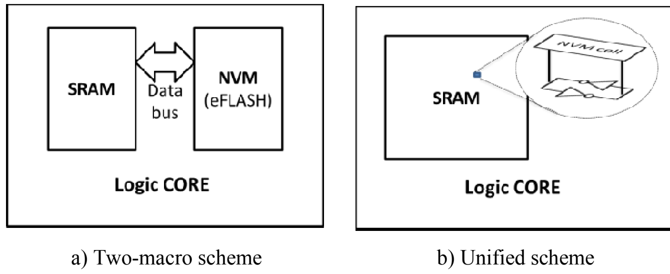
Back-up and recall of data present density, consumption and timing response time challenges. This section approaches non-volatile Flip-Flop and hybrid-SRAM design.

a) ReRAM-based SRAM bit-cell

To suppress memory standby power without a loss of data while providing storage at high speed read/write operation, on-chip non-volatile memories, such as eFlash memory, have been associated to SRAMs in low power systems. To overcome the speed and supply voltage gaps between SRAM and eFlash memories, a two-macro scheme has been required, as shown in Fig. 9.a. The main drawback of such scheme is a long store/restore time due to word-by-word access, resulting in long power on/off time exposing the circuit to data loss in event of sudden power-failure.

With emerging non-volatile technologies, the concept called unified non-volatile SRAM bit-cell (NV-SRAM) has emerged and has become an important research topic in recent years to achieve fast parallel data transfer and fast power-on/off speed. Overall, the NV-SRAM solutions integrate 6T bit-cells and stacked resistive or capacitive NVM devices within a single bit-cell, forming a direct bit-to-bit connection in vertical arrangement as depicted in Fig. 9.b. In a volatile state with an active power supply, data is held in the SRAM portion, and this data is read/write accessed as standard SRAM cell. Before powering down the supply voltage, the data in the SRAM

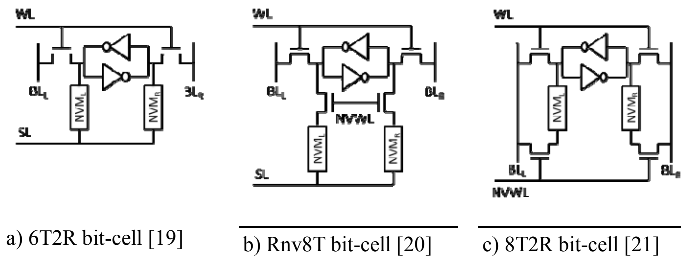
portion is stored into the NVM portion. When the circuit is powered up, the stored value is restored to the SRAM portion.



a) Two-macro scheme b) Unified scheme

Fig. 9. NV-SRAM schemes

Several emerging memristor devices have been considered in NV-SRAM satisfying more or less the SRAM requirements in terms of speed, supply voltage, stability and area due to technology constraints (voltage, current…) and limitations (switching time, endurance, reliability…). Among them, the SONOS-based cells [15] require a high store-voltage, long store-time and large area. The MRAM- and PCM-based cells [16][17] consume a high current for storing. And the Fe-capacitor-based cells [18] require minimizing the capacitor for decent write access time.



a) 6T2R bit-cell [19] b) Rnv8T bit-cell [20] c) 8T2R bit-cell [21]

Fig. 10. ReRAM-based NV-SRAM architectures

On the other hand, ReRAM-based bit-cells appear in a favorable position as ReRAM provides fast switching at low voltage and set current, limiting area overhead. Fig. 10 shows and compares three architectures. In [19], the ReRAM-6T2R (Fig. 10.a) connects NVMs to SRAM storage nodes directly achieving the simplest bit-cell solution. However, it can lead to stability issues and high leakage coming from the resistive elements introduced in the cell architecture. The leakage issue can be improved by increasing the low- and high- resistance values of ReRAM devices. To maintain the SRAM performance, additional transistors to isolate ReRAM devices from the 6T core have been integrated in [20][21]. Therefore, both 8T2R (Fig. 10.b) [20] and Rnv8T (Fig. 10.c) [21] bit-cells require an additional word-line (NVWL), as for regular 2 ports bit-cells, to deliver the store/restore signal, consuming area. In 8T2R bit-cell, to store a third source-line (SL) is required. SL can be shared overall the array or addressed row-by-row. When a NVWL is turned on, SL toggles from 0 to a high voltage to set and reset the ReRAM ($NVM_{L,R}$) devices following the value of storage nodes. In Rnv8T bit-cell, store operation is achieved in two steps. Both bit-lines (BL_L and BL_R) are first raised to a high voltage to set one NVM and then grounded to reset the complementary NVM of the selected bit-cell. In both schemes, during a restore operation, the data are recalled from the two NVM devices into the SRAM storage nodes during the system power-on period. NVWL is turned on and both bit-lines as well as SL are grounded. The difference in resistance between NVML and NVMR creates a differential current restoring the bit-cell.

Because ReRAM devices are moving toward fast switching time and low switching current, those solutions are very promising to suppress leakage power consumption in standby/idle period with fast wake-up time. It overcomes the two-macro scheme high data store/restore energy consumption and wake-up time limitations, in particular for short standby/idle period-based applications.

b) ReRAM-based Flip-Flop

For saving and restoring the state of sequential circuits during the power-down mode shadow or balloon latches are commonly employed. Typically, it requires ten extra transistors, to the Flip-Flop, increasing the transistor count from 16 to 26 [22]. It also leads to an increase in delay through the latch and its active power, because of the extra transistors connecting the balloon latch to the Flip-Flop.

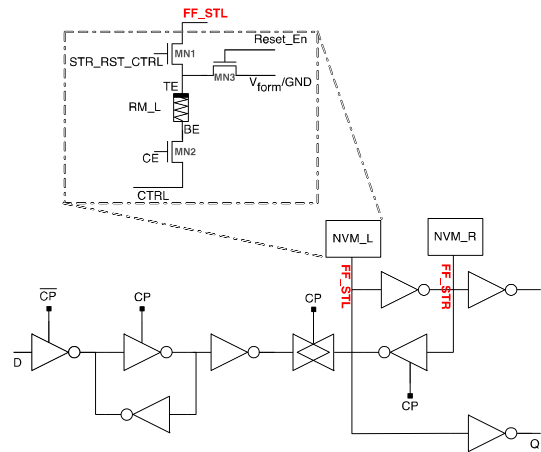


Fig. 11. An example of non-volatile flip-flop circuit for introducing freeze mode or context saving in need based computing systems in Internet of Things

Following the spirit of NV-SRAM, Fig. 9 gives an example of a ReRAM-based non-volatile Flip-Flop [23]. The NVM_L and NVM_R blocks are hooked up to the slave part of a standard master-slave Flip-Flop. Depending on the state of the logic the control, transistors MN1, MN2 and MN3 are used to store/restore the logic to/from the non-volatile ReRAMs. The advantage of using this approach is that one can still employ these design topologies at the optimum best during normal mode of operation by disabling the non-volatile blocks. However, when encountered with the need to transit to sleep mode the non-volatile block is enabled. Such sleep modes using ReRAMs unlike the traditional balloon or retention flops with high-V_t transistors can ensure zero static power dissipation. The device increasing count is 6 transistors and 2 stacked ReRAMs making it competitive with standard balloon latch.

ReRAM-based NV-SRAM and NV-Flip-Flop unified non-volatility zero standby leakage and rapid power on/off operations.

V. SCALING CHALLENGES

Design solutions for ULP embedded systems are mainly implemented using mature CMOS technology nodes due to lower leakage currents and higher reliability. As most of the reported results on ReRAM are obtained using over-130nm nodes, it is evident that co-integration of CMOS and ReRAM technologies for these purposes is straightforward from design point of view. On the other hand, in mobile devices design the usage of most advanced technology nodes is assumed and co-integration with ReRAM encounters design issues that need to be addressed.

CMOS devices scaling is followed by reducing of nominal supply voltage, as well as maximum pin-to-pin voltage that prevents from oxide breakdown and provides reliable operation. Circuits in sub-100nm nodes operate at 1V and lower. In case of OxRAM devices, scaling of oxide thickness will potentially lead to reducing the forming voltage [1]. However, reported ReRAM operating voltages remain above the CMOS range (1V - 2.5V). Moreover, high performance systems will demand fast switching behavior which is feasible with higher voltages according to inverse relationship between set/reset switching time and applied voltage (Fig. 2).

Consequently, in order to merge low and high voltage technologies it is necessary to implement design techniques to overcome that discrepancy (e.g. level-shifters). Also, a CMOS circuitry that reliably tolerates a high supply voltage and has all transistors working in safe operating region must be implemented. One solution for high-voltage tolerant transistors is the use of thick gate-oxide devices in critical parts of the circuit which might not be easy to co-integrate with thin oxide digital transistors. The second approach includes alternative circuit topologies – transistor stacking with a bias voltage that provides limited voltages across the terminals of every cascade transistor. Both solutions come at the cost of a degraded performance and increased area.

Another challenge of ReRAM technology is both spatial (device to device) and temporal (cycle to cycle) variability. Current-based monitoring design solutions have already been proposed for high capacity memories. It can be expected that it will be one of major research topic in the coming up years.

VI. CONCLUSION

ReRAM technology appears a prime candidate to save energy in mobile devices and ULP embedded systems. It enables advanced power management and freeze mode capabilities with fast parallel data transfer and fast power-on/off speed. High speed write/erase operation, scalability and feasibility of BEOL integration have been reported for both CBRAM and OxRAM technologies. Regarding IC design, in this paper two representative applications have been approached. The high R_{off} state and R_{off}/R_{on} ratio of CBRAM technology enables to achieve low leakage long retention time 2T2R cell to achieve dense memory configuration and solve FPGA leakage issue. On the other hand, the lower voltage operation of OxRAM technologies enable NV-SRAM and NV-Flip-Flop design, unifying non-volatility, zero standby leakage, and rapid power on/off operations for mobile devices and ULP embedded systems.

However, the challenges to solve before the adoption of ReRAM by industry are numerous. Among them, spatial and temporal variability have to be address to achieve robust design. Addressing scaling, sub-32nm technologies open new paradigms. Research on forming-free devices and reliable design solutions has to be pursued to face up reliability issues caused by the voltage gap between CMOS technology and ReRAM.

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