Magnetic memories: From DRAM replacement to ultra low power logic chips

G. Prenat, G. Di Pendina, C. Layer, O. Goncalves, K. Jaber, B. Dieny, R. Sousa, I.L. Prejbeanu, J.P. Nozieres
Spintec
17, Rue des Martyrs
38054 Grenoble Cedex, France

Abstract— **The recent advent of spin transfer torque (STT) has shed a new light on MRAM with the promises of much improved performances and greater scalability to very advanced technology nodes. As a result, MRAM is now viewed as a credible solution for stand-alone and embedded applications where the combination of non-volatility, speed and endurance is key.**

Whereas the technology is nearing maturity for DRAM replacement, with the exception of process scaling to sub-20nm which remains a challenge, circuit designers are now actively looking at SoCs where MRAM could bring in better performance and lower power consumption in data intensive applications as well as instant-on capability in mobile applications.

In this paper we present a review of the MRAM technology and a methodology for ASIC design using a custom full digital hybrid CMOS/Magnetic Process Design Kit. We finish by a few examples showing that magnetic memories can be efficiently integrated in logic designs, for both safety and low power purposes.

Keywords—spin transfer torque, MRAM, hybrid CMOS

978-3-9815370-2-4/DATE14/©2014 EDAA