III-V Semiconductor Nanowires for Future Devices

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***Abstract*— The monolithic integration of III-V nanowires on silicon by direct epitaxial growth enables new possibilities for the design and fabrication of electronic as well as optoelectronic devices. We demonstrate a new growth technique to directly integrate III–V semiconducting nanowires on silicon using selective area epitaxy within a nanotube template. Thus we achieve small diameter nanowires, controlled doping profiles and sharp heterojunctions essential for future device applications. We experimentally demonstrate vertical tunnel diodes and gate-all-around tunnel FETs based on InAs–Si nanowire heterojunctions. The results indicate the benefits of the InAs–Si material system combining the possibility of achieving high I_{on} with high I_{on}/I_{off} ratio.**

Keywords— Tunnel FETs, Esaki diodes, nanowires, III-V semiconductors

For many decades, the performance improvement of microelectronic circuits and devices has been based on continuously scaling down the size of Si MOSFET transistors. As this type of conventional scaling reaches the end, innovative device architectures, novel materials and new device concepts are required for continuous enhancement of performance. Bottom-up grown semiconducting nanowires are very attractive for direct integration of III-V materials on Si thus opening up new possibilities for the design and fabrication of electronic as well as optoelectronic devices. In particular, the cylindrical geometry of the nanowire provides the most ideal device structure for ultimately scaled field-effect transistors (FETs) from an electrostatics perspective. Furthermore, the possibility of combining materials with high lattice mismatch in axial heterostructures makes them a first choice material for tunnel FETs (TFETs) [1]. TFETs are being considered today the most promising steep slope devices for low power applications, being able to reach a subthreshold swing S of below 60 mV/dec. at room temperature [1].

In order to truly become a competitive technology it is important to integrate the III-V materials onto the established Si platform. Major challenges hereby are the occurrence of anti-phase boundaries, cracks and dislocations in the III-V films. For the integration of III-V materials directly on silicon we have developed a new approach in which III-V homo- as well as heteroepitaxial nanowires are selectively grown using metal-organic chemical vapor deposition (MOCVD) within nanotube templates [2]. Hereby the morphology of the nanowire is defined by the shape of the template as shown in Fig. 1. To demonstrate this technique we have grown single-crystalline In(Ga)As wires on Si as well as InAs–InSb axial heterostructures within the template as shown in Fig. 1b), c). The nanowire heterointerface achieved is very sharp and confined within 5–6 atomic planes. Compared to commonly used metal- or self-catalyzed nanowire growth processes the template approach does not suffer from the often observed intermixing of (hetero-) interfaces and non-intentional core-shell formation. Hence the proposed growth of device layers within a nanotube template opens up the possibility for a monolithic integration of III–V material-based electronic and optoelectronic nano-devices on silicon.

In terms of devices, our main interest is on tunnel devices, Esaki diodes as well as TFETs. For the implementation of TFETs we investigate the InAs-Si system because the small effective bandgap of the heterojunction promises high tunnel currents at low voltage operation, and the larger bandgap of Si in the channel assures a high I_{on}/I_{off} ratio. To achieve high performing tunnel devices the control of doping profiles, defect-free sharp hetero-junctions, small diameter nanowires and optimized gate-stacks with low interface state density and small equivalent oxide thickness are essential.

The control of doping, we have thoroughly studied for n-type doping of InAs nanowires. The carrier concentration and the mobility are extracted by a combination of 4-point probe characterization, measurements of the Seebeck coefficient and InAs homojunction diodes including TCAD simulations [3].

We have fabricated and characterized Esaki tunnel diodes and TFETs [4] based on InAs-Si heterostructure nanowires. The reverse-bias current in an Esaki tunnel diode can be considered as the upper limit for the current output of a TFET. Recently, we demonstrated high quality n-InAs−p-Si Esaki tunnel diodes as indicated by the negative differential resistance with a peak-to-valley current ratio of 2.44 and record high tunnel currents of up to 6 MA/cm^3 at 0.5 V reverse bias ($N_D^{InAs} = 5{\cdot}10^{19}$ cm^{-3} and $N_A^{Si} = 1.2{\cdot}10^{20}$ cm^{-3}), see Fig. 2. In addition, the electrical characterization of InAs-Si vertical nanowire TFETs as shown in Fig. 3 will be discussed.

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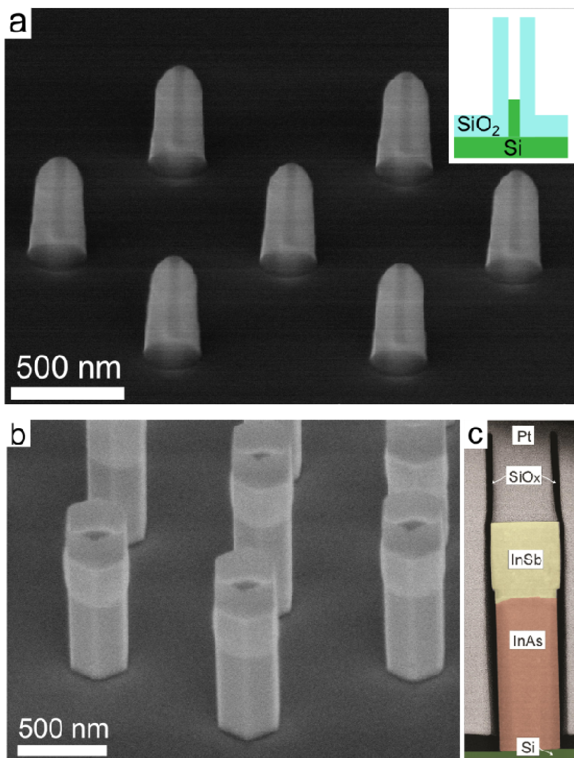

Fig. 1: (a) SEM image of SiO_2 nanotube templates, ready for III-V growth. The inset shows a schematic image of a single SiO_2 nanotube template. (b) SEM overview and (c) false-colored TEM image of axial InAs/InSb heterostructure nanowires grown within templates directly on the Si(111) substrate.

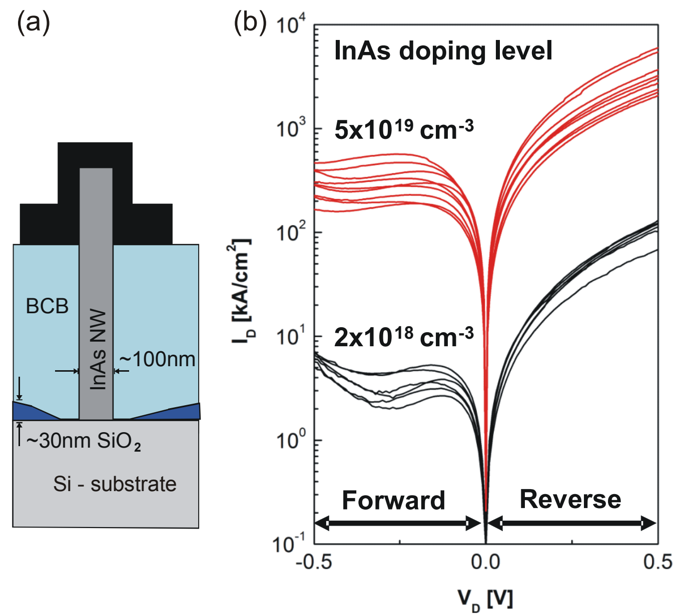

Fig. 2: (a) Schematic of the InAs–Si heterostructure tunnel diode. The InAs nanowire diameter is in the range of 100 nm. (b) Current density vs voltage of nanowire diodes as sketched in (a). The Si p-doping level is $N_A = 1.2 \cdot 10^{20}$ cm^{-3} and the InAs n-doping level is varied as indicated.

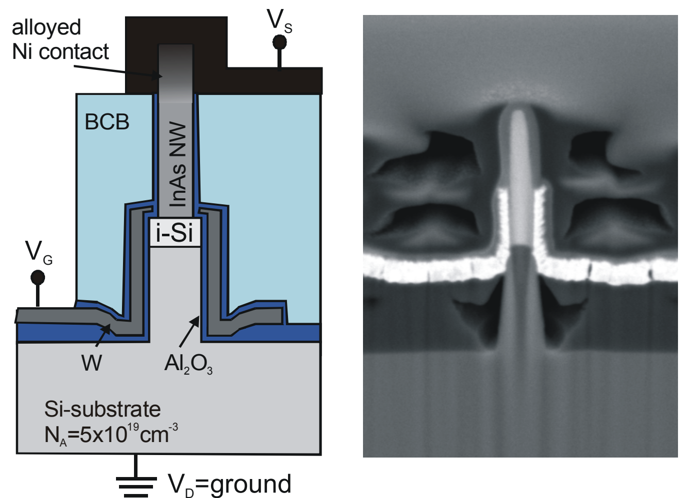

Fig. 3: Left, schematic cross-section of a vertical InAs–Si heterostructure nanowire TFET. Right, scanning electron micrograph showing the cross-section of a fabricated InAs–Si TFET. The InAs nanowire has a diameter of 100 nm, and the undoped Si channel on top of the p-type substrate is 150 nm long.