Brain-Inspired Computing with Spin Torque Devices

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Abstract: In this paper we discuss the potential of emerging spin-torque devices for computing applications. Recent proposals for spin-based computing schemes may be differentiated as 'all-spin' vs. hybrid, programmable vs. fixed, and, Boolean vs. non-Boolean. All-spin logic-styles may offer high area-density due to small form-factor of nano-magnetic devices. However, circuit and system-level design techniques need to be explored that leaverage the specific spin-device characterisitcs to achieve energy-efficiency, performance and reliability comparable to those of CMOS. The non-volatility of nano-magnets can be exploited in the design of energy and area-efficient programmable logic. In such logic-styles, spin-devices may play the dual-role of computing as well as memory-elements that provide field-programmability. Spin-based threshold logic design is presented as an example. Emerging spintronic phenomena may lead to ultra-low-voltage, current-mode, spin-torque switches that can offer attractive computing capabilities, beyond digital switches. Such devices may be suitable for non-Boolean data-processing applications which involve analog processing. Integration of such spin-torque devices with charge-based devices like CMOS and resistive memory can lead to highly energy-efficient information processing hardware for applicatons like pattern-matching, neuromorphic-computing, image-processing and data-conversion. Finally, we discuss the possibility of using coupled spin-torque nano oscillators for low-power non-Boolean computing.

Keywords: spin, logic, low power, threshold logic, analog, neural networks, non-Boolean, programmable logic array, coupled spin torque nano oscillators

1. Boolean Logic with Spin-Torque Devices:

Recent experiments on spin-torque in device structures like lateral spin valve (LSV) [1], (fig. 1a), domain wall magnets (DWM) [2], and magnetic tunnel junctions; have opened new avenues for spin based computation. Several digital logic schemes have been proposed based on such devices. Such proposals may be classified as programmable or fixed logic styles.

1.1 Fixed Logic Styles using Spin-Torque Switches

All Spin Logic (ASL) proposed in [3], employs cascaded LSV's interacting through spin-torque, to realize logic gates and larger blocks like compact full adders [4], based on spin majority evaluation (fig. 1). The key feature of ASL is its compactness; however, energy inefficiency resulting from relatively larger magnet-switching delay can be identified as the down-side of it. In a standard ASL design, achieving 500MHz operation for an 8x8 multiplier would require ~60ps switching-speed for individual magnets (of size $30 \times 15 \times 1.5 nm^3$), leading to untenably high current-levels. This results in large static power in the ASL device (fig. 2). Non-volatility of nano-magnets can be exploited by introducing 2-phase pipelining, which would result in high-throughput for a given switching current, thereby mitigating the requirement of high-switching speed for individual magnets. Overhead due to clocking transistors can be minimized by the use of 'leaky' transistors with relatively low *ON*-resistance, without incurring significant loss in robustness [5].

The non-local STT employed in ASL decouples the biasing charge-current path from the spin-current path along which computation is performed (fig. 1). Common charge current channels can therefore be shared by multiple ASL layers in a vertical stack,

leading to a high-density 3-D spin logic design. In such a design, a single CMOS substrate can be used to supply 2-phase clock to a large number of low-resistance, metallic ASL stacks, leading to high energy efficiency along with very high integration-density [5].
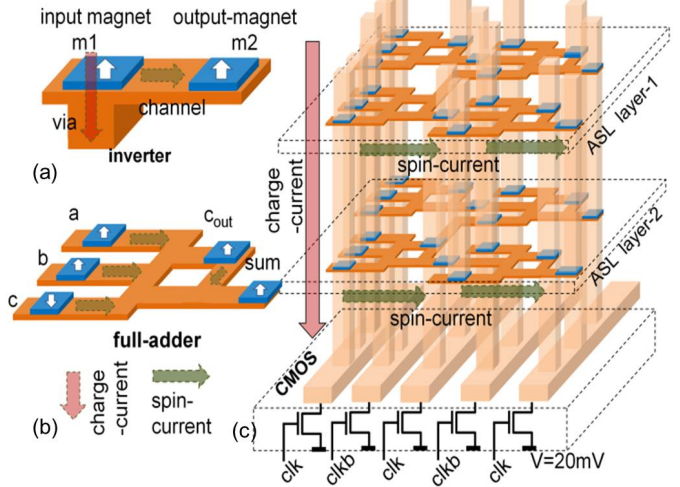

Fig. 1 (a) ASL inverter, (b) ASL full adder, (c) 3-D integration scheme for ASL with shared transistors for pipelining
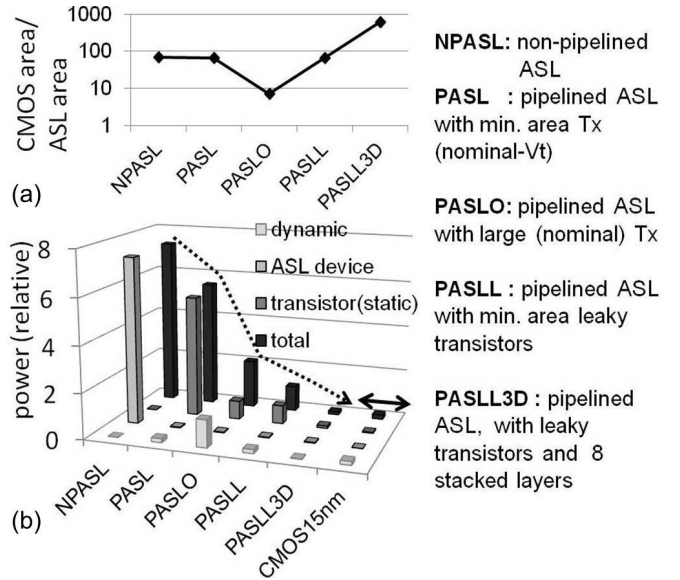

Fig. 2 (a) Area comparison of proposed ASL design with CMOS, showing the possiblity of 3 order of magnitude higher logic density, (b) different components of power dissipation in pipelined, 3D-ASL [10, 11] and their comparison with standard ASL and 15nm CMOS.

Optimized 2-phase pipelining and 3-D stacking can lead to two orders of magnitude lower power consumption as compared to a non-pipelined ASL, for a given set of device parameters. Notably, the proposed design-scheme can achieve power consumption and performance comparable to CMOS, provided desirable device parameters (like efficient magnet-channel interface, low contact resistances and high-spin diffusion length for channel) are achieved in the future [6]. The most attractive feature of 3D ASL is evidently the ultra-high area density. The prospects of achieving ~1000x higher

logic density as compared to CMOS may be a motivating factor for the on-going research and experiments in this field.

Recent experiments have achieved domain wall (DW) motion with relatively small current density (10^7 A/cm^2) in magnetic nano-strips with perpendicular magnetic anisotropy (PMA) [7, 8]. Device scaling and the use of emerging spin-orbital coupling phenomena [8], can further reduce the required current density for DW-motion. Such techniques can be exploited to design ultra-low voltage logic schemes based on nano-scale domain-wall switches [9, 10]. Owing to non-volatility of DWM based logic cells, fine-grained pipelining can be achieved, leading to high throughput along with low computation energy for low and medium frequency data processing.

1.2. Programmable Logic Design using Spin Devices

Non-volatile spin-torque switches can be used in designing configurable logic blocks [11-13]. Such circuits can possibly provide enhanced scalability and energy-efficiency resulting from reduced-leakage of the spin-based memory elements. Exploiting these benefits of spin-torque devices, hybrid logic circuits like magnetic full adders [12], non-volatile flip-flops [13], and memory-cells for hybrid FPGAs have been proposed [14].

Spin devices can be attractive for logic schemes that involve direct use of memory elements for computing. One such scheme is threshold logic [15].The operation of a threshold logic gate (TLG) involves summation of weighted inputs, followed by a threshold operation as given in eq.1:

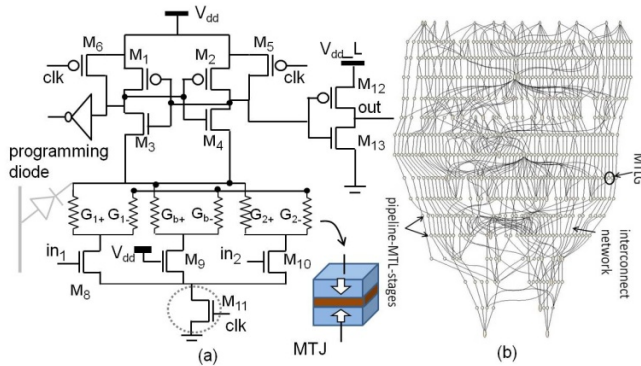$$Y=sign\left(\sum In_i\,W_i + b_i\right) \qquad (1)$$

Fig. 3 (a) Magneto-resistive threshold logic gate (MTLG) with two fan-ins, (b) Pipelined threshold logic network using MTLG

Table-1 Performance Comparison: MTL vs. CMOS-LUT

ISCAS-85 benchmark	# input	# output	delay /throughput (ns)		Energy (fJ)		% reduction	
			LUT	RTL	LUT	RTL	energy	energy-delay
c432	36	7	10.1	0.5	17362.56	480	97.2	99.86
c499	41	32	8.18	0.5	33795.57	940	94.5	99.83
c880	60	26	8.4	0.5	26394.41	970	96.3	99.78
c1355	41	32	9.95	0.5	56284.24	1480	97.4	99.87
c1908	33	25	11.55	0.5	56930.13	1200	97.89	99.91

Here, In_i, W_i and b_i are the inputs, weights and the thresholds respectively. A network of TLGs with configurable W_i and b_i can be realized with the help of spin-torque memory elements [16]. A spin-CMOS hybrid Magneto-resistive TLG (MTLG) is shown in fig. 3a. It uses magnetic tunnel junctions (MTJ) to implement the programmable input weights and the bias, connected to the input transistors (M_8, M_{10}) and a dynamic CMOS latch for the thresholding operation. Such a hybrid MTLG can be used to design pipelined, high-performance and energy-efficient TLG-array as shown in fig. 3b [16]. Table-1 compares the performance of MTLG with 4-input

LUTs showing the possibility of ~100x improvement in energy-delay product as compared to CMOS-based programmable logic.

An all-spin MTLG can also be designed that uses spin-torque switches for thresholding as well as programmable resistive weights (fig. 4). Such a spin-torque thresholding switch is shown in fig. 4a. It constitutes of a thin and short (20x60x2 nm^3) nano-magnet domain d_2 connecting two anti-parallel magnets of fixed polarity, d_1 and d_3. The domain d_1 forms the input port, whereas, d_3 is grounded. Spin-polarity of the domain d_2 can be written parallel to d_1 or $d3$ by injecting a small current (~1μA) along it, depending upon the direction current flow [17-19]. Thus, the domain wall switch (DWS) acts as a compact, fast and low-voltage current-comparator. MTJ-based detection port is used for reading the-spin polarity of the free-domain (fig. 4). CMOS-inverter can be used to sense the state of the DWS and communicate it to the fan-out gates [20]. An all-spin MTLG can be more area efficient as compared to dynamic MTLG in fig. 3. For achieving high energy efficiency, it needs the application of small input voltages (~50mV) in order to minimize the static power consumption due to direct current-paths.
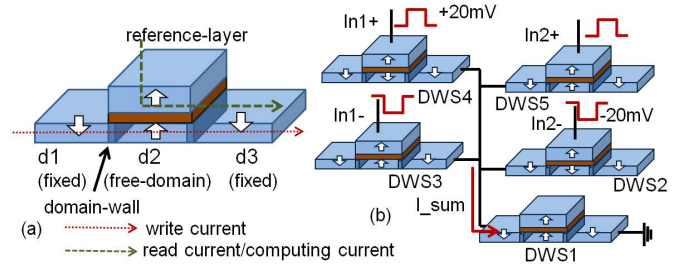

Fig. 4 (a) Domain-wall switch (DWS), (b) All-spin MTLG using spin-torque based DWS: DWS1 is the thresholding device, while DWS2-DWS4 are acting as programmable weights.

2. Spin-Torque Devices for Energy Efficient Non-Boolean Computing

Most of the spin based computation schemes (both hybrid as well as 'all-spin') proposed so far, have been centered on modeling digital logic gates using these devices. A wider perspective on the application of spin-torque devices, however, would involve, not only exploring possible combination of spin and charge devices but, searching for computation-models which can derive maximum benefits from such heterogeneous integration.

Ultra low voltage, current-mode operation of magneto-metallic devices like LSV's and domain-wall magnets (DWM) can be used to realize analog summation/integration and thresholding operations with the help of appropriate circuits [17-22], [23,24]. Such device-circuit co-design can lead to ultra-low power non-Boolean computation circuits. Examples of such device-circuit design are given in the following sub-sections.

2.1 Non-Boolean computing using spin-based circuits

Low current threshold for domain wall motion in PMA nano-magnet strips clubbed with the application of spin-orbital coupling [8], can be exploited to model a spin-torque thresholding device or 'neuron' as shown in fig 4a [17, 18]. Such a low-voltage current-mode switches can be used to for computing current-mode analog summation and thresholding operations, required in non-Boolean computing circuits like neural networks.

Fig. 5 shows neuromorphic circuit model using the DWN device described above. This example shows a 'receiving' neuron connected to two 'transmitting' neurons through synapses. A synapse is defined in terms of the magnitude and the sign of its connectivity strength or 'weight'. In the spin-based neural circuit, a dynamic CMOS latch senses the state of the DWN-MTJ while injecting only a small transient current into the detection terminal. The latch drives transistors operating in deep triode region (biased across a small drain to source voltage, ΔV~50mV), which transmit synapse-currents to all

the fan-out neurons. The transistors corresponding to the positive weights, effectively source current to the receiving neurons, whereas the transistors corresponding to the negative weights act as drains. In this scheme, the spin neurons facilitate ultra-low voltage biasing of the static current-path, leading to reduced static-power consumption. Moreover, the thresholding operation of the spin- neurons can be much more energy-efficient as compared to that of conventional analog CMOS circuits [17].
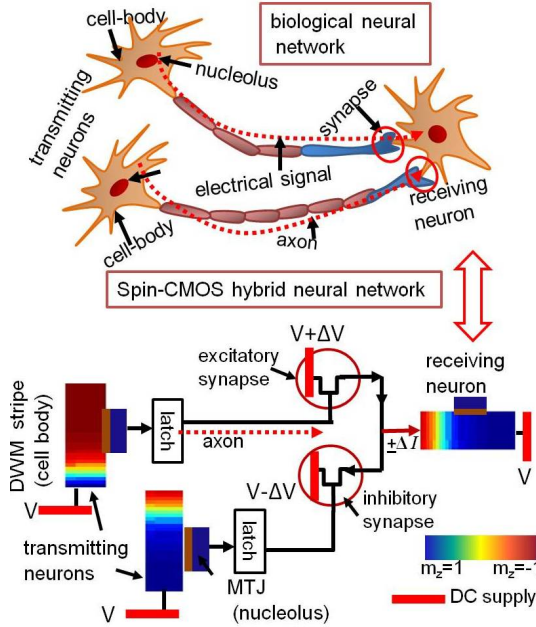

Fig. 5 Emulation of neural network using spin-CMOS hybrid circuit: In each neuron, the MTJ acts as the firing site, i.e., the nucleolus; DWM strip can be compared to cell body and its spin polarization state is analogous to electrochemical potential in the neuron cell body which affects 'firing', the CMOS detection unit can be compared to axon that transmits electrical signal to the receiving neuron, and finally a weighted transistor acts as synapse, as it determines the amount of current injected into a receiving neuron.
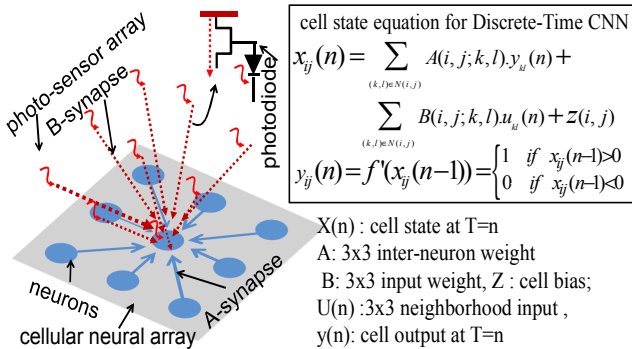

Fig. 6. 3x3 neighborhood architecture of CNN and equation for neuron's state: Current from each photosensor u_{ij}, is transmitted to 3x3 neighbors through type-B synapses implemented using weighted transistors, whereas, inter-neruron connection is determined by type-A synapses.

Design Example: The circuit concept described above can be employed in the design of different classes of neuromorphic architectures. Using this technique, we presented the design of an image processing architecture based on cellular neural network (CNN) in [24] (fig. 6). Each neuron in a CNN has two kinds of synaptic connections, type-A and type-B (fig. 6). Through the type-A synapses, a neuron receives the outputs y_{ij}, of its eight nearest neighbors and its own state as a feedback. Through type-B synapses,

it receives the external signals, u_{ij}, (in this work, photo-sensor current from neighboring pixels) from 3x3 surrounding input points. The choice of the two sets of weights determines the input-output relation for the whole array and hence the image processing application. The recursive evaluation of neurons in CNN essentially involves weighted sum of these two sets of synaptic inputs, followed by a sign operation (fig. 6). In the on-sensor image processing architecture presented in [24], A and B-type synapse weights were realized using weighted triode source transistors, as described above. Note that, in this scheme, the B-synapse transistors receive analog-mode photo-sensor voltage at their gate, and, in turn, provide proportional currents to the neurons. On the other hand the A-synapse transistors receive binary voltage levels at their gates, corresponding to the source neurons' output-state.

Table-I CMOS vs. spin based feature extraction IC

Ref	CMOS Tech	E(CMOS) /E(spin)
[23]	0.35μ	253
[24]	0.35μ	560
[25]	0.25μ	470

E= (total power) / (S²x#Pixels x Fps)

Table-II CMOS vs. spin based ADC

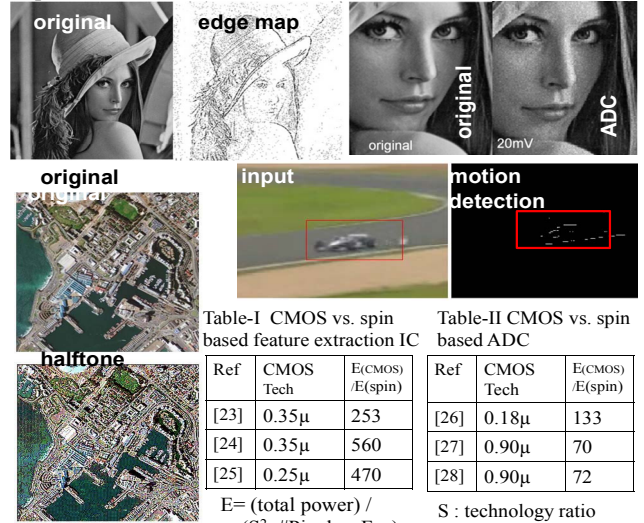| Ref	CMOS Tech	E(CMOS) /E(spin)
[26]	0.18μ	133
[27]	0.90μ	70
[28]	0.90μ	72

S : technology ratio
fps : frames/sec

Fig. 7 Simulation results for different image processing applications: edge-extraction , motion-detection , halftoning and digitization; Table 1, 2 compares the energy per computation frame, per-pixel, of the propsoed CNN design with some recent CMOS designs for edge extraction and ADC.

Simulation results for some common image processing applications like edge-extraction, motion-detection, half-toning and digitization (fig. 7), using the spin based CNN, showed ~100x lower computation energy, as compared to state of art mixed-signal CMOS designs. As mentioned earlier, the main advantage comes from ultra low voltage, pulsed operation of spin neurons that are applied to analog computation. While subthreshold analog circuits operating at few 100mV can achieve low power [17, 24], but the corresponding switching speed is generally less than 1MHz. The spin-neurons on the other hand, while operating at ~50mV can still provide ~1GHz processing speed.

2.2 Ultra low energy non-Boolean computing using spin neurons and resistive memory
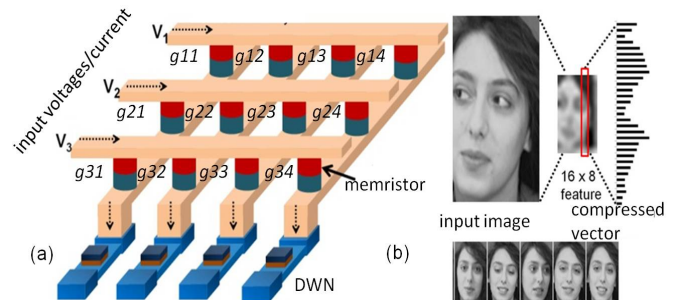

Fig. 8 (a)RCN interfaced with DWN, (b) generating of compressed vector representation of stored and input images [25]

In recent years several device-technologies have been proposed for fabricating nano-scale programmable resistive elements, generally categorized under the term 'memristor' [25, 26]. Of special interest are those which are amenable to integration with state of art CMOS technology, like memristors based on Ag-Si filaments [26]. Multi-level write techniques for memristors in crossbar arrays have been proposed and demonstrated in literature that can achieve precision up to 0.3% (equivalent to 8-bits) [26]. Such devices can be integrated into metallic crossbars to obtain high density resistive crossbar networks (RCN). The Resistive-Crossbar Network (RCN) technology has led to interesting possibilities of combining memory with computation. RCN can be highly suitable for non-Boolean computing applications that involve pattern-matching. For instance, memristors can be exploited as compact programmable weights needed in neural circuits, discussed earlier.

The RCN shown in fig. 8 constitutes of memristors (Ag-Si) with conductivity g_{ij}, interconnecting two sets of metal-bars (i_{th} horizontal bar and j_{th} in-plane bar). The horizontal bars shown in the figure receive input currents/voltages. Assuming the outward ends of the in-plane bars grounded, the current coming out of the j_{th} in-plane bar can be visualized as the dot product of the inputs V_i and the cross-bar conductance values g_{ij} (Fig. 8). An RCN can therefore, directly evaluate the weighted summation of analog inputs and hence provides an efficient model for synapse or weighted input connections for a neural network. Each of the in-plane bars in Fig. 8 therefore can be input to an analog unit that can provide the essential neural functionality of thresholding. Several design schemes for neuromorphic hardware based on RCN have been proposed in literature that employ analog CMOS circuits to perform the thresholding task [18, 19]. As mentioned earlier, such circuits, employing current-mirrors and analog operational amplifiers (OPAMPs) lead to large static power consumption.

The critical neural functionality needed in RCN based designs can be provided by the magneto-metallic spin neurons at ultra-low energy cost. Fig. 8 depicts DWN neurons interfaced with an RCN. Since the DWN neurons are fully metallic and do not need any biasing circuitry, they facilitate the application of ultra-low input voltages. Moreover, they can provide the high-speed current-mode thresholding operation without dissipating any additional static power. Preliminary simulation results show that owing to these two factors, the spin neurons can potentially achieve more than two order of magnitude lower computation energy as compared to analog CMOS neurons. Hence, the proposed technique can facilitate the design of ultra-low energy and high performance non-Boolean computing blocks with RCN.

A design example for analog associative computing was presented in [18]. In this work, compressed representation of different face-images were stored along the in-plane columns of the RCN (fig. 8), while the dot-product between an analog input (applied to the horizontal bars) vector and the conductance values were used for detecting the best match for an input face-image. The winner detection was done with the help of spin neurons. The spin-neurons acting as compact current-mode comparators can facilitate energy-efficient successive approximation based analog to digital conversion, following which a compact and low power digital WTA can detect the highest value. Moreover, application of spin-neurons facilitates the use of ultra low input voltage levels (~50mV) in order to reduce the static power consumption in the RCN itself. Thus, ultra-low voltage, high-speed analog computing with RCN using spin neurons can achieve much higher energy-efficiency as compared to analog-CMOS circuits applied for the same task (~100X improvement). Results showed more than three order of magnitude lower computation-energy as compared to a 45nm digital CMOS design.

The basic associative unit discussed above, can be extended to a more generic architecture. The proposed design scheme can be applicable to a wide class of non-Boolean computing architectures that also include different categories of neural networks. Different spin-devices can also be used to obtain different network

functionality. For, instance, long-channel DWN devices can be applicable to spiking neural networks [27].

3. Spin-Torque Nano Oscillators for Non-Boolean Computing

A vertical spin valve constitutes of two ferromagnetic layers separated by a thin non-magnetic metal-spacer (Giant Magneto Resistance-GMR device) or a tunneling-oxide (Tunneling Magneto Resistance-TMR device). The magnetization of one of the layers is fixed (fixed or pinned layer). Magnetization of the other layer (free layer) can be switched parallel (*P*-state) or anti-parallel (*AP*-state) to the fixed-layer by injecting charge current along the two terminal device, depending upon the direction of current flow [33]. The device offers higher resistance in *AP* state (R_{AP}) compared to that of the *P* state (R_P).

An external magnetic field can be used to induce steady state precession in the spin polarity of the free layer, biased with a constant charge current [34,35]. Under such a condition, the spin-torque due to the charge current balances the inherent damping force in the free-layer, preventing its bi-stable switching transition (notably, free-layer oscillations can be effected by other methods, like the use of tilted or perpendicularly polarized fixed-layer [36]). The resistance of the spin valve can be expressed as a function of relative angle between the spin-polarization of the two ferromagnetic layers θ,

$$R = \left(\frac{R_P + R_{AP}}{2}\right) + \left(\frac{R_P - R_{AP}}{2}\right)\cos\theta \qquad (2)$$

An output oscillating voltage can be obtained by passing a constant read current through the device. The absolute resistance of the TMR device is much higher than that of the GMR device. GMR based STNO, being fully metallic, can be operated with very low voltage (~10 mV). However the sensed signal amplitude is very low, which requires complex sense-amplifier circuitry, leading to large power consumption [33]. On the other hand, though the TMR based STNO can provide large amplitude output signals, due to the high-resistance tunnel junction, it requires a large bias voltage, leading to energy inefficiency at the device-level.
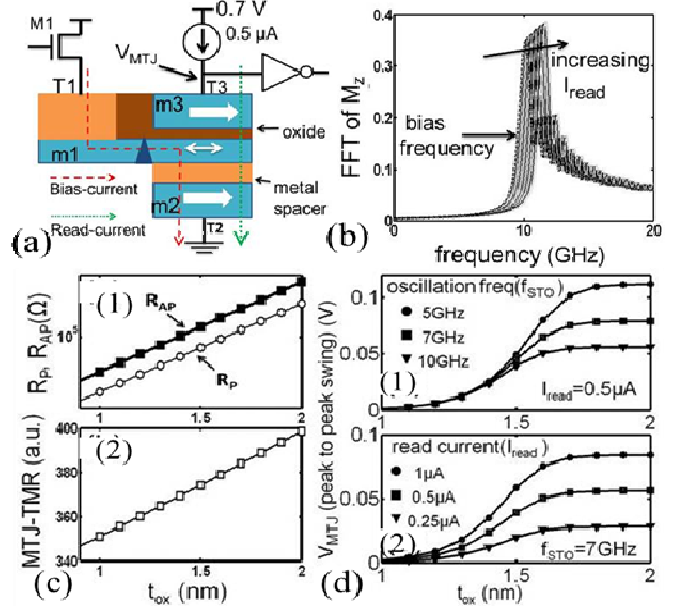

Fig. 9 (a) Proposed DP-STNO and CMOS interface for biasing and sensing (b) Fast-Fourier-Transform (FFT) of magnetization oscillation showing frequency disturb due to read current. (c) 1. MTJ Resistance vs. t_{ox}, 2. MTJ TMR vs. t_{ox} (d) V_{MTJ} (p-p) saturates for higher t_{ox} due to low pas filtering effect

Device dynamics of frequency coupled STNOs can be attractive for non-Boolean computing [33,34], however, it is essential to explore

methods to achieve low computing energy per device in order to facilitate large-scale integration of STNOs for practical data-processing applications.

We propose a Dual-Pillar STNO (DP-STNO) with decoupled bias and read paths [37]. The bias path employs a low resistance, magneto-metallic GMR interface that allows the application of low bias-voltage, while a high-resistance TMR interface is used to obtain a large-swing output-signal with a small sensing current. We present device-circuit co-simulation results for the proposed device for edge-detection, as a benchmark non-Boolean computing application and compare its performance with standard 2-terminal STNOs.

Fig 9a shows the schematic diagram of the Dual Pillar Spin Torque Nano Oscillator (DP-STNO) along with biasing and sensing circuit. The DP-STNO employs an extended 'free' magnetic layer m_1, with input terminal T_1. It forms a GMR interface with a fixed magnet m_2 and a TMR interface with another fixed magnet m_3. The input bias current is applied between terminals T_1 and T_2 using a transistor-M_1 (dashed line in Fig 9a). Owing to the small resistance of the magneto-metallic GMR interface (between terminals T_1 and T_2), the bias-current can be provided by the transistor-M_1 operating across a small drain-to-source voltage. This current induces spin-torque on the portion of free layer in contact with GMR interface and sets its magnetization into sustained oscillations (under conditions mentioned earlier).

The oscillations can be sensed by injecting a small read current into the TMR junction formed between the magnets m_1 and m_3 (dotted line in Fig 9a). It is desirable to minimize the read-current in order to minimize the power-consumption for sensing and also to avoid shift in the oscillation-frequency from the desired value (Fig 9b), while maintaining a large enough output-signal. This can be achieved by increasing the resistance of the TMR junction, by increasing the oxide thickness t_{ox} of the MTJ (fig. 9c). For larger values of t_{ox}, amplitude of the output voltage signal saturates due to the low-pass filtering effect of the parasitic capacitance at the output node (Fig 9d). Based on the simulation results a read current of ~0.5 μA was chosen, which was less than 1% of the bias current (~75 μA for an MTJ area of 20x20nm^2) for an oscillation frequency of 5 GHz. It provided an output voltage swing of ~100 mV that can be sensed by a CMOS inverter.

Fig 10a shows the transient plot of two DP-STNO's (solid and dashed lines) lock over time, due to dipolar-coupling. In Fig. 10b current through one of the STNOs is kept constant at 100μA and the current through the second DP-STNO is increased from 90 μA to 120 μA. Constant current through the first DP-STNO generates a constant frequency of oscillation, whereas, the frequency of the second device increases with its input current. When the frequencies of DP-STNO's are far apart, they oscillate independently. They acquire phase and frequency-lock when their frequencies lie in locking range, as depicted in Fig 10b. In this work mono-domain DP-STNO model was used for the parallel simulation of large-number of devices. This model was compared and verified with multi-domain micro-magnetic simulations, as shown Fig. 10b.

We employ a network of DP-STNOs with spin-wave-based near-neighbor coupling, for image-edge-extraction. To initialize the computation, all the STNOs were set to a locked-state using a common biasing-current and spin-wave coupling. The pixel intensities of grey-scale image were translated into current values which were added to the bias currents as external inputs. Since STNO frequency depends upon the biasing current, the neighboring STNOs for which the difference between the external inputs was large, encountered relative phase-frequency shifts, strong enough to upset the locking. The range of the input current was so adjusted that only the neighboring inputs corresponding to sharp intensity change (i.e. edges) in the image would be effective in bringing the corresponding STNOs out of lock (fig. 10d).

Fig. 11 (a) Circuit for edge detection, (b) for locked case (1) diode input, (2) output; for unlocked case (3) diode input, (4) output

The CMOS circuit for detecting the phase-frequency lock is shown in Fig 11a, which shows 9 spin wave coupled DP-STNO's. The outputs of all the STNOs in a 3x3 neighborhood are capacitively added and the resulting waveform is applied to a diode that acts as a peak-detector (PD), as shown in the figure. The signals at the input and the output of a PD corresponding to a set of STNO's oscillating within locking range, are shown in Fig 11b.1 and Fig 11b.2 respectively. Such phase-synchronous oscillations sum up to provide a relatively clean sinosoid that results in fast charging of the PD output. Fig 11b.3 and 11b.4, on the other hand show the signals at the input and the output (respectively) of a PD connected to a set of STNOs that are out of lock (corresponding to an edge location in the image). Summation of such signals results in an irregular waveform that leads to slow (or very small) charging of the PD output. Thus the edge locations can be identified by CMOS inverters connected to the PD outputs. For an oscillation frequency of 5GHz a time period of 10-ns was found to be sufficient for edge-map evolution. Fig 12a compares the power consumption of DP-STNO with conventional STNO's, showing ~98% lower computing energy for DP-STNO. Fig 12b shows the simulation framework used in this work.

The proposed device structure achieves high energy-efficiency due to low-voltage GMR interface for biasing and large-signal TMR interface for sensing. DP-STNO device can facilitate simplified interface with CMOS circuitry and is suitable for large scale integration for non-Boolean computing and RF-signaling applications.
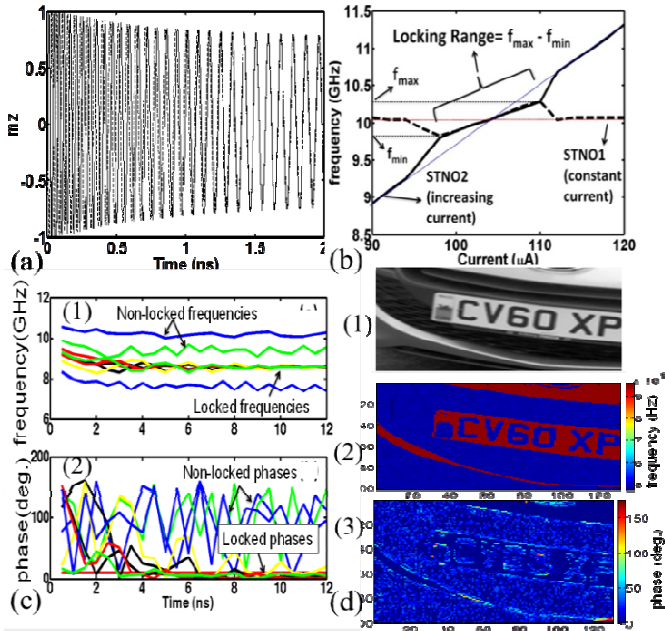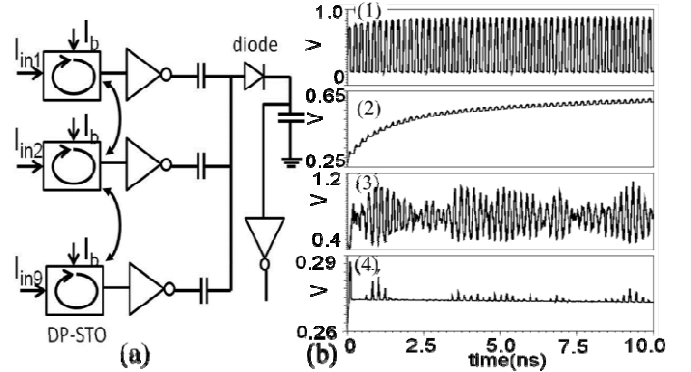

Fig. 10 (a) Transient plot of frequency locking between two DP-STNO's, (b) Frequency vs. current plot for two spin-wave coupled STNOs, showing the locking range, (c) Transient plots of spin-wave coupling, (1) frequency and (2) phase of 9 STNO's in a 3x3 array (d) : (1) Input image, (2) STNO frequency-plot, (3) STNO phase-plot

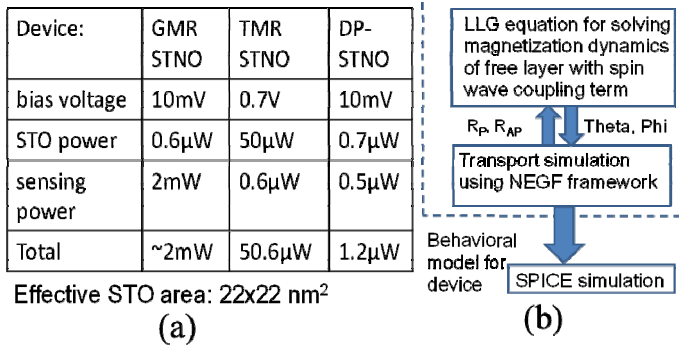| Device:	GMR STNO	TMR STNO	DP-STNO
bias voltage	10mV	0.7V	10mV
STO power	0.6µW	50µW	0.7µW
sensing power	2mW	0.6µW	0.5µW
Total	~2mW	50.6µW	1.2µW

Effective STO area: 22x22 nm^2

(a)

(b)

Fig . 12 (a) Comparison of DP-STNO with GMR and TMR STNO's, (b) Simulation framework

4. Conclusions

Emerging spin device phenomena have lead to interesting possibilities of low energy non-Boolean computing. We noted that ultra low voltage, current mode operation of magneto-metallic spin torque-devices and oscillators can be suitable for non-Boolean, analog-mode computing. Such devices may be integrated with CMOS and other charge-based devices to model energy-efficient computing systems. Non-volatility of nano-magnets can be also exploited in the design of energy-efficient programmable logic hardware for hybrid FPGAs.

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