# A Low-Cost Radiation Hardened Flip-Flop

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***Abstract*—The aggressive scaling of semiconductor devices has caused a significant increase in the soft error rate caused by radiation hits. This has led to an increasing need for fault-tolerant techniques to maintain system reliability. Conventional radiation hardening techniques, typically used in safety-critical applications, are prohibitively expensive for non-safety-critical electronics. This work proposes a novel flip-flop architecture named SETTOFF which significantly improves circuit resilience to radiation hits over previous techniques. In addition, compared to other techniques such as a TMR latch, SETTOFF reduces the area and performance overheads by up to 50% and 80%, respectively; the power consumption overhead is also reduced by up to 85%. In addition, a novel reliability metric called radiation-induced failure rate is developed which can be a valuable tool to predict the impact of radiation hits and quantitatively compare the reliability of various radiation hardened techniques. Our analysis shows that the proposed technique can achieve zero SEU failure rate, and significantly reduce the SET failure rate.**

***Keywords*—*Soft error, reliability, single-event upset, single-event transient, fault-tolerant.***

## I. Introduction

Soft errors are caused by radiation-induced transient faults in electronic systems. Neutrons from cosmic rays [1] and alpha particles from the packaging and bonding materials [2] are the major radiation sources, which can induce transient faults in 2 different ways: (1) Single Event Upsets (SEUs) which change the state stored in a storage cell; (2) Single Event Transients (SETs) which generate transient voltage pulses in combinational gates. Only the SETs that are captured by the storage elements can turn into soft errors.

SEUs are a major concern in both dense memory arrays and sequential logic. The former can be efficiently protected by conventional Error Correction Coding (ECC) techniques [3]. However, ECC is typically not applicable in random sequential logic since that is distributed across the entire system. On the other hand, the soft error rate in combinational gates increases significantly with technology scaling, and becomes comparable to that in the storage cells in 60nm technology or below [4]. Therefore, it is a challenge to achieve efficient error-mitigation in general logic.

Conventionally, safety-critical electronics (such as space applications) use Triple Modular Redundancy (TMR), [5], to mitigate soft errors in general logic. Although TMR is highly reliable, the large overhead (more than 200% area and power consumption) makes it uneconomical for most non-safety-critical electronics. There are other techniques to achieve cheaper solutions, but they are normally less reliable than TMR [6] [7]. Technology and customer demands are pushing performance and energy efficiency. However, the soft errors are becoming a concern at the same time. To balance these conflicts, it is crucial to develop a technique to provide a desirable level of reliability for non-safety-critical electronics without unacceptable overheads.

The first contribution of this paper is the design and implementation of a radiation hardened flip-flop, named SETTOFF (Soft Error and Timing error TOlerant Flip-Flop), to realize cost-efficient error-tolerance in general logic. SETTOFF can correct SEUs on the fly and detects SETs originating in the preceding combinational gates. Timing errors (TEs) are also naturally detected. By incorporating a replay recovery technique at the architectural level, SETTOFF can tolerate all SETs, TEs and SEUs. Besides providing a higher level of reliability than previous techniques, SETTOFF also requires relatively small error-tolerance overheads. With a 10% activity rate, SETTOFF consumes an average of 28% extra power in 65nm technology, compared with a standard flip-flop. The area overhead is 30 extra transistors for each bit, and the average delay overhead is 13.2%. These figures are smaller than or comparable with previous techniques. The second contribution of this paper is the development of a novel reliability metric called the radiation-induced failure rate, which can quantitatively compare the resilience of various radiation hardened techniques against particle strikes. The results show that SETTOFF can reduce the SEU failure rate to 0, and SET failure rate to 4% at 1GHz in 65nm technology.

This paper is organized as follows, the next section describes previous techniques and their drawbacks. In section III, we introduce the design of SETTOFF. The failure rate model is proposed in section IV. Section V presents the comparative evaluation results. Finally, we conclude in section VI.

## II. Previous Techniques

Previous error-tolerant techniques either require large overheads or provide a limited level of reliability. Most of them focus on either SETs or SEUs, but cannot cover both. DICE, [6], is a transistor-level approach which duplicates the state-holding elements in a conventional latch and uses feedback loops to combat SEUs. The area overhead is close to 100%. The drawback is that the SEU correction process is not immediate; therefore it generates a glitch on a correction, which may propagate and corrupt the following stage. The SEU-tolerant latch proposed in [7] uses duplicated storage and weak transistors to increase its immunity against soft errors. But it is still susceptible to particles with rather high energy.

FERST, [8], uses three C-elements to mitigate both SEUs and SETs at the input of the latch. Although FERST is

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more cost-efficient than a TMR-latch, it still induces nearly 100% area and power overheads. The C-element added in the signal path also induces a delay overhead of around 70% in 65nm technology. BISER, [9], reuses the duplicated flip-flop originally used for scan to provide a redundant copy for the system flip-flop. A C-element is used to prevent any SEUs occurring in either of the two copies from propagating. Similar to FERST, the delay overhead of BISER can be big due to the C-element added in the signal path.

The Time Redundancy-based Detection (TRD) technique, [10], detects SETs at the input of a flip-flop by comparing the sampled data at two time instants delayed by $\delta$. The error-tolerance overhead of TRD is small since no duplication is required. An SET pulse with a width no greater than $\delta$ will be detected since it cannot overlap the two time instances. The TRD technique also naturally detects timing errors occurring in the preceding combinational logic, and the SEUs occurring in the flip-flop before the second time instance. However, other SEUs will escape detection which may be fatal to the system. Razor flip-flops, [11], aim to optimize a DVS system by tuning out timing errors. Some soft errors are naturally mitigated in Razor, but the soft-error tolerance capability is limited, [12]. The SEM and STEM cells proposed in [13] remove the delay overhead cost by the error detection in TMR latch. However, the power and area overhead is still similar to TMR.

A previous version of SETTOFF, [12], can detect SEUs. However, it has a major drawback as the SEU-correction process is slow; therefore it generates a wide correction glitch which may still cause an error. Moreover, the previous design occupies 2.5 times the area of a conventional flip-flop, and it has a large delay overhead due to the additional SEU-detection circuitry added in the signal path. The design proposed in this paper has a superior performance and fault-tolerance capability, and has significantly less power and area overheads.

## III. The Low-cost Radiation-Hardened Flip-flop

In this section, we propose the radiation hardened flip-flop, SETTOFF, which overcomes the drawbacks of previous techniques and achieves a higher error-tolerance with lower cost. The errors occurring during a write cycle of SETTOFF are detected such that they can easily be recovered by a replay mechanism at the architectural level. Other errors that corrupt the state stored in SETTOFF are detected and corrected on the fly. If these errors occur during a hold cycle, it is difficult otherwise to target the erroneous write operation for architectural replay.

### A. Principle of Operation

The architecture of SETTOFF is shown in Fig. 1. The main flip-flop is a conventional flip-flop. For clarity, only the last state-holding element (the inverter pair) is shown. Node *N* indicates the state held by the inverter pair. The inverter driving the output of the flip-flop is replaced by a correction XOR-gate. Therefore, in normal operation, the output *Q* is the inverse of node *N*. We introduce SETTOFF in two parts which work in turn during the TRD interval (the high clock phase), and the TD interval (the low clock phase) shown in Fig. 2.

Part I is an adapted TRD architecture. It contains a detection XOR-gate that compares the input and output of

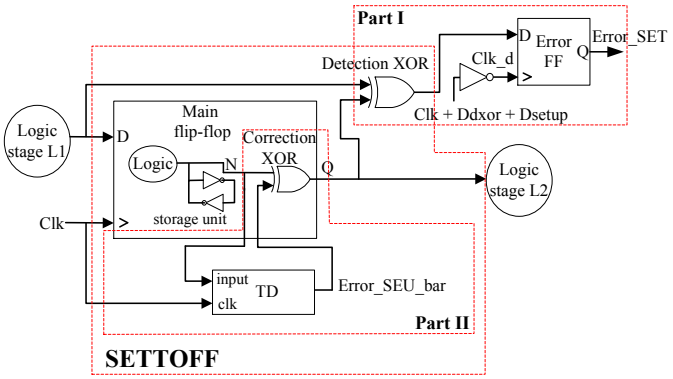


Fig. 1: The architecture of SETTOFF.

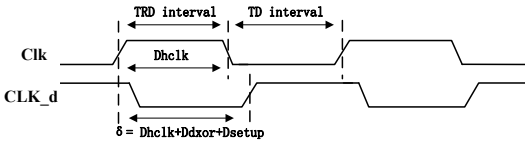


Fig. 2: The TRD and TD interval in SETTOFF.

SETTOFF, and an error flip-flop which is driven by a delayed clock (*Clk_d*). The delay element $\delta = D_{hclk} + D_{dxor} + D_{setup}$ (Fig. 2), where $D_{hclk}$ is the period of the high clock phase, $D_{dxor}$ is the delay of the detection XOR-gate and $D_{setup}$ is the setup time of the error flip-flop. The TRD interval is hence equal to $\delta - D_{dxor} - D_{setup} = D_{hclk}$. The error flip-flop is enabled during the write cycle of the main flip-flop to capture error signals. Part I is responsible for detecting three types of error during TRD interval: (1) SETs on the output of Logic Stage L1 with a pulse width no greater than $D_{hclk}$; (2) Timing errors with a delay no more than $D_{hclk}$; (3) SEUs that flip node *N* during $D_{hclk}$. The error flip-flop generates a signal upon the detection. Since the errors detected by Part I are those occurring during the write cycle of the flip-flop, it is easy to target an erroneous write operation affected by an error. A replay mechanism can be applied to re-execute the erroneous write operation and re-write SETTOFF to recover the detected SETs and SEUs. In order to recover the detected timing errors, certain frequency or voltage tuning may be required during the re-execution. This will be addressed in future work.

Part II is the TD-based architecture which is responsible for detecting and correcting the SEUs occurring during the negative clock phase (i.e. the TD interval). It comprises a transition detector (TD), monitoring the internal node *N*, and a correction XOR-gate which propagates or inverts *N* to *Q* according to the *Error_SEU_bar* signal. Only those SEUs that corrupt the last state-holding element of the main flip-flop are considered; others are masked. During the TRD interval, TD is disabled and its output (*ERROR_SEU_bar*) stays high, indicating no errors. The correction XOR-gate inverts *N* to *Q*. During the TD interval, TD is enabled such that any SEUs that flip the state stored in the inverter pair will be detected as illegal transitions at node *N*. *ERROR_SEU_bar* will then be set to zero, indicating an error so that the correction XOR-gate will propagate *N* to correct the SEU at *Q*. *ERROR_SEU_bar* will be set to 1 by the next rising clock edge and the flip-flop

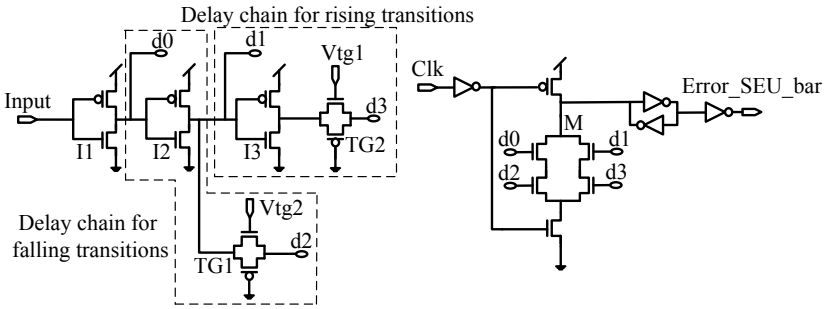


Fig. 4: The circuit schematic of TD in SETTOFF.

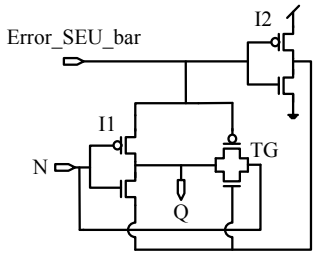


Fig. 5: The correction XOR gate.

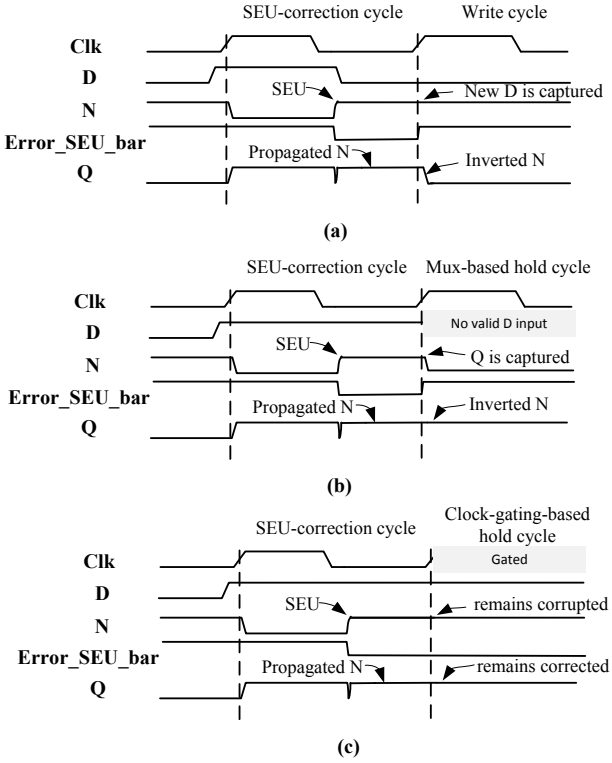


Fig. 3: The operating principle of Part II in SETTOFF.

will operate normally. To further illustrate this, we consider the three conditions shown in Fig. 3.

(a) When the cycle following an SEU-correction cycle is a write cycle, the flip-flop captures a new input value so that the bit-flip error at *N* is overwritten at the rising clock edge. Meanwhile, *ERROR_SEU_bar* is also asserted to let the correction XOR-gate invert *N* to *Q*.

(b) When the cycle following an SEU-correction cycle is a hold cycle, the flip-flop is typically held by using one of the two architectures: the multiplexer-based architecture or the clock-gating-based architecture. In a multiplexer-based architecture, the flip-flop still captures the input in a hold cycle, but the output *Q* is selected by a multiplexer to feed back into the input *D*. The flip-flop therefore captures the *Q* corrected in the former cycle to overwrite the SEU stored in the last inverter pair during the hold cycle. *ERROR_SEU_bar* is set to 1 at the same time.

(c) In a clock-gating-based architecture, the clock driving the flip-flop is gated such that no input is captured in a hold cycle. The bit-flip error remains at node *N*. The clock feeding into the TD is also gated, therefore *ERROR_SEU_bar* remains at 0 to ensure that the bit-flip stays corrected at *Q*.

The SEU-correction process generates a correction glitch (see Fig. 3) at the output of SETTOFF due to the propagation delay of the TD. However, the width of the glitch is very small with a mean value of 98ps in 65nm technology (studied in Section IV). This is due to the fact that the TD is relatively fast and the correction process is embedded in the flip-flop architecture. Even if the correction glitch propagates, it is not fatal because if captured in the following stage, it will be detected by the TRD architecture as an SET pulse.

### *B. Transistor Level design of SETTOFF*

The circuit schematic of TD shown in Fig. 4 is developed from the transition detector proposed for the former version of SETTOFF [12]. The high clock signal is used to disable TD and assert the *ERROR_SEU_bar* signal. The lower dynamic OR-gate is enabled only during the negative phase of the clock. Two delay chains are constructed, each by an inverter and a transmission gate, to capture the rising and falling transitions at the input node, respectively. If a rising transition is captured, nodes *d1* and *d3* will be both asserted momentarily to discharge node *M*, and *ERROR_SEU_bar* will be set to zero. A falling transition will discharge node *M* through *d0* and *d2*. The cross-coupled inverter pairs are used to prevent node *M* from discharging or charging due to leakage currents.

Fig. 5 shows the circuit schematic of the correction XOR-gate, which is used to replace the inverter in a conventional flip-flop to drive the output *Q*. The input *Error_SEU_bar* is connected to the output of the TD, which is 1 in normal operation. Therefore the Transmission Gate (TG) is blocked and the delay of the XOR-gate equals that of inverter I1, which is the same as the delay of the replaced inverter in normal operation. In other words, SETTOFF completely removes the extra delay path used for SEU-corrections. The increase of the CLK-to-Q delay in SETTOFF is only caused by the extra load added at the output of the flip-flop.

### *C. Clock Management*

Using the system clock to drive both the main flip-flop (on the rising edge) and the error flip-flop (on the falling edge)

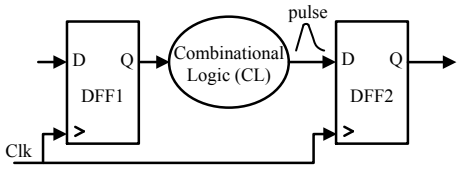


Fig. 6: The synchronous pipeline architecture for failure rate model.

is significantly simpler than using two separate clocks. The TRD and TD intervals in SETTOFF can be altered by tuning the clock duty cycle to achieve the best trade-off between the SET detection capability and SEU correction capability. An asymmetric clock may be required and buffers may need to be inserted to satisfy the shortest path constraint of the TRD architecture [12]. However, the falling clock edge is not timing-critical in normal operation. The duty-cycle clock jitter at the falling clock edge only affects the TRD interval.

## IV. Statistical Analysis of Failure Rates

A failure of a flip-flop is defined as the corruption of its output due to an SET or an SEU. This section proposes two metrics, SET failure rate and SEU failure rate, which can quantify the resilience of various radiation hardened designs against high energy particle strikes.

### A. SET Failure Rate Evaluation Model

Consider a synchronous pipeline, Fig 6. Assume an SET pulse has been generated within the Combinational Logic (CL) and has propagated to DFF2. The pulse can cause a functional failure if it is erroneously sampled (but meets the setup and hold time of DFF2), or if it forces the device to go into the metastability state (violates the setup and hold time of DFF2).

*1) SET Failure Rate Model for Conventional Flip-flops:* For a pulse to be sampled by a flip-flop its amplitude has to satisfy two conditions: (a) it exceeds the threshold voltage before DFF2 samples its input; (b) it remains higher than the threshold voltage, while the input is being sampled. The probability of a functional failure caused by a transient pulse is product of the probability of the two conditions.

*Probability of Condition (a)*: Fig. 7 shows two scenarios for the transient pulse. Scenario (1) satisfies Condition (a), while Scenario (2) does not cause a failure since the amplitude of the pulse exceeds the threshold voltage after the data sampling. $T_{clk}$ is the clock period. $t$ denotes the time that the pulse appears at the input of the DFF2, which can be any time during the clock cycle, therefore $t$ can be written as:

$$t = \alpha T_{clk} \tag{1}$$

where $0 \leq \alpha \leq 1$ and $D$ denotes the time it takes for the pulse to reach the threshold voltage. It depends on the delay of the path the pulse has taken (logic + wire delay). The probability ($Pr$) of Scenario (1) is:

$$g1 = Pr(T_{clk} \geq D + \alpha T_{clk}) \tag{2}$$

The timing variables $D$ and $T_{clk}$ are functions of the circuit's physical layout and supply voltage, which are subject to random process variations [14]. Based on the results and arguments in [14], it is reasonable to assume that these timing variables have normal distributions. $\mu_D$ and $\mu_{T_{clk}}$ denote the mean values of $D$ and $T_{clk}$ respectively, and $\sigma_D$ and $\sigma_{T_{clk}}$ denote the standard deviations. The closed form solution of Equation (2) can be obtained as a function of $\alpha$, [15]:

$$g1 = \Phi(\frac{(\alpha-1)\mu_{T_{clk}} + \mu_D}{\sqrt{\sigma_D^2 + ((\alpha-1)\sigma_{T_{clk}})^2}}) \tag{3}$$

where

$$\Phi(x) = \frac{1}{2} + \frac{1}{2} erf(\frac{x}{\sqrt{2}}). \tag{4}$$

*Probability of Condition (b)*: If the transient pulse satisfies Condition (a), there are another two cases shown in Fig. 8. Scenario (3) satisfies Condition (b), in which the amplitude of the pulse remains higher than the threshold voltage when sampled. Scenario 4 does not cause failures since the amplitude of the pulse falls below the threshold voltage before the data is sampled. $w$ denotes the width of the pulse, the time for which the amplitude of the pulse exceeds the threshold voltage. The probability of Scenario (3) is given as:

$$g2 = Pr(T_{clk} \leq D + \alpha T_{clk} + w) \tag{5}$$

According to the SET distribution results presented in [16], [17], SET pulses can also be modelled by a normal distribution. Hence, similar to Condition (a), the closed form solution for Equation (5), as a function of $\alpha$, is:

$$g2 = \Phi(\frac{(1-\alpha)\mu_{T_{clk}} - \mu_D - \mu_w}{\sqrt{\sigma_D^2 + \sigma_w^2 + ((1-\alpha)\sigma_{T_{clk}})^2}}) \tag{6}$$

The failure rate for such a transient pulse is hence the product of $g1$ and $g2$:

$$Fr = g1 \cdot g2 \tag{7}$$

*2) SET Failure Rate Model for SETTOFF:* As with a conventional flip-flop, a transient pulse has to satisfy two conditions to corrupt SETTOFF. The first condition is the same as that for a conventional flip-flop. However, the second condition requires the pulse amplitude to remain higher than the threshold voltage not only when it is sampled, but also till the end of the TRD interval. Let the duty cycle of the clock be $\tau = T_{TRD}/T_{clk}$, where $T_{TRD}$ denotes the TRD interval which is equal to the high phase of the clock. The probability of the second condition for SETTOFF can be derived as:

$$\begin{aligned} g2' &= Pr(T_{clk} + \tau T_{clk} \leq D + \alpha T_{clk} + w) \\ &= \Phi(\frac{(1+\tau-\alpha)\mu_{T_{clk}} - \mu_D - \mu_w}{\sqrt{\sigma_D^2 + ((1+\tau-\alpha)\sigma_{T_{clk}})^2 + \sigma_w^2}}) \end{aligned} \tag{8}$$

The failure rate in this case is the product of $g1$ and $g2'$:

$$Fr' = g1 \cdot g2' \tag{9}$$

### B. SEU Failure Rate Evaluation Model

SEUs that flip the output of a conventional flip-flop cause a failure at 100% probability. SETTOFF corrects SEUs on the fly by generating a correction glitch, which does not cause a failure unless it corrupts a SETTOFF flip-flop in the following stage. The SEU failure rate of SETTOFF therefore equals the failure rate caused by the correction glitch, and can be derived by using Equation (9) to model the failure rate of SETTOFF caused by correction glitches from the previous stage.

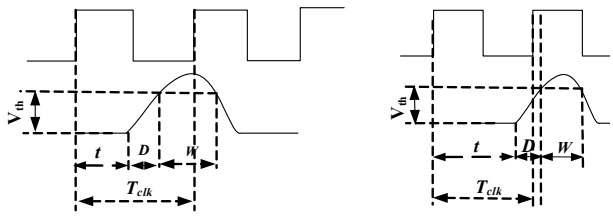


Fig. 7: Timing Condition (a) of the transient pulse.

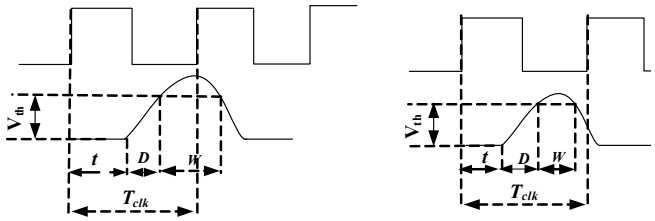


Fig. 8: Timing Condition (b) of the transient pulse.

## V. Experimental Setup and Comparative Results

SETTOFF has been implemented in a 65nm technology for evaluation. We compare SETTOFF with other previous techniques in terms of reliability and error-tolerance overheads.

### A. SET Failure Rate Results

The SET failure rates for both the conventional flip-flop and SETTOFF are evaluated in the proposed model. The mean $\mu_D = 10ps$ is measured by using a combinational gate with a fixed drive strength and a flip-flop connected together. The relative standard deviation of the $T_{clk}$ and $D$ were both set to 10% to model parameter variations. These values are in agreement with the results presented in [18]. The SET width distribution results for 65nm technology presented in [17] are used for the evaluation. The mean and the standard deviation of the pulse widths are derived from the distribution results, where $\mu_w = 530ps$ and $\sigma_w = 150ps$. Both of the flip-flops are driven by symmetric clocks at 1GHz, which means that the TRD interval of SETTOFF is 500ps in this case.

For both the conventional flip-flop and SETTOFF, the SET failure rates are a function of $\alpha$, which indicates the time instance when a transient pulse occurs during a clock cycle (see Equation (1)); therefore $Fr$ and $Fr'$ vary with $\alpha$. The evaluation results show that with different $\alpha$ values, the average SET failure rate ($Fr$) of a conventional flip-flop is 45% in 65nm technology. SETTOFF reduces the average SET failure rate ($Fr'$) to 4% with a 500ps TRD interval. Notice that SETTOFF can further decrease the SET failure rate by using asymmetric clocks with wider TRD intervals. The average SET failure rate can be reduced to zero when the TRD interval reaches 800ps.

### B. SEU Failure Rate Results

The SEU failure rate of SETTOFF caused by the correction glitch is evaluated. The width of the glitch is measured under various PVT corners. The temperature variation ranges from 5°C to 45°C with a typical value of 25°C. The 1.2V supply voltage and transistor sizes vary from -10% to 10%. The measurement results show that the correction glitch can also be modelled by a normal distribution. The mean of the correction glitches $\mu_{w'} = 98ps$. The standard deviation $\sigma_{w'} = 33ps$. The results show that SETTOFF can reduce the SEU failure rate to 0 when using a 1GHz symmetric clock (500ps TRD interval). This is because the width of the correction glitch is much smaller than that of a typical SET pulse, so the TRD interval can easily cover such glitches even when they are broadened during propagation.

### C. Implementation Overhead and Comparative Results

Table I summaries the error-tolerance capability and overheads of different radiation hardened techniques in 65nm technology. Since the error flip-flop in the TRD architecture can be easily shared by multiple bits, SETTOFF requires 30 extra transistors. Compared with a conventional flip-flop built with 32 transistors, SETTOFF has a 94% area overhead. This is noticeably smaller than the former version which had a 150% area overhead. FERST requires an area overhead of around 100% (42% less than TMR) in 65nm technology [8]. The area overhead percentage of BISER is small since it uses the scan flip-flop as a duplicate. SETTOFF has a comparable area overhead with Razor, which requires 31 extra transistors.

The power consumption of the conventional flip-flop and SETTOFF with the same drive strength are compared. Both of the flip-flops were tested with 1.2V supply voltage and 185MHz clock. The clocks and the inputs of the flip-flops are driven by signals with 50ps transition times. At a 10% activity rate, the average power overheads of SETTOFF compared with a conventional flip-flop with different load capacitance is 28.0%. This is much lower than the former version which requires an average 40.8% power overhead under the same operating conditions. SETTOFF induces a relatively small power consumption overhead because the error-mitigation circuitry does not require switching power in normal operation. Previous techniques (such as DICE and FERST) typically rely on the duplication of the state-holding elements which consumes extra switching power even in normal operation. Therefore, their power overheads can be more than 100%. BISER has a power overhead of 126% compared to a scanned flip-flop. The power overhead of SETTOFF is comparable to Razor flip-flops which require 28.5% to 30.0% extra power under the same operating conditions in 130nm technology.

Compared with a conventional flip-flop with the same drive strength, SETTOFF induces an average CLK-to-Q delay overhead of 13.2% when using different load capacitance. This is about 50% less than the previous version which induces an average of 26.5% delay overhead. The majority voter in TMR, and the C-elements in FERST and BISER are all in the signal path. They induce a similar delay overhead of around 70%, which is much more noticeable than SETTOFF. The delay overheads of DICE and STEM are not reported by the authors. However, they do not have error-tolerant circuitry added in the signal path; therefore the delay overhead should be small.

The error-tolerance capability of different techniques are compared using the SET and SEU failure rates derived from 65nm technology when using 1GHz symmetric clocks. TMR

TABLE I: Comparison of error-tolerance capability and overheads in 65nm technology

| | Conventional flip-flop | SETTOFF | TMR latch | DICE | FERST | BISER | STEM |
|---|---|---|---|---|---|---|---|
| Area overhead | - | 94% | 200% | 100% | 100% | 24% | 200% |
| Power overhead | - | 28% | 200% | 100% | 100% | 126% | 200% |
| Delay overhead | - | 13.2% | 70% | not reported | 70% | 70% | not reported |
| SET failure rate (average) | 45% | 4% | 45% | 45% | 4% | 45% | 4% |
| SEU failure rate | 100% | 0 | 0 | 3.8% | 0 | 0 | 0 |
| Timing error tolerance | NO | YES | NO | NO | NO | NO | YES |

latch, DICE, and BISER do not have SET-tolerance capabilities; therefore the average SET failure rate is the same as for a conventional flip-flop. STEM uses an adapted TRD architecture to tolerate SETs, thus its average SET failure rate is the same as that of SETTOFF. FERST uses a delay element followed by a C-element to prevent SETs from propagating to the latch. The average SET failure rate is also the same for FERST, when using a delay equal to that of a TRD architecture. Apart from DICE, all other techniques can reduce the SEU failure rate to 0. The SEU failure rate in DICE is caused by the SEU-correction glitch being propagated and sampled by the following stage. SETTOFF eliminates the threat of the SEU-correction glitch in DICE. In addition, the SEU tolerant capability of SETTOFF does not depend on the particle energy or the affected nodes as most previous transistor level approaches. The SEUs at any internal nodes are tolerated if they corrupt the output of a flip-flop. Among them all, only SETTOFF and STEM tolerate both SETs & SEUs, and timing errors. However, SETTOFF provides a better trade-off between the error-tolerance capability and the overheads.

Notice that SETTOFF can be used to construct multiple-bit registers or the register file in a microprocessor. The SETTOFF-based register can tolerate not only a Single-Bit Upset (SBU), but also Multiple-Bit Upsets (MBUs) since each bit has its own built-in correction circuitry. The MBU-tolerant capability gives the SETTOFF-based register a noticeable improvement in reliability over the conventional ECC technique, which requires much larger overhead to correct MBUs.

## VI. Conclusions and Further Work

This paper has proposed a radiation hardened flip-flop, SETTOFF, that is suitable for protecting non-safety-critical electronics. In SETTOFF, the SEUs occurring inside the flip-flop are corrected on the fly and the SETs and timing errors occurring in the preceding logic are detected. By combining with a replay recovery technique at architectural level, SETTOFF can efficiently tolerate all the SETs, SEUs and timing errors. Besides providing a better error-tolerance capability than most previous techniques, SETTOFF requires less or a comparable overhead. A reliability metric is also proposed to comparatively evaluate the reliability of SETTOFF and other radiation hardened techniques. The results show that SETTOFF reduces the SEU failure rate to 0 and SET failure rate to 4% at 1GHz in 65nm technology. Future work will focus on implementing a microprocessor with SETTOFF to realize system-level error-tolerance.

## References


[1] J. Ziegler and W. Lanford, "The effect of sea level cosmic rays on electronic devices," in *Solid-State Circuits Conference. Digest of Technical Papers. 1980 IEEE INT*, vol. XXIII, Feb. 1980, pp. 70 – 71.

[2] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," *Electron Devices, IEEE Transactions on*, vol. 26, no. 1, pp. 2 – 9, 1979.

[3] C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," *IBM Journal of Research and Development*, vol. 28, no. 2, pp. 124 –134, Mar. 1984.

[4] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Dependable Systems and Networks, 2002. DSN 2002. Proceedings. International Conference on*, 2002, pp. 389 – 398.

[5] M. Favalli and C. Metra, "TMR voting in the presence of crosstalk faults at the voter inputs," *Reliability, IEEE Transactions on*, vol. 53, no. 3, pp. 342 – 348, Sept. 2004.

[6] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 6, pp. 2874 –2878, Dec. 1996.

[7] S. Whitaker, J. Canaris, and K. Liu, "SEU hardened memory cells for a CCSDS Reed-Solomon encoder," *Nuclear Science, IEEE Transactions on*, vol. 38, no. 6, pp. 1471–1477, 1991.

[8] M. Fazeli, S.-G. Miremadi, A. Ejlali, and A. Patooghy, "Low energy single event upset/single event transient-tolerant latch for deep submicron technologies," *Computers Digital Techniques, IET*, vol. 3, no. 3, pp. 289–303, 2009.

[9] S. Mitra, N. Seifert, M. Zhang, Q. Shi, and K. S. Kim, "Robust system design with built-in soft-error resilience," *Computer*, vol. 38, no. 2, pp. 43–52, 2005.

[10] L. Anghel and M. Nicolaidis, "Cost reduction and evaluation of a temporary faults detecting technique," in *Design, Automation and Test in Europe Conference and Exhibition. Proceedings*, 2000, pp. 591 –598.

[11] S. Das, C. Tokunaga, S. Pant, W.-H. Ma, S. Kalaiselvan, K. Lai, D. Bull, and D. Blaauw, "RazorII: In situ error detection and correction for PVT and SER tolerance," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 1, pp. 32 –48, Jan. 2009.

[12] Y. Lin and M. Zwolinski, "SETTOFF: A fault tolerant flip-flop for building cost-efficient reliable systems," in *On-Line Testing Symposium (IOLTS), 2012 IEEE 18th International*, June 2012, pp. 7 –12.

[13] N. Avirneni and A. Somani, "Low overhead soft error mitigation techniques for high-performance and aggressive designs," *Computers, IEEE Transactions on*, vol. 61, no. 4, pp. 488 –501, Apr. 2012.

[14] S. Nassif, K. Bernstein, D. Frank, A. Gattiker, W. Haensch, B. Ji, E. Nowak, D. Pearson, and N. Rohrer, "High performance cmos variability in the 65nm regime and beyond," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 569–571.

[15] J. A. Gubner, *Probability and Random Processes for Electrical and Computer Engineers*. Cambridge: Cambridge Univ. Press, 2006.

[16] R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "SET pulse-width measurement eliminating pulse-width modulation and within-die process variation effects," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*, 2012, pp. SE.1.1–SE.1.6.

[17] ——, "Measurement circuits for acquiring SET pulsewidth distribution with sub-FO1-inverter-delay resolution," in *Quality Electronic Design (ISQED), 2010 11th International Symposium on*, 2010, pp. 839–844.

[18] A. Narasimhan and R. Sridhar, "Impact of variability on clock skew in h-tree clock networks," in *Quality Electronic Design, 2007. ISQED '07. 8th International Symposium on*, 2007, pp. 458–466.