Modeling and Analysis of Digital Linear Dropout Regulators with Adaptive Control for High Efficiency under Wide Dynamic Range Digital Loads

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Abstract – Discrete time digital linear regulators, including low dropout regulators (LDOs) have become competitive in muti-Vcc digital systems for fine-grained spatio-temporal voltage regulation and distribution. However, wide dynamic current range of the digital load circuits poses serious problems in maintaining stability and high efficiency at all corners. In this paper we present a control model for discrete time LDOs and demonstrate how online adaptive control can be employed for consistent performance and high efficiency across the load current range.

I. INTRODUCTION

With current technology scaling providing manufacturing processes at 22nm and beyond, microprocessors and SoCs continue to improve both performance and power efficiencies. With many voltage domains providing fine-grained spatial and temporal control of the operating voltage and frequency, and software-controlled chip power-states enabling lower standby power along with faster wake-up, digital circuits are expanding their dynamic ranges of operation. The integration of on-die voltage regulation on the core microprocessor [1,2] allows faster and wider dynamic voltage and frequency scaling (DVFS).

Modern microprocessors and SoCs employ hierarchical voltage regulators to allow fine grained voltage distribution and regulation (Fig. 1). Hence the digital load supplied by each VR is smaller and exhibits higher dynamic range. Unfortunately, this comes at the expense of lower de-coupling capacitor per grid, higher IR drops, and complex interconnected control systems. This leads to over-design and unwanted frequency and power guard-bands that often limit both power efficiency as well as the granularity at which the supply voltages can be regulated. The VRs of choice for local supply regulation are linear voltage regulators (LVRs) including low-dropout regulators (LDOs) [1-2]. Analog design solutions for linear VRs are not compatible with the digital design and process flows, and require careful custom design and placement. Consequently, design solutions have been proposed for linear regulators with digital control using digital process and libraries. Such LVRs can be discrete time [1] or continuous time [2] and provide compact, process compatible, high efficiency design solutions.

With the popularity of digital LVRs, it is prudent to investigate not only the overall stability of LVRs, but also understand how to maximize high efficiency with adaptive control under wide dynamic digital loads. This problem is further exacerbated by the fact that digital loads undergo large dynamic ranges, resulting in significant movement of the output pole frequency, thereby making it difficult to guarantee overall system stability across the operating range. The time and frequency domain response of the closed loop system also changes as the output load changes going from an under-damped to an over-damped system. Further designing for the highest load current leads to an inefficient design solution in light load conditions. This calls for autonomous and adaptive control strategies in the VR loops that will be cognizant of the position of the output pole. In this paper, we introduce adaptive digital control for discrete time linear regulators with focus towards wide dynamic range of operation. We present a comprehensive and novel discrete time regulator design emphasizing on programmable gain and high system efficiency. We introduce a hybrid control model for the digital LDO that comprehends the dynamic nature of the load, and illustrate through models and simulations how autonomous and dynamic adaptation can be achieved during runtime for a consistent time and frequency domain response of the closed loop system.

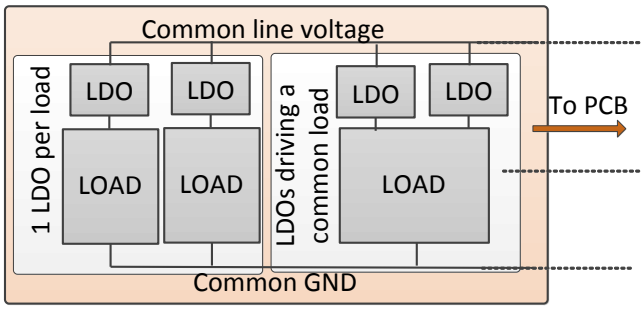

Fig. 1: A generic VR architecture of a multi LDO regulator system illustrating two possible scenarios (a) single LDO driving a single load or (b) multiple LDOs driving the same load.

In section II of this paper, we propose the design of a discrete time digital LDO focusing on the different design components. This is followed by a hybrid control model in Section III illustrating the interaction of the discrete time LDO loop and the continuous time output load (plant). Simulation results are presented in section IV, followed by the proposed adaptive control strategies and simulation results in section V.

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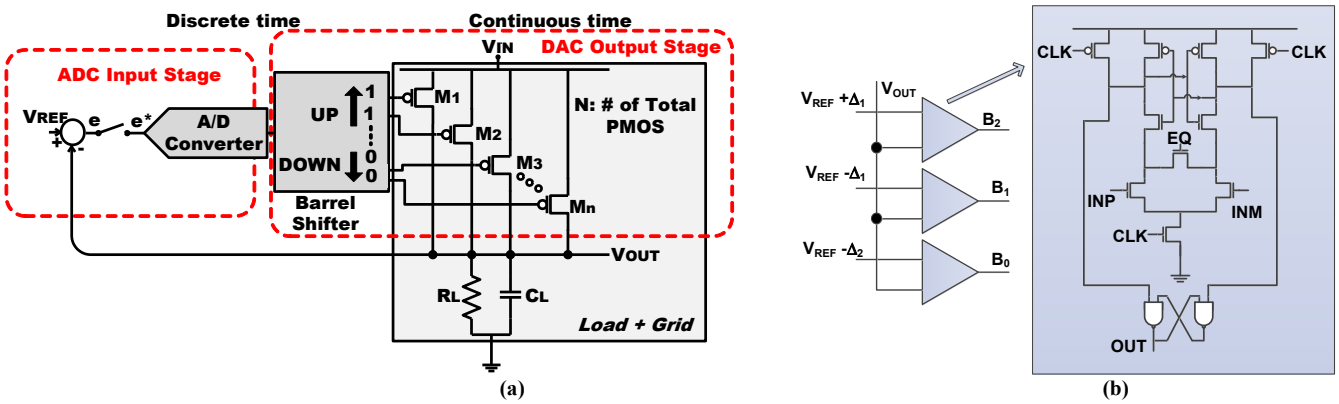


Fig. 2: (a) Schematic diagram of a generic discrete time digital LDO featuring (i) an input ADC stage (ii) a barrel shifter with programmable gain (iii) a current DAC based output stage. The CLK is not explicity shown and is used by the ADC and the shifter (b) The topology of the ADC stage featuring clocked comparators and a 3b thermometer coded output. The voltage levels Δ1 and Δ2 are programmable and represent the resoloution of the output. By making Δ1 infinitesimally small, we can realize a bang-bang controller. Using different magnitudes for Δ1 and Δ2 can also result in a non-linear ADC and non-linear control.

II. DISCRETE TIME DIGITAL LDOs: DESIGN PERSPECTIVE

Power management of microprocessors and SoCs contain both off-chip switching converters and on-chip LDOs and provide regulated power supplies to different voltage islands. For digital loads requiring large dynamic range, the impetus for a local LDO are digital design, fine spatiotemporal voltage regulation, scalability and higher system power efficiency across load conditions. This often comes at an expense of reduced PSR, higher output ripple (in a bang-bang type controller) and lower loop bandwidth. The discrete-time digital LDO proposed consists of three main stages: an ADC input stage, a controller stage with programmable gain and a current-based DAC at its output stage. In this section we will discuss a generalized form of the design illustrating the key design components.

As shown in Fig. 2, the analog-to-digital converter (ADC) samples the output voltage at the rising edge of the ADC clock. The resolution of the ADC shows a design trade-off between the speed of the regulator loop and the complexity of design. For most practical designs a 1-4b flash ADC suffices. Bias currents in the ADC comparator can be avoided by employing a CLK-ed sense amplifier (SA) based ADC front-end. Fig. 2a shows a typical flash ADC block diagram and Fig. 2b shows a simple architecture of a SA with a latch connected at the output for signal restoration. For an N-bit thermometer coded ADC output, the circuit employs N comparators with reference voltages determining the corresponding resolution of the converter. Thus the ADC provides a digitally sampled measure of the error voltage (V_{OUT} -V_{REF}) and this encoded error is used in the control loop to turn on or off power MOSFETs. In steady state the closed loop control will ensure an infinitesimally small error, and the output voltage (V_{OUT}) will track the reference (V_{REF}).

The ADC output drives a bidirectional barrel shifter. The purpose of the barrel shifter is to take in parallel data, shift it, and drive control signals to the power PMOSes. If the error (ADC output) is negative illustrating $V_{OUT} > V_{REF}$, then the shifter shifts down, turning off more PMOSes. On the other hand a positive error leads to a shift-up resulting in the turning-on of more PMOS devices. The number of PMOS devices that will be turned on for each bit of error, is programmable and implemented using the barrel shifter. The architecture of the parallel barrel shifter allows the shifter to achieve multiple gains of two and three shifts in a single cycle. A higher gain is instrumental for a faster convergence when the error voltage is larger in magnitude thereby causing a multi-bit error. The shifter used in the current design is 128b wide and uses two 4x2 bit multiplexers. The first level mux makes the choice between latch outputs An, An+2 and An-2 to produce the output Bn. The second level of a mux makes a choice between Bn, Bn+1, and Bn-1 to determine the input to each latch. The select signals are chosen according to sign and the magnitude of the error. As an example, different

Table I

B2	B1	B0	d	mux_1	mux_2
0	0	0	1	k1	k0
0	0	1	1	0	1
0	1	1	0	0	1
1	1	1	0	k1	k0

k1	k0	Programmable gain
1	1	3
1	0	2
0	1	1

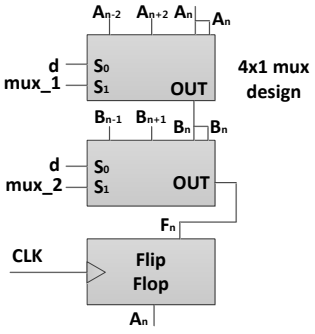


Fig 3: Generation of the control signals for the barrel shifter corresponding to the ADC outputs (B_{0-2}). The barrel shifter is composed of two 4-to-1 MUXes with programmable direction and magnitude of shift. Symbols d represent the direction of the shift (1=up; 0=down) and mux_1, mux_2 controls the amount of shift. Table I illustrates the different programming modes and the control of the barrel shifter by the ADC output.

programmability modes corresponding to different gains have been shown in Table. I.

The output stage of the digital LDO comprises of a bank of pull up PMOS devices. Depending on the demand of the load current as well as the target output voltage (V_{REF}), a section of the PMOSes is turned ON and the rest are OFF. In steady state, when regulation is achieved, the number of ON PMOSes is just enough to supply the load current and suppress the error voltage to an infinitesimal value.

III. HYBRID CONTROL MODEL FOR DISCRETE TIME DIGITAL LDOS

To understand the overall control loop and the overall system stability, we present a z-domain model for the digital LDO, as illustrated in Fig. 4. The ADC acts as a voltage sampler and converts the continuous time error signal to its discrete time representation e*.

$$e^* = V_{REF}(nT) - V_{OUT}(nT) \quad (1)$$

The barrel shifter acts as a discrete time integrator and in its simplest implementation α=1. The output of the shifter, which is a thermometer coded digital word (D(nT)) represents the number of pull-up PMOSes that are on at the time instance, nT, where T is the period of the sampling ADC Clock. It can be written as:

$$D(nT) = \alpha D\big((n-1)T\big) + K_{DIGITAL}e(nT) \quad (2)$$

Here $K_{DIGITAL}$ is the overall gain of the digital control loop and is set by the programmable gain of the barrel shifter. Non-linear gain can be provided, as shown in Table I. It programs the step-size in the barrel shifter.

From Eq. (2) the transfer function D(z) is :

$$D(z)=K_{DIGITAL}\frac{z}{z-\alpha}e(z) \quad (3)$$

The output of the shifter controls the number of PMOSs that are turned on, and thus interfaces with a continuous time plant (power MOSFETs and the load). This can be modeled as a zero-order hold (ZOH) cascaded with a single order plant whose output pole, a, is given by the load circuit. The s-domain model for ZOH followed by the plant is:

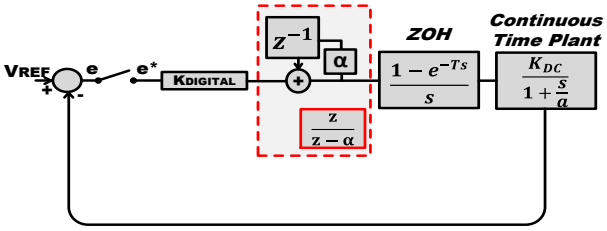


Fig. 4: A hybrid control diagram of the discrete time digital LDO illustrating the discrete time control and the continuous time plant.

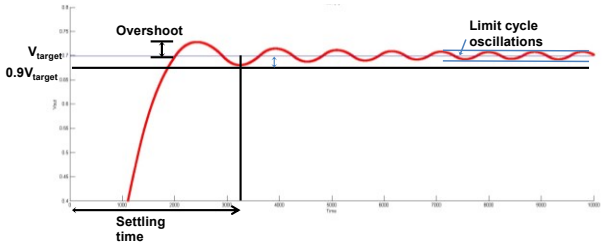


Fig 5: An example step response of the digital LDO control loop illustrating relevant parameters.

$$P(s)=\left(\frac{1-e^{-sT}}{s}\right)\left(\frac{K_{DC}^{PLANT}}{1+\frac{s}{a}}\right) \quad (4)$$

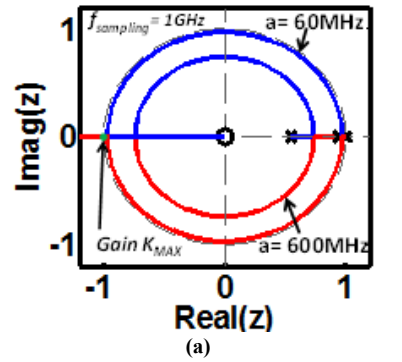
Using the Eq. (3) the corresponding P(z) in the z-domain can be represented as

$$P(z) = \frac{K_{DC}^{PLANT}(1-e^{-aT})}{a}\left(\frac{1}{z-e^{-aT}}\right) \quad (5)$$

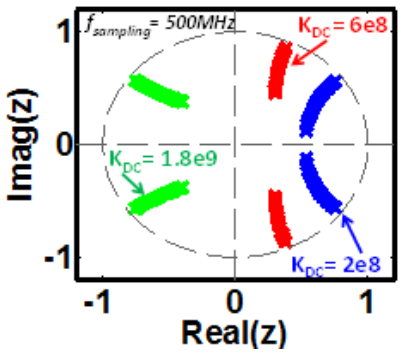
Thus, the open loop forward path transfer function of the digital LDO can be written in the z-domain as:

$$G(z)=K_{DIGITAL}K_{DC}^{PLANT}(1-e^{-aT})\frac{z}{(z-\alpha)(z-e^{-aT})} \quad (6)$$

where $T=1/F_{SAMPLING}$ is the time period of the sampling CLK of the digital control and the plant load frequency (a)



(a)



(b)

Fig. 6: Root locus of the digital control in the Z-plane showing (a) the maximum allowable gain corresponding to two output pole frequencies and (b) the movement of the closed loop poles as the digital load current changes in a representative circuit (data derived from [3])

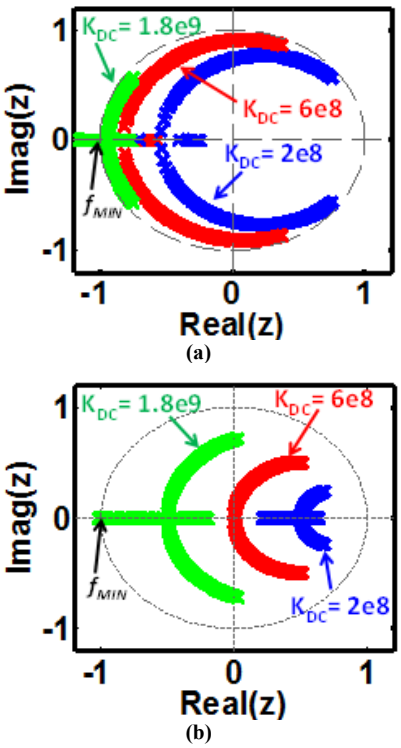


Fig. 7: Root locus of the digital control in the Z-plane showing the minimum sampling frequency required for the system to be stable (f_{MIN}) under two different load conditions (a) pole of the output load is at 600MHz and (b) pole of the output load is at 60MHz.

can be described as follows:

$$R_{pu} = \left(\frac{R_{on}}{\mathrm{D(nT)}} + \frac{R_{off}}{N - D(nT)}\right)$$

$$Z_{eq} = \frac{R_L}{1 + sCR_L} \qquad (7)$$

$$\mathrm{a} = Z_{eq} || R_{pu} = \frac{Z_{eq} R_{pu}}{Z_{eq} + R_{pu}}$$

where N is the total number of pull-up PMOSes.

As can be observed in the Eq. (5), the poles are located at $\mathrm{z} = \propto$ and $\mathrm{z} = \mathrm{e}^{-\mathrm{aT}}$. Using unity feedback, the overall closed loop transfer function of the digital LDO in the z-domain is:

$$\mathrm{H(z)} = \frac{\mathrm{G(z)}}{1 + \mathrm{G(z)}} \qquad (8)$$

Eq. (5-8) provides insights into the stability of the digital LDO. Key parameters from an example transient response of the proposed model are shown in Fig. 5. Noting that for a digital system to be stable, the poles in the z-domain need to lie within the unit circle, we can perform a root-locus analysis of the system, which shows the closed loop poles while the open loop DC-gain K_{DC} of the system is varied. Fig. 6a shows the root locus of the digital LVR for two different output poles, 600MHz and 60MHz. The root-locus provides design insight into the maximum DC-gain that can be achieved without causing instability in the loop. It can be observed that a maximum DC gain of 10.71dB (30.46dB) can be achieved for an output pole position of 600MHz (60MHz), respectively. Ensuring stability in a digital control for digital load circuits is made difficult by the fact that the underlying circuit can go through wide dynamic ranges of operation, across V_{CC}, power states as well as fine-grained power gating. From data published in [3] on a wide dynamic range digital signal processor, we can obtain the movement of the output pole (e^{-aT}) in the z-plane, and it has been plotted in Fig. 6b. For a constant gain and sampling frequency, one can note how the output pole position traces a locus on the z-plane leading to a stable system for higher load currents and a heavily under-damped (or instable) system for light load conditions as the closed loop zero approaches the unit circle. Further, the root locus of the system as the sampling frequency is varied, is shown in Fig. 7a and 7b for two different output pole positions illustrating the bound on the minimum sampling frequency for the system to be stable.

IV. SIMULATIONS AND RESULTS

The proposed digital LDO has been designed and simulated across a wide dynamic load range in the Toshiba 65nm process using nominal devices and a nominal V_{CC} of 1V. A nominal gain K=1 has been chosen to illustrate the key design trade-offs. We observe the closed loop LDO response under varying $F_{SAMPLING}$ when a voltage noise of magnitude 200mV is injected on the local grid by turning on pull down noise generator circuits. First, let us consider the effect of the sampling frequency when the load current is constant. As can be seen in Fig. 8, a low value of $F_{SAMPLING}$

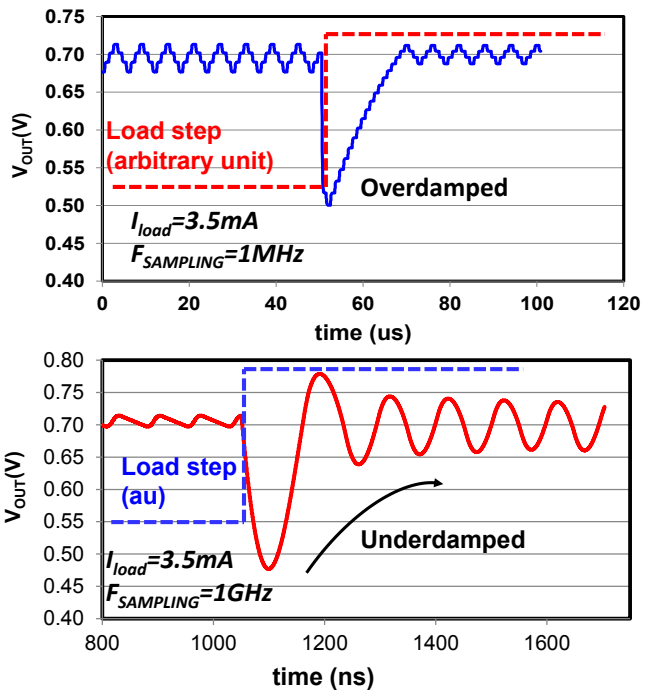


Fig. 8: SPICE simulations showing the change of loop behavior as the sampling frequency changes at iso-load conditions in response to a step load. The magnitude of the load step has been adjusted to produce iso-droop (~200mV) on the grid.

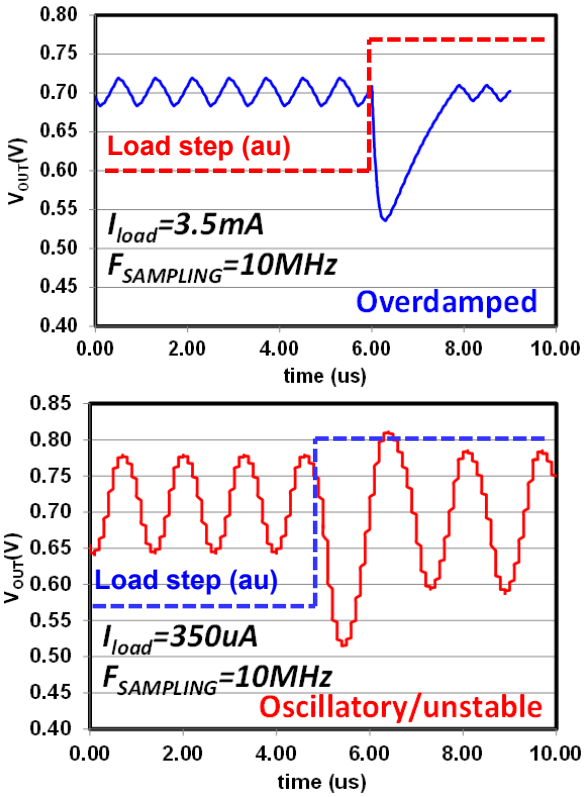


Fig. 9: SPICE simulations showing the change of loop behavior as the load condition changes from 3.5mA to 350uA at iso- sampling frequency in response to a step load.

(1MHz) results in an over-damped system response in whereas a higher sampling frequency $F_{SAMPLING}$ =1GHz leads to a severely under-damped response. This results in a faster settling time (due to the increase in the sampling frequency), but exhibits higher limit cycle oscillations and oscillatory behavior. This inconsistency in the loop response under varying load becomes stark as the load current changes. In digital logic the load current can change by two or three orders of magnitude as different functional units are activated or go to sleep states. Fig. 9 illustrates the closed loop system response as the load current changes by 10X

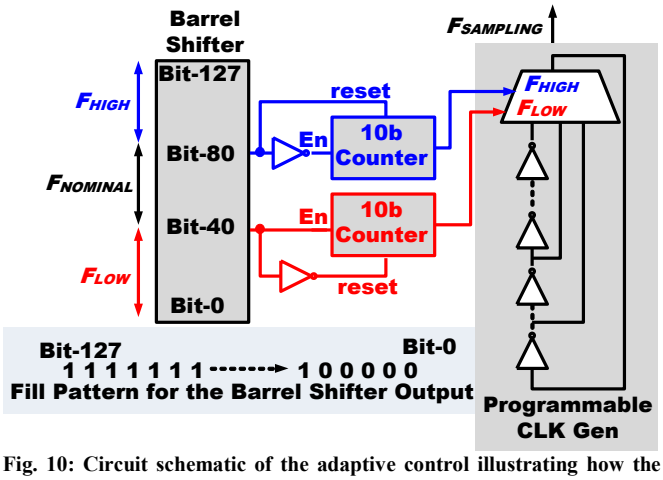


Fig. 10: Circuit schematic of the adaptive control illustrating how the barrel shifter output can be used to change the sampling frequency during runtime.

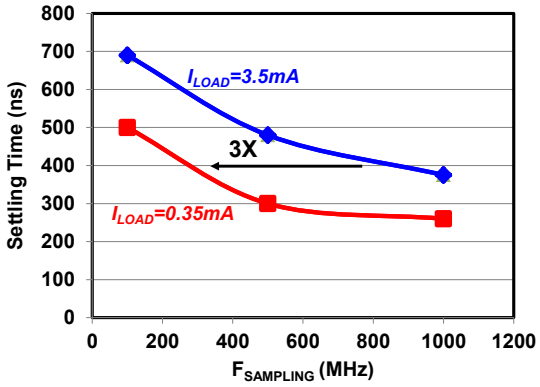


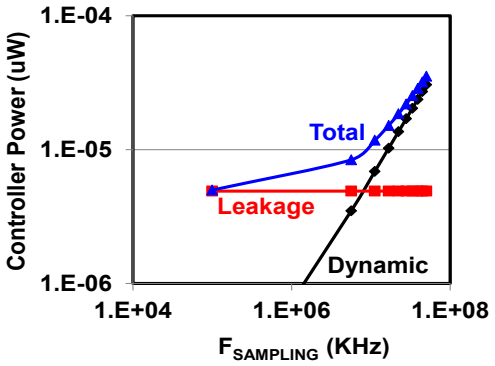
Fig. 11: Settling time as a function of the sampling frequency for two different load current conditions., It can be observed that as the load current decreases by 10X (i.e., load pole decreases by 10X), the same settling time can be obtained with 3X lower sampling frequency.

(from 3.5mA to 350uA). For a constant sampling frequency ($F_{SAMPLING}$) a stable under-damped system is realized when the output pole is at a higher frequency (corresponding to a load of 3.5mA). But as the bandwidth of the load decreases and the sampling frequency remains constant, the system becomes highly under-damped, oscillatory and can even become unstable.

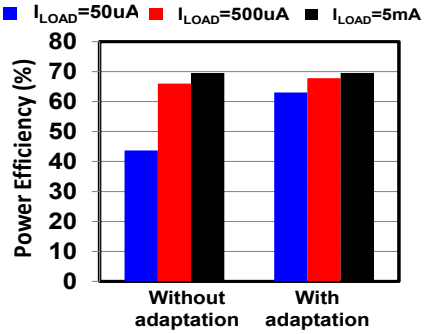
V. ADAPTIVE CONTROL FOR WIDE DYNAMIC RANGE

From the discussions so far, it is evident that the dynamic nature of digital load circuit necessitates an online adaptation of the control loop such that the closed loop system poles are constrained within bounds. In essence, as the output pole changes (movement in *a*), a truly adaptive control scheme [4] should be able to adjust the sampling period T, such that the z-domain open loop pole (e^{-aT}) remains invariant. Such fine-grained control is, of course, not energetically viable. Hence we propose a simple adaptation scheme, which instead of keeping e^{-aT} invariant will ensure that it is constrained within certain pre-defined bounds. A programmable ring-oscillator based CLK generator, capable of providing three CLK frequencies (F_{HIGH}, $F_{NOMINAL}$ and F_{LOW}) automatically selects one of the three sampling frequencies depending on the location of the output pole. The online adaptation scheme is described as follows.

It can be noted from Eq. (7) that the output pole is a function of the number of pull-up PMOSes that are ON. We can use this knowledge to predict if the frequency of output pole is below or above a predefined threshold. The circuit implementation of this adaptive controller logic has been shown in Fig. 10. We observe two specific bit locations of the barrel shifter (bit-40 and bit-80) and feed the output to two 10b counters. If bit-80 is '0' for a consecutive of 1024 cycles, then the counter output reaches all ones, indicating that for the last 1024 cycles the load current has been such that at least 80 pull-up devices were ON. In other words, the pole location, *a,* has moved to a higher frequency. In such a case, the output of the counter will trigger the CLK



(a)



(b)

Fig. 12: (a) Controller power as a function of the sampling CLK frequency showing the leakage component and a linearly increasing dynamic component. (b) Power efficiency of the adaptive controller illustrating that a severe loss of efficiency at lighter load conditions can be compensated for by employing adaptive loop control. The $F_{SAMPLING}$ corresponding to 50uA, 500uA and 5mA load currents are F_{LOW}, $F_{NOMINAL}$ (=3X F_{LOW}) and F_{HIGH} (=3X $F_{NOMINAL}$). The case of "no adaptation" illustrates the design for worst case load. The theoretical maximum for power efficiency is 70% (V_{OUT}=0.7V and V_{DD}=1V).

generator network to select a higher sampling frequency thereby constraining the z-domain pole (e^{-aT}) within a specific bound. In a very similar fashion, if bit-40 is '1' for at least 1024 cycles, indicating a light load condition, then the CLK generator network selects a lower sampling frequency, thereby preventing the system to become highly under-damped or even unstable. Averaging over 1024 cycles provides an estimate of the dc shift in the load (output pole) and by making this control loop more than 1000X slower than the LDO loop, we avoid any instability due to the interaction of the loops. In the current system we have three different sampling frequencies that are generated at ratios that are 3X of each other. Although the frequencies and the ratios can be programmable, in the current discussion the experimental results were obtained using F_{LOW}=33MHz, $F_{NOMINAL}$=100MHz and F_{HIGH}=300MHz. When a light load condition is detected, F_{LOW} is triggered and a heavy load corresponds to F_{HIGH}. This results in a consistent time domain response and prevents under-damping or limit cycle oscillations when the digital load goes to a low power state. This can be illustrated in the system behavior in response to a voltage noise on the supply. A measure of the transient response of the system is its settling time defined at the time required for the output to reach 90% of the stable value (Fig. 5). It can be seen in Fig. 11 that the settling time is a strong function of not only the sampling frequency but that of the load current as well. For example as the load current reduces by 10X, the sampling frequency needed for iso-settling time (400ns) is 3X smaller, which an adaptive control as described will be able to provide.

The biggest advantage of adaptive control in the digital loop is in increased power efficiency across the load range. A high sampling ratio (required for stability at a high load current) will cause unnecessary controller power to be dissipated at light loads and hence would lead to overall loss of power efficiency. Fig. 12a illustrates the different components of power dissipated in the controller and illustrates the fast increase in power with the sampling CLK frequency. Fig. 12b illustrates power efficiency for three different load conditions (covering a 100X current range) when no adaptation is employed and the sampling frequency is chosen for maximum load (worst case condition). In such a case, the efficiency drops to 42% in light load conditions as most of the power is dissipated in the CLKing circuits of the controller. However, if the adaptive control, as shown in Fig. 10 is employed and the three different load conditions are allowed to adaptively choose their own sampling frequencies, we can provide a better match between $F_{SAMPLING}$ and the output pole frequency. This results in higher efficiency at light load where $F_{SAMPLING}$ is reduced by 9X. Simulations reveal an efficiency increase of 50% in case of light load and 6% in case of nominal load conditions. Thus adaptive control can provide (a) a consistent time domain behavior in response to load changes and also (b) a higher overall power efficiency in discrete time digital LDOs supplying power to a wide dynamic range digital load.

VI. CONCLUSIONS

This paper presents the design and a comprehensive methodology for analyzing a gain programmable discrete time digital LDOs. We propose control models and demonstrate how adaptive control can be used for a consistent time domain behavior and higher overall power efficiency when such LDOs are used to power digital load circuits with wide dynamic range.

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