Asynchronous Design for New On-Chip Wide Dynamic Range Power Electronics

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***Abstract* – Asynchronous circuits will play an important role in microelectronic systems in the future, especially in energy harvesting and autonomous (EHA) systems where such circuits will be able to offer robustness and deliver high efficiency in a wide range of power-energy conditions. The concept of Capacitor Bank Block (CBB) mechanisms was proposed to form the basis of electronics for powering asynchronous loads. These mechanisms will benefit EHA systems by enabling effective co-scheduling of computational tasks and energy supply. This paper demonstrates how the CBB mechanisms can themselves be controlled by asynchronous circuits, thereby forming a new type of power delivery units (PDU) that will be able to deliver power to intelligent digital logic in future EHA systems. These PDUs are superior to traditional power converters largely because the latter can only regulate sufficiently high power and energy levels (regular and periodic) as well as their controllers require stable power levels themselves. This makes them unsuitable for intermittent and sporadic conditions inherent to EHA systems. In this paper, a novel asynchronous control for the CBB is described. Experiments and analysis of the new PDUs, comprising CBBs and asynchronous control, are presented and discussed in detail.**

Index Terms – Energy Harvesting, Power Electronics, Power Delivery Method, Asynchronous Control, Asynchronous Loads, Task and Power Scheduling, Voltage Threshold Sensing, Robustness.

I. Introduction

An important direction of future computation systems is to harness the capabilities provided by semiconductor scaling and new materials and technologies to provide low energy embedded services. EHA systems work on energy obtained from the environment, making zero-power operations possible [1][5][7]. The systems should start from zero energy and adjust working modes depending on the energy accumulation. More importantly, all parts of such a system should operate well under a wide dynamic range of such physical parameters as energy, power, and supply voltage.

The most recent research focuses on several scenarios for this type of systems, such as energy coming in regular, periodic, aperiodic, and intermittent patterns to explore how to build highly efficient, robustness systems, and make the systems more survivable in a wide voltage dynamic range [22]. High energy or power efficiency has two aspects. Power should be efficiently delivered to the computation load which should also make use of this power in an efficient manner. Survivability, on the other hand, also means that systems should be able to work in a complex environment, in particular not dying when one of the key physical parameters (e.g. voltage) becomes too low.

Normally synchronous circuits require a stable voltage level or a few discrete voltage levels to which corresponding clock frequencies can be set, for efficient operation. Asynchronous circuits [12] can work in a wide voltage range with potentially higher energy efficiency [6][8] and are robust under lower voltage. This could enlarge the survival zone of EHA systems into energy states where synchronous loads are not supported. However, existing power control such as switched capacitor DC-DC converters (SCC) focus on delivering a few stable Vdd values and require better input energy conditions.

CBB is a newly proposed type of power buffering method and starts working under energy conditions which SCC and other conventional power regulators could not handle. It delivers a wide range of voltage levels not limited to a few discrete values, based on the simple technique of storing energy on individual capacitors organized sequentially. With this flexibility, control is as important as in the case of the SCC, but because of the flexibility especially in not requiring absolute timing and clock, asynchronous control can be used, further reducing overheads.

In this paper, a set of CBB PDU implementation techniques is described. This method includes the CBB itself, sensors for charge condition feedback, and asynchronous controller design. Previously only the CBB concept and speculative studies existed in the literature and this work completes the CBB PDU method with realistic CBB, sensor, interface and control subsystem designs as well as experimental exploration.

The rest of the paper is organized as follows: Section II introduces the CBB concept and compares it with SCC. Section III describes the CBB PDU system design. Section IV describes the asynchronous control design in detail. Experimental results are given in Section V and the paper concludes with Section VI.

II. Capacitor Based Power Converters

With CMOS technology, on-chip capacitors have had higher Q and energy density and lower cost than on-chip inductors [2]. This led to recent efforts in exploring on-chip SCC such as [3] and [4]. Usually SCC has a fixed conversion topology, and outputs several fixed voltage levels. By tuning the switches, the output voltage can be changed between the fixed levels (stepping up and down).

In [6], a reconfigurable SCC is used to attempt regulating variable harvested power directly from a piezoelectric EH circuit. When harvested energy is abundant and varies in a

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small range, SCC provides loads with a high voltage level. However, it performs inefficiently and has to stop power delivery to accumulate enough energy, when harvested energy is sparse and varies in a large range. Moreover, for step-down power delivery, almost all switch states need to be changed to perform voltage conversions in each switching. This may cause high control overhead and energy loss.

In addition, before triggering voltage regulation, energy needs to be accumulated to a significant level. In this region, with current power buffering systems, the load cannot work.

Similar to SCC, an on-chip CBB connects to power inputs (e.g., EH) on the one side and computation loads on the other, and individual capacitors in the bank are charged from the source and discharged into the load during operation. With on-chip voltage sensing, the energy flow can be controlled. The CBB is designed to work similar to the SCC to power synchronous loads and to work in a wide Vdd range to power asynchronous loads [8][9]. This method has been predicted to become more common by [10]. The CBB shows obviously better abilities to cope with sparse energy with large variations and has potential as a platform on which a task and power scheduling method based on energy modulated computing [11] can be developed.

The concept of CBB was originally introduced in [6] but that work did not show the complete power delivery system based on CBB. This paper describes a complete CBB PDU system implementation method including its control and sensing and interface subsystems, as well as presenting asynchronous logic for the control and hybrid analogue and digital solutions in the system design. The block diagram of the system under discussion is shown in Figure 1.

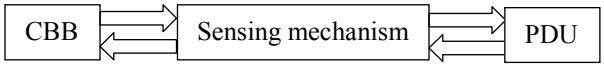

Figure 1. The block diagram of the proposed CBB.

III. Working Principle and HW Implementation

The operation of the CBB is based on charging a capacitor from power sources, and then discharging it over a load. Power delivery management can determine the capacitor value to use and the voltage range to charge and discharge at any time based on different load requirements and energy states. For urgent tasks, a high voltage level and small discharge range can maintain a high Vdd for the load. The CBB thus works very similarly to an SCC regulator to support fast task completion. When efficiency and power are priorities, a greater discharging range around a lower voltage point is more appropriate.

The control is the key to providing this type of operational versatility with a CBB PDU. It needs real-time sensing of charging and discharging and information on task scheduling.

Traditional ADC based sensing methods in synchronous systems uses either polling or interrupts to trigger subsequent actions. These ADCs typically need stable reference voltages [13] and are based on current mirrors and operational transconductance amplifiers (OTA) [14]. Unfortunately, generating reference and bias voltages may cause large energy consumption. And it may make the situation even worse in EHA systems where harvested power is very limited and unstable. Besides, in EHA systems, very high voltage conversion resolutions provided by ADCs may not be necessary and high resolution may usually mean large energy consumption and long conversion time [15].

The relatively low-resolution and simple control needed here make traditional controllers based on microcontrollers or FPGA solutions unattractive for power cost reasons. These also require stable working voltages which limits the survival zone [22]. Previously it was also found that when everything is organized by a global system clock, a microcontroller-based control cannot precisely regulate CBB charging and discharging anyway [24].

A. CBB block

Figure 2 shows a CBB structure extended to facilitate the choice of different capacitor values and different charging and discharging ranges. The example only has one power input and one power output without losing generality. It has n capacitor banks (CB). For each CB, it has one capacitor bank sense line (CBSL) used to connect the CB to voltage sensing circuits. Signals ChSwOn(n) and DsChSwOn(n) are used to control CBB charge and discharge respectively. Each CB(i) is designed to have one basic capacitor CapA(i,1) and it may have extra capacitors CapB(i,m) connected in parallel to the CapA(i,1) to raise the capacitance of the CB. The CapB(i,m) are switched by transmission gates (TG) and controlled by signal SW(i,m). For the value of n, and m (the number of CBs and sub-CBs), there is a trade-off in the power delivery flexibility and energy buffering ability versus chip area and fabrication costs.

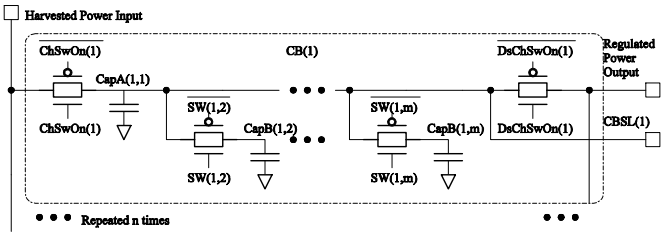

Figure 2. CBB with multiple capacitance values for each CB ($2 \leq n < \infty$ and $2 \leq m < \infty$, n and m are integers).

B. Sensing Mechanism and Interface

Figure 3 shows the CBB structure extended with interfaces to voltage sensors. Each CB in the CBB (A) has a CBSL connected to voltage sensing blocks for charge (B) and discharge (C). For (B) and (C), voltage threshold sensing circuits detecting fixed voltage levels are employed. The more thresholds can be sensed, the more flexibility in power delivery the CBB PDU will have. However, there is also a trade-off between power delivery flexibility and circuit area.

In (B), threshold sensing circuits are used during the charge process. The TGs inside (B) are controlled by signal ENA(x). When the threshold sensing circuit VthA(x) is selected by the PDU, the TG located between charge sense line (ChSL) and VthA(x) will be switched on by the ENA(x). The outputs of these threshold voltage sensing circuits SenOutA(1:n) are connected to an OR gate with n inputs. When the relevant threshold is reached, signal charge finish (ChFin) will be generated.

For voltage sensing during the charge process, when a CB is selected to be charged, the task and power scheduler will set the corresponding signal charge sense (ChSen) to High to switch

on the TG located between the CBSL of the CB and the ChSL. Therefore, the voltage level at the CB can be sensed by one of the threshold sensing circuits inside (B).

For voltage sensing in the discharge process, the same principle described above works in (C), which is constructed in the same way as (B).

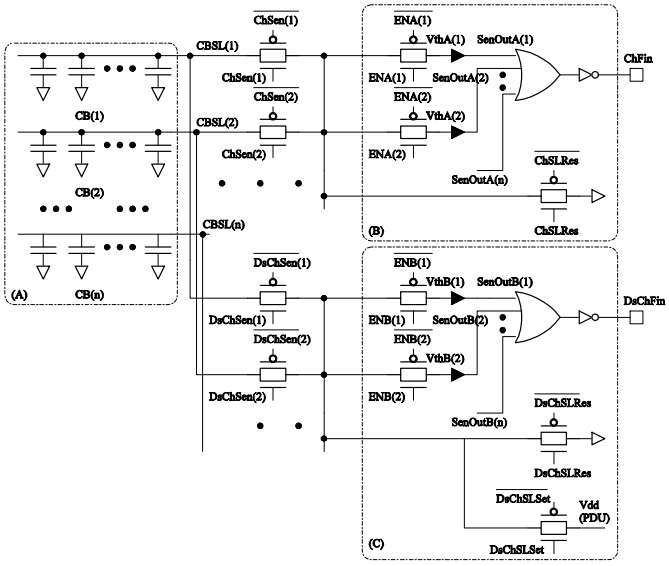

Figure 3. CBB interface to voltage sensing. (A) CBB block, (B) interface: voltage sensing block for charge, and (C) for discharge ($1 \leq x < \infty$, and $1 \leq y < \infty$, n, m, x and y are integers).

Signal ChSLRes resets ChSL, and signals DsChSLSet and DsChSLRes sets and resets DsChSL.

IV. Asynchronous Control Implementation

This section describes asynchronous controller and voltage sensing mechanism designs for the PDU.

A. Voltage Threshold Sensing Circuits

Because threshold voltage sensing circuits can be made to not require reference and bias voltages, they may consume less energy than normal ADC's and can be power-gated when not in use [16]. The threshold of such a circuit depends on the width and length of its transistors [17] [18].

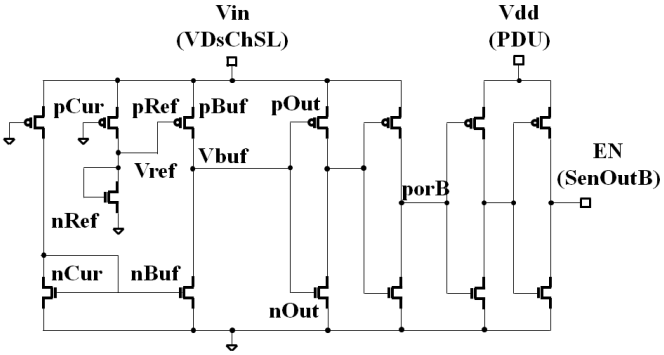

Figure 4. Voltage threshold sensing circuit employed for sensing falling voltage by CBB PDU.

Following [19], a voltage threshold sensing circuit is used to sense voltage (Vin) for the CBB discharge process here shown in Figure 4. A voltage divider consisting of transistors pRef and nRef is used to adjust its threshold. Two inverters are used here as a level shifter to transfer signals (portB) to the controller as an input of the controller. When the voltage of a sensed CB is higher than the preset threshold, the output of the circuit EN will be raised to High. When the voltage drops below the threshold, EN will be pulled down to GND.

For the CBB charge process the "memory effect" can lead to failure in highly frequent sensing rounds due to charges accumulated in the circuit. A sensor reset mechanism is therefore added to Figure 4 to reset Vref and Vbuf to GND before sensing in the charge threshold sensors.

These sensors are indicated by the black arrows in Figure 3. VthB(i) as Figure 4 and VthA(i) with added reset.

B. Asynchronous Controller Working with Tasks

CBB can work effectively with task scheduling [6]. Figure 5 shows a diagram of the CBB PDU (CBB, Interface, and asynchronous controller) structure to implement this. The controller contains CB Ch/DsCh control blocks, and one charging sequence control block and one discharging sequence control block for each CB. The CB Ch/DsCh control block controls charge and discharge of the CB through signals ChSwOn and DsChSwOn.

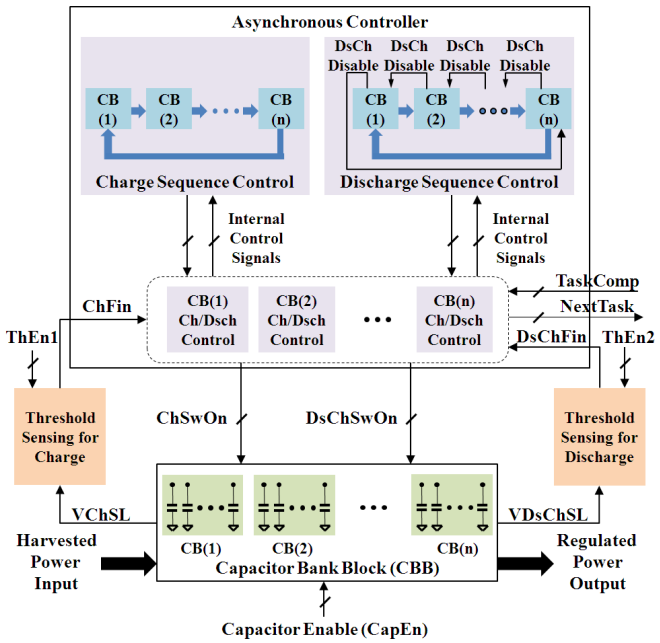

Figure 5. PDU with asynchronous controller, two voltage threshold sensing blocks and CBB, and taking task information as input.

A task and power scheduler (outside the scope of this paper) provides task-related inputs to the PDU including 1) ThEn1 and ThEn2 to control the CB charge and discharge range, 2) CapEn to adjust capacitance of a CB for buffering demanded energy, and 3) TaskComp to indicate the completion of the current task. In turn, the PDU sends out signal NextTask to request a new task when the present one has been completed.

The asynchronous controller is designed using the publicly available asynchronous synthesis tool Petrify [23]. An STG [25] model of the control is shown in Figure 6. In the model, there are two main control loops, one for charge control (A), and the other for discharge control (B) for each CB.

The charge control loop cannot start until SetDsChAv- is triggered by SetChAv- and DsChSwOn-. The discharge control loop cannot start until SetDsChAv+ is fired by ChSen- and NextPro-. This effectively enables the CBB PDU to avoid performing charge and discharge on any CB at the same time.

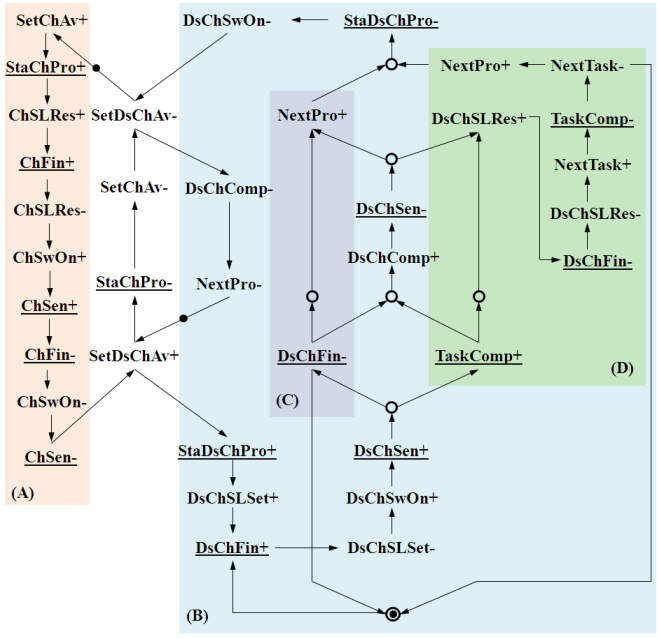

Figure 6. STG of CB Ch/DsCh control model (signal transitions with under line are inputs). (A) Charge loop. (B) Discharge loop. (C) Switching performed when low end of discharge range is reached. (D) Switching performed when present task is finished.

1) *Charge Loop Control*

In Figure 6 (A), after the CBB PDU initialization, all CBs are labeled available for charge (SetChAv+). Then charge sequence control block chooses one of CBs inside the CBB to start charge process (StaChPro+). Subsequent actions including control signal resets are needed before actual charging happens between (ChSwOn+) and (ChSwOn-) with voltage sensing when charging (ChSen+).

After completing the charge process, the CB will be labelled available for discharge (SetDsChAv+). The charge loop may be repeated after the CB is discharged (SetDsChAv-).

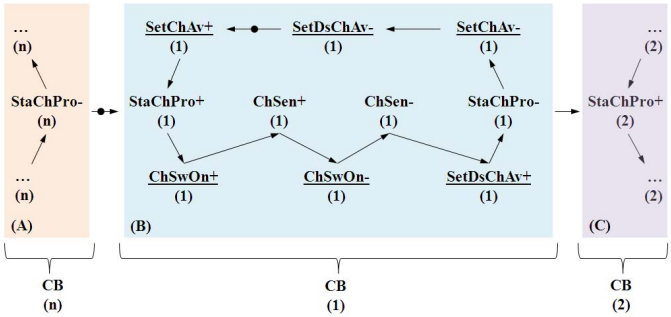

Figure 7. STG of charge sequence control model, (signal transitions with under line are inputs). For (A), (B) and (C), charge control loop for each CB is the same.

In the CB charge loop, ChSLRes+ is necessary because 1) the transition is used to reset the threshold sensing circuit to remove the memory effect, 2) it can be used to help the CB Ch/DsCh control block avoid Stuck at "0" faults for signal ChFin. When the target voltage level V_H is lower than the existing level, ChFin+ may never be fired, and 3) ChSLRes+ can prevent the sensing circuit from sensing failure caused by charges left on the ChSL after each threshold sensing.

CBs are charged sequentially and discretely (see STG of charge sequence control in Figure 7). The next CB becomes available for charging (StaChPro+(2)) only after the current CB has been charged (StaChPro-(1)).

2) *Discharge Loop Control*

In Figure 6 (B), when one of CBs inside the CBB is available to be discharged (SetDsChAv+), once the discharge sequence control block decides to perform discharge on the CB (StaDsChPro+), the discharge sequence on this CB can start.

DsChSLSet is a house keeping signal to avoid stuck at "0" faults on stale capacitors whose voltage may have leaked down to below the sensing threshold for discharge.

The actual discharge happens between DsChSwOn+ and DsChSwOn-. In order to prevent unnecessary CBB switching, the energy delivered to the load needs to be slightly more than demanded by a task. As a result, task computation may be completed before the voltage level at the CB reaches the low end of the discharge range. In this case, the controller will be informed of the completion of the present task (TaskComp+). Then the discharge sequence control block will be informed accordingly (DsChComp+), shown in Figure 6 (D), which covers part of the STG which deals with the relevant complications.

After completing the current task, the CB Ch/DsCh control block will request a new task (NextTask+) and inform the discharge sequence control block to prepare switching the loads to a charged CB to start a new task or maintain the computed data to wait for next task (NextPro+). The discharge loop may be repeated when the chosen CB is charged (SetDsChAv+).

Buffered energy is discharged from CBs sequentially and continuously over the load. Incorporating asynchronous handshake logic in the control helps avoid non-power gaps arising at the CBB output when CBB switching is performed. The discharge sequence control model is similar to the charge sequence model in Figure 7 with a more complex structure because there are more signals in Figure 6 (B) to control.

V. Experiments and Analysis

Based on the Petrify output the PDU controller design was optimized and then implemented in UMC 90nm CMOS technology using Cadence toolkits. MIM capacitors from the UMC 90nm library are used in the CBB. The CBB has three CBs and each CB has three sub capacitors (20 pF each). A stable voltage source 1.2 V is used as a power input for the CBB in the experiments. An RC circuit was used to emulate the load (1.5 KOhm, 1 pF).

A. *Power Consumption of Voltage Threshold Sensing*

For studying the sensors, the Vdd of the PDU is set at 1 V, assuming a small battery just to power the PDU and taking it out of the power drawn from the CBs to focus attention on the sensing circuits alone. The threshold sensors consume energy from the sensed CBs. The threshold sensing for charge starts when the voltage level at the CB is raised to 0.4 V. Until

threshold 1 V is sensed, the charge process is stopped. In the charge process from 0.4 V to 1 V, the power source totally delivers energy 28.7 pJ to the CB (60 pF) and the voltage sensing circuit for charge has drawn 0.33 pJ within 78 ns from the CB. After the charge process, discharge is performed from the charged CB and voltage sensing for discharge is enabled. When the threshold 0.4 V is sensed, the discharge is stopped. The sensing circuit for discharge has drawn 0.74 pJ within 66 ns from the CB. Therefore, the threshold sensing for charge and discharge in this case only consume 1.2% and 2.6% of the total energy coming from the power source.

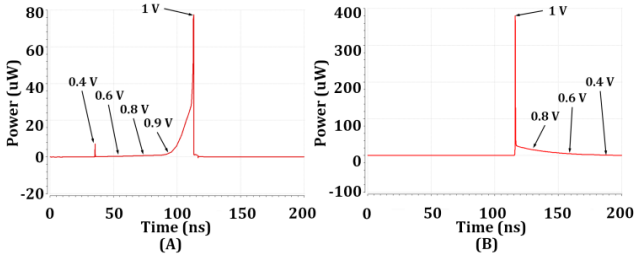

Figure 8. Power Consumption of threshold voltage sensing circuits for (A) charge (to 1 V) and (B) discharge (to 0.4 V) versus different voltage levels of CB.

The power consumption of the sensors and interfaces versus different voltage levels of the CB is shown in Figure 8. For threshold sensing in the charge process, the sensing circuit consumes very low power when the voltage at CB rises from 0.4 V to 0.9 V. Then the power goes high. When the threshold 1 V is sensed, its instant power jumps to around 75 uW. On the other hand, when the sensing circuit for discharge is connected to the CB, its instant power jumps to around 370 uW, then it drops significantly to 40 uW. From there the power of consumption of the circuit keeps to a very low level. The threshold sensors mainly switch when thresholds are crossed.

B. CBB PDU Working with Variable Vdd

In order to investigate the robustness of the asynchronous controller against voltage variation, the controller is powered with a Vdd varying in different ranges. The voltage waveforms of the PDU output are recorded and discussed.

- Experiment 1: PDU Vdd range higher than CBB charge/discharge range – Figure 9 (A), (B) and (C)

In Figure 9 (A), the PDU suffers light Vdd variation from 1.1 V to 1 V and the CBB works correctly and discharges power from 1 V to 0.4 V. Due to the intrinsic capacitance of the load, the high end of the discharge range is pulled down to 0.9 V. In (B), the PDU suffers medium Vdd variation from 1.1 V to 0.8 V. The performance of the CBB delivering power from 0.8 V to 0.4 V is still acceptable. In (C), the PDU suffers heavy Vdd variation form 1.1 V to 0.6 V. the controller is getting slower along with the voltage dropping and the signal transition speed inside the asynchronous controller varies largely caused by the serious and rapid Vdd variation. Theoretically, the charge and discharge switches cannot be controlled in time. Therefore working with heavy Vdd variation, it is hard for CBB PDU to regulate output power. However, the power delivered to the load is still continuous without stops. It shows the CBB and controller are robustness to voltage variations.

- Experiment 2: PDU Vdd variation range overlapping CBB discharge range – Figure 9 (D), (E) and (F)

In Figure 9 (D) there is a small overlapping between the PDU Vdd variation range (from 1.1 V to 0.8 V) and CBB voltage range (from 1 V to 0.4 V). The CBB PDU works correctly and is able to regulated power. In (E), there is a medium overlapping between the Vdd variation range (from 1.1 V to 0.6 V) and regulated power range (1.1 to 0.4 V). The CBB PDU shows weak power regulating ability. However, the power delivery is still continuous without stops. In (F) since the regulated power has the same variation range as that of Vdd, the CBB PDU fails to regulate output power due to various signal transitions inside of the asynchronous controller and not fully open or closed TGs in the CBB (working in low Vdd such as 0.4 V). However the signal transitions inside the controller, which works with low Vdd 0.4 V, are still correct. Although the CBB PDU is not good at working with Vdd that varies seriously and rapidly, it still shows a certain degree of Vdd variation tolerance.

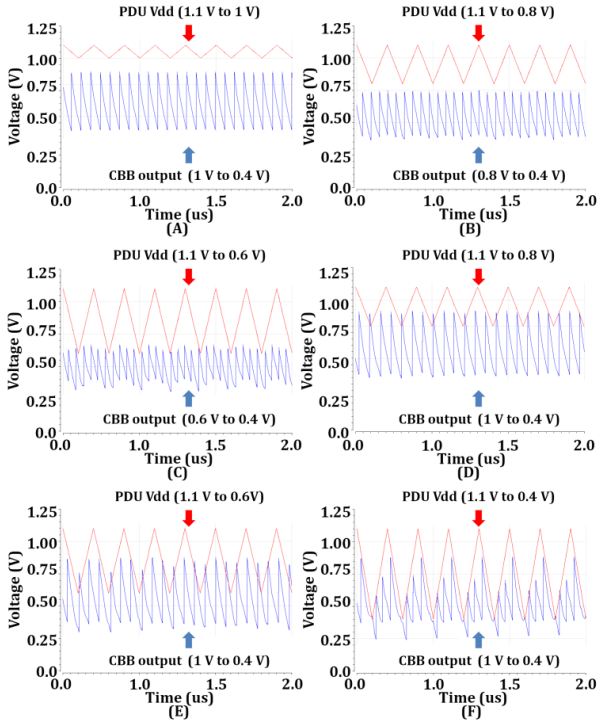

Figure 9. CBB PDU working with Variable Vdd.

C. Power Consumption of CBB PDU

According to recent literature, the switching frequency of on-chip SCC designs is mainly in a range approximately from 100 KHz to 15 MHz [20] except [21] that is implemented with 45 nm CMOS technology and employs 30 MHz switching frequency. However, the CBB PDU may not need to achieve switching speed as fast as SCCs in order to minimize voltage ripples at the output, as it is designed to power asynchronous loads or other loads with good voltage variation tolerance.

Figure 10 shows the CBB PDU average power consumption versus CBB switching frequency working with 1V Vdd. For example at 4.0 MHz, the controller consumes about 5 uW, and at 37 MHz about 25 uW. This average power consumption includes the power consumed by the controller, voltage shifting

from sensing circuits to the controller, and TGs inside the CBB. In the simulation, the CBB PDU, discharging energy from 1V to 0.4V, is able to deliver output power from 77 uW (switching at 4 MHz) to 565 uW (37 MHz) to the asynchronous loads. Only 4% – 7% of the total power delivered to the load is consumed by the PDU. If the PDU employs shorter discharge ranges starting from 1V, the output power will be higher, as a longer discharge range from 1V provides lower average output voltage than a shorter discharge range from 1V.

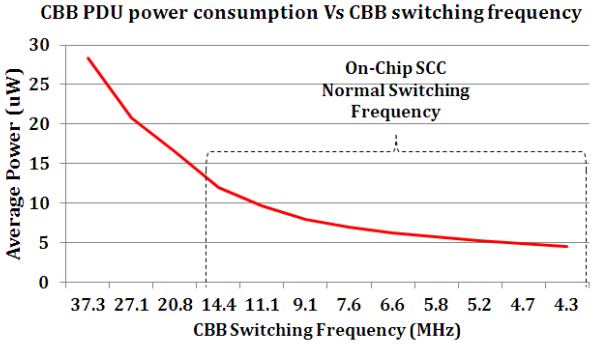

Figure 10. CBB PDU power consumption Vs CBB switching frequency working with 1 V Vdd.

VI. Conclusions and Future Work

This paper describes an on-chip power buffering and delivery system based on the CBB technique. Such a PDU is capable of delivering power to the load with a large range of variable but programmable voltages, depending on the load needs and the energy source conditions. This flexible and efficient delivery potentially allows loads to start working under much worse energy availability states than previously, and is especially suitable for supporting asynchronous or other types of loads which are capable of making effective use of a wide Vdd range.

In order for this flexible energy management to become a reality efficient control of the CBB PDU operation is needed. To this end this paper describes design techniques which allow the realization of efficient sensing and its necessary interfacing to the control, and also the control circuits themselves.

By using asynchronous and analogue techniques wherever appropriate a highly robust and efficient design is obtained for the overall system. Different from traditional asynchronous circuit design, the controller and supporting interfaces blend digital with analogue. The design process may benefit future research as it starts to break the mold of intelligent but inefficient digital and efficient but simplistic analogue. For example, asynchronous SRAM which uses self-timed circuits for reading/writing control shows more intelligence, and efficiency [8] compared to the conventional digital/analog control mechanism.

The system implementation is studied through a sequence of experiments. The results obtained demonstrate the robustness and efficiency of the overall method and the implementation qualitatively and quantitatively. The sensing circuits and the controller have very low overheads and work in a widely variable environment. The system can start buffering power and supporting load operations under severe input energy shortage. This shows that CBB coupled with asynchronous or other robust loads could potentially extend the survival zone.

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