Electromigration-Aware and IR-Drop Avoidance Routing in Analog Multiport Terminal Structures

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***Abstract*— This paper describes an electromigration-aware and IR-Drop avoidance routing approach considering multiport multiterminal (MP/MT) signal nets of analog integrated circuits (IC). The effects of current densities and temperature in the interconnects may cause the malfunction/failure of a circuit due to IR-Drop or electromigration (EM). These become increasingly more relevant with the ongoing reduction of circuit sizes caused by the evolution of the nanoscale integration processes. Therefore, EM and IR-Drop effects must be taken into account in the design of both power networks and signal wires of analog and mixed-signal ICs, to make their impact on the circuits' reliability negligible. In previous EM and IR-Drop-aware analog IC routing approaches, 'dot-models' are assumed for the terminals, i.e., each terminal has only one port that need to be routed, however, in practice, analog standard cells usually contain multiple electrically-equivalent locations, often distributed over different fabrications layers, where legal connections can be made, i.e., MP terminals, which need to be properly explored. The design flow is detailed, and the applicability of the approach is demonstrated with experimental results, and also, by generating the routing of an analog circuit structure for the UMC 130nm design process.**

I. INTRODUCTION

Analog and mixed-signal (AMS) ICs suffer from diverse non-idealities that became increasingly more relevant with the ongoing reduction of the circuit sizes in the last years, and may cause catastrophic circuit failures. These must be taken into account during the circuit design in order to mitigate their effect on the product reliability [1]. Two of them are: EM [2], which refers to the material migration in the power networks and signal wires that are stressed with high current densities, affecting interconnection lifetime; and, IR-Drop, that consists of a fluctuation of the net voltage due to the increase of the interconnects resistance, affecting circuit behavior and performance [3][4]. Previous works focused essentially on how to deal with the multitude of current densities observed in AMS circuits, and, how to assign the interconnects and expand the widths accordingly in the routing step of the layout generation. This problem is often divided into wiring planning (WP), that determines the tree with the flow of currents between terminals, and wire routing, that rectilinearizes the paths.

In the first AMS current-driven solution [5, 6], a Steiner tree for a set of single-port (SP) sources/sinks with different current densities was constructed in a semi-automatic manner, based on local choices to add the nearest terminal to the current sub-tree. In [7] a current-driven wiring topology (WT) is extracted by greedily assigning the source-sink edges that maximize the interconnect area gain and satisfy a set of IR-Drop constraints. In [8] an integer linear programming-based algorithm is proposed, however, the computational time is prohibitive. In [9] a WT for analog high current application is obtained by separating the single-port multiterminal (SP/MT) into small clusters that are routed by an exhaustive procedure. In [10] the original NP-hard problem is converted to a class P problem via the proof of the greedy-choice property, this way, the competition among the flow of all sources is considered in the WP, unlike all the previous approaches. Finally, in [11], channel space restrictions are considered, in which wider paths avoid narrow channels in the construction of the WT.

In all the reviewed approaches, the terminals of the signal nets have only one port that can be routed, i.e., SP/MT nets, which simplify the problem. While SP cells may be suitable in digital or at system-levels of AMS circuits, where the terminals of the macro-cells are usually located at higher layers of the manufacturing process, at analog cell-level they degrade the quality of the solutions, since most of the device's ports are located in lower layers, and a complicated terminal geometry can easily have tens of ports located on multiple fabrication layers. The use of an automatic MP approach greatly increases the flexibility of the devices' placement in any orientation. In Fig. 1, two folded CMOS transistors in a common-centeroid layout style are presented, each terminal has multiple ports that should to be considered to increase the routing efficiency. For the approaches considering only WP or path assignment abstractly from the silicon level [7–11], simplistic 'dot-models' are used to represent these complex multilayer MP terminal structures. In the semi-automatic approach for EM-reliable layouts [5, 6], the exact location of the SPs may be either defined in the generation of the modules or selected manually, which lead to higher setup times and/or sub-optimal solutions.

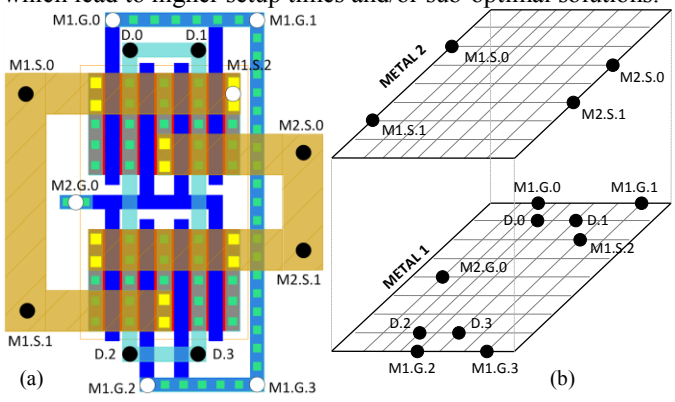

Fig. 1. (a) Two folded transistors, M1 and M2, in a common-centeroid layout style with multiple electrically-equivalent ports: (S)ource, (D)rain and (G)ate. (b) Transversal view of the terminals ports' location, for the 2 layers used.

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This paper presents a new EM-aware and IR-drop avoidance methodology for automatic generation of analog IC layouts. A current is attached to each of the terminals, then, a MP/MT routing procedure is used to compute the interconnects currents and find the shortest paths, considering every port available in the terminal, which further increases the complexity of the NP-complete Steiner problem [12]. As the best of our knowledge, this is the first dedicated analog routing approach considering MP/MT signal nets.

This paper is organized as follows. In Section II, the proposed design flow is sketched. Afterwards, in Section III the generation of the WT is briefly covered, and, in Section IV the selection of the MPs is detailed. In Section V, the methods for the assignment of the Steiner-points are provided, and, in Section VI, the calculation of the EM/IR-drop aware wire width is described. The experimental results are described in Section VII, and, the conclusions are addressed in Section VIII.

II. Design Flow

The developed MP/MT EM- and IR-Drop-aware routing methodology was embedded on an in-house analog IC design automation environment, AIDA [13], which implements a design flow from a circuit-level specification to a layout description, and is presented in Fig. 2. During the circuit-level synthesis, the tool preforms a layout-aware optimization, and also, considers corner analysis together with circuit simulator as the evaluation engine, fundamental for high accuracy. The currents for each terminal are automatically extracted in this process, and then, the layout is generated using the Layout Generator [14]. In the Placer module, each device in the flooplan is instantiated with multiple electrically-equivalent ports for each terminal, the number of ports and effective locations are defined in the Module Generator.

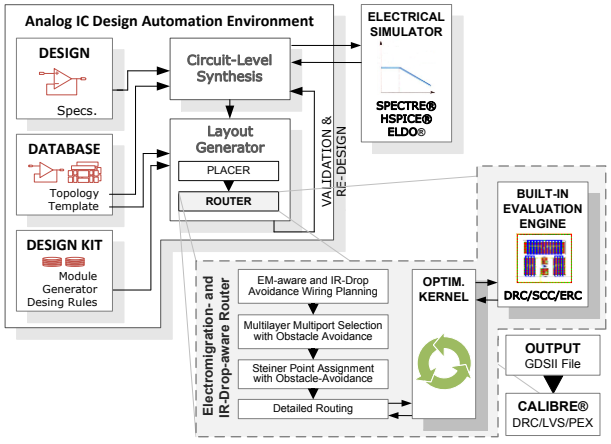

Fig. 2. EM/IR drop-aware design flow embedded in the layout generator.

The traditional problem in an EM- and IR-Drop-aware Router is to assign the paths and expand the wires' widths according to the current densities imposed on them, while minimizing the wiring area. If the WT is computed without current considerations, assigning currents only in the detailed routing, will lead to very sub-optimal solutions in terms of total wire area, and further, expanding the interconnect widths may even result in unfeasible solutions, which will lead to re-design cycles and iterations over the already routed nets. Our Router is divided into 4 different phases, in the first it is performed the EM- and IR-Drop-aware WP, i.e., starting from a netlist and a set of current-sources/current-sinks the current-correct tree that provides the terminal-to-terminal connectivity and minimizes the wire area is formulated. After, each terminal-to-terminal connection is transformed into a rectilinear path and the MPs selected are those that minimize the wire area, and then, the Steiner points are assigned to overlap sections of adjacent paths. The width of the interconnects is then calculated taking into account the EM/IR drop effects. A last step of detailed routing [14] is required to ensure design-rule-correctness of the previous phases.

III. Wiring Planning (WP)

Given a set of k terminals $\{T_1, T_2, \ldots, T_k\}$ of a net, where m terminals are current-sources, indicated by the positive current value attached, and n are current-sinks, in opposition, indicated by the negative current value, the WP objective is to construct the tree that minimizes the total wire area of the net:

$$\sum_{i=1}^{n}\sum_{j=1}^{m} l_{ij} \times w_{ij} \qquad (1)$$

where l_{ij} is the length and w_{ij} the width of the wire ij. The current I_{ij} is used instead of the wire's width while computing the WP, due to its proportionality. Further, the tree topology must be constructed while satisfying the Kirchhoff's current laws in every terminal. Recovering the example from [6] that considers a set of 7 terminals of the same net, where T_1, T_4 and T_5 are defined as current-sources and T_2, T_3, T_6 and T_7 as current-sinks. The normalized current values $\{I_1, I_2, \ldots, I_7\}$ are $\{+7, -8, -4, +3, +9, -5, -2\}$ and are marked at the center of the MP terminals in Fig. 3 (a). Each of the terminals was transformed into a four port quadrangular terminal geometry, but any other multilayer MP geometry could be defined.

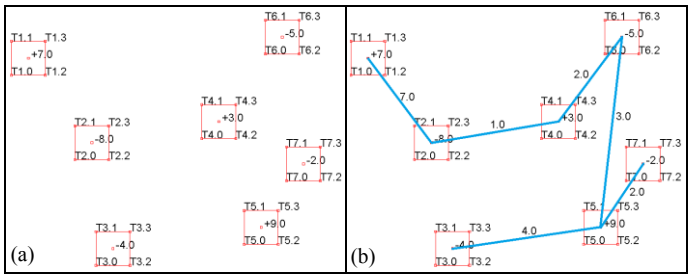

Fig. 3. (a) Topology with multiport terminals and attached current vectors, $T_1(+7)$, $T_2(-8)$, $T_3(-4)$, $T_4(+3)$, $T_5(+9)$, $T_6(-5)$ and $T_7(-2)$. The number after the terminal's designation is the port's index. (b) EM-aware wiring topology, i.e., terminal-to-terminal connectivity and current densities for each connection.

From the EM-aware WP approaches found in the state-of-the-art, WiT [10] proved to outperform the topologies of the previous implementations both in terms of minimizing the total wire area, as in the computational time required to achieve the solutions, for any range of SP terminals. The approach is based on the proof of the greedy-choice property, i.e., only current from sources to sinks is considered, source-to-source or sink-to-sink flow is not supported. Due to this property, the current assignment problem can be strongly simplified and dealt as a class P problem instead of NP-hard. This approach also allows the inclusion of IR-Drop constraints in the construction of the

WT. The terminal-to-terminal connectivity and flows of the optimal WT are determined in WiT using the multilayer geometrical center of the terminals' ports, Fig. 3 (b).

IV. Multilayer Multiport Selection with Obstacle-Avoidance

An automatic Router should be able to connect all terminals of a net without the intervention of the designer, for this, it must be aware of all the possible locations where the MPs of a terminal might be. There are two different approaches for the problem of routing MP/MT nets [12]: the weak-connectivity version, where only one port of each terminal is routed and all the connections are made to generate a single tree, Fig. 4 (a); and the strong-connectivity version, which allows the use of intra-group connections along with the use of optional Steiner points, assuming that all ports of a group are connected internally, Fig. 4 (b). In the last one, the result is a forest of trees, and this is the approach considered for the proposed Router, due to the MP nature of the generated modules (Fig. 1).

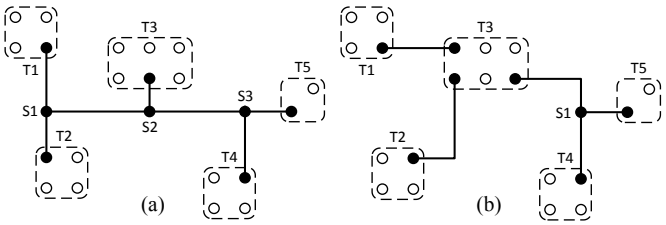

Fig. 4. MP/MT nets, each set of points within the same boundary represent the available ports of a terminal T_i, a point out of any boundary represents a Steiner S_j; (a) weak-connectivity and (b) strong-connectivity solution [12].

A. Multilayer Multiport Obstacle-Aware Grid

Before selecting the appropriate ports for the terminal-to-terminal connectivity obtained from the WP, it is necessary to construct a multilayer rectilinear grid for the problem, which consists of a directed graph considering 3-dimensional vertices. The device's structures are ignored during the grid construction, only the port locations and obstacles locations (which may be located inside device's structures) are of concern. The generic terminal T_1 consisting of 4 distinct ports all located in the same manufacturing layer, will be used to illustrate the implemented methods. Assume that all ports $\{T_{1.0}, T_{1.1}, T_{1.2}, T_{1.3}\}$ are electrically-equivalent locations for the same terminal, e.g., a transistor drain.

Initially, each of the terminal's ports is extended to each of the fabrication layers considered, as presented in Fig. 5 (a), vias are used to represent the connection between of two vertices in different layers. If an obstacle blocks the extension of a port to another layer, that vertex is not instantiated, nor the resulting extensions to the layers above or below that one, as depicted in port $T_{1.3}$. The same method is used to extend the corners of each obstacle to each different layer, and instantiate the subsequent possible vertices in locations not blocked by other obstacles, Fig. 5 (b). The process of extending ports and obstacles' corners is performed simultaneously, and the result is the main set of available vertices in each layer, Fig. 5 (c). After having all vertices for each different layer assigned, a vertical and horizontal line is passed through each vertex, i.e., through ports, extended ports, obstacles' corners and extended obstacles' corners. The intersections of those lines define the remaining vertices of the graph, Fig. 5 (d). Finally, for each vertex the rectilinear neighbors are assigned, i.e., the edges of the graph, with a cost obtained from (2), where (x_i, y_i) is the source vertex of the segment, (x_j, y_j) the sink vertex of the segment, the z-axis is reserved for shifts between conductor layers, i.e., vias, where z_j is the destination layer and z_i the source layer, and V_{cost} stands for the cost of assigning a via.

$$l_i = |x_i - x_j| + |y_i - y_j| + |z_i - z_j| \times V_{\text{cost}} \quad (2)$$

Each vertex may have a maximum of 6 neighbors, i.e., a neighbor at left, right, above or below in the same manufacturing layer, and neighbor in the exact (x, y) coordinates but located one layer above (x, y, z+1) or one layer below (x, y, z-1). For each neighbor assigned in a different layer, a via is required. When all the possible neighbors are assigned, the final custom grid is achieved, Fig. 5 (e).

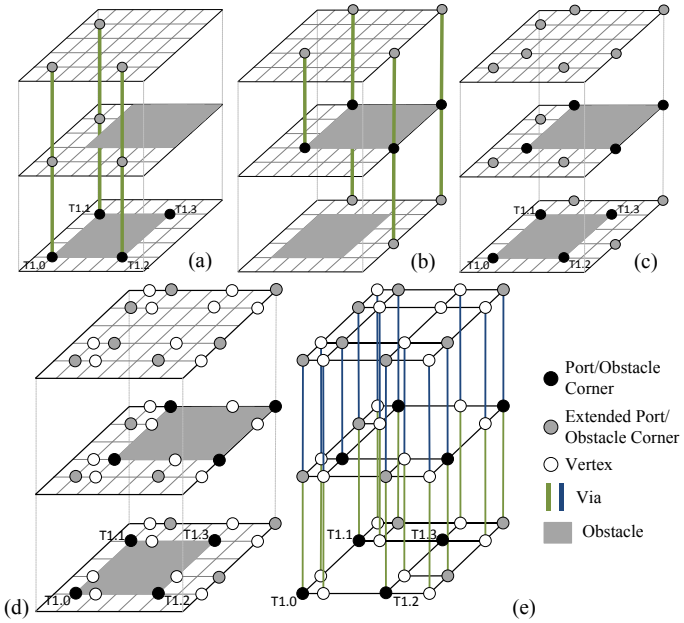

Fig. 5. Example with one MP structure and two obstacles (one located inside the MP structure), 3 fabrication layers considered. (a) Each port of a terminal and (b) each corner of an obstacle are extended to each layer. (c) Steps (a) and (b). (d) Horizontal and vertical lines are passed through each vertex, which originate the remaining vertices. (e) The assignment of rectilinear neighbors to each vertex results in a custom grid for the current ports and obstacles.

B. Multilayer Multiport Selection

To select the best ports to be connected, we propose a variation of the A* search algorithm, where all possible routes from all start ports to all end ports are explored simultaneously. By expanding all the routes simultaneously, the number of nodes explored is reduced, as only the best route will be totally explored. The modified A* search pseudo code is presented in algorithm 1, where the cost for leaf *l* in the path to terminal port Te_j is given by (3), where the *pathCost(i, j)* is the real path size from the start terminal port to node *i* found in the way to the end terminal port j, and the heuristic, *dist(i, j)*, is the Manhattan distance between nodes *i* and *j*.

$$ct(l, Te_j) = pathCost(l, Te_j) + dist(l, Te_j) \quad (3)$$

Fig. 6 illustrates the execution of the shortest path search between terminal T1, with 4 ports, and terminal T2, with only

one port (for clarity). Where Fig. 6 (a) shows the grid, the vertices and the slant edges mark the possible connections between T1 and T2. Fig. 6 (b) shows the expansion of nodes during the search. First, node T1.3 is expanded because the dist(T1.3, T2.0) is the smallest, but the path is blocked, and while going around the obstacle, T1.1 becomes the node closer to T2.0 and starts to be explored leading to the final path. T1.0 and T2.0 were not explored. Fig. 6 (c) highlights the selected path connecting T1.1 to T2.0. The efficiency of this approach can be seen in this simple example, where only 13 nodes were explored, and some of the ports of T1, were not even explored. In networks this small, it is really of no importance, but for larger networks with many obstacles and ports per terminal the savings are relevant.

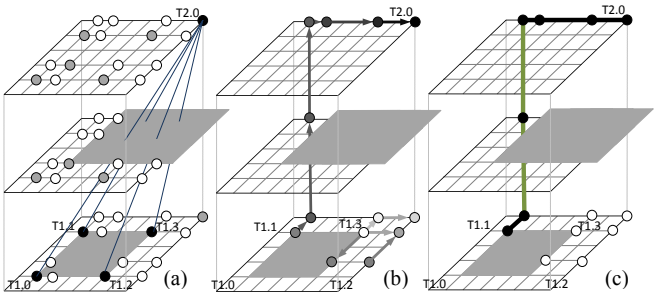

Fig. 6. Example of the parallel A* search: (a) Grid for a 4 to 1 connection example (b) A* expansion of nodes (ordered from lighter to darker) (c) Nodes in the path (darker) and explored nodes not in the shorter path (lighter).

The MP selection is executed for all edges in the MST obtained from the WP to construct the port-to-port optimal rectilinear forest. By considering multilayer and obstacle-avoidance a great reduction on the required wiring length is achieved, while simultaneously assigning the rectilinear paths, which are obtained from the multilayer MP rectilinear obstacle-aware grid.

V. Steiner Point Assignment

With the port-to-port optimal rectilinear forest done, it is possible to assign Steiner points that will reduce the total wire area by considering two directed edges at a time. Some heuristics are used to determine the optimal Steiner point location on the grid, which maximize the edges' overlap. There are two distinct situations: if a common source connects two different sinks (ports or previously assigned Steiner) located in the same quadrant or adjacent quadrants, as depicted in Fig. 7; or if two different sources located in the same quadrant or adjacent quadrants connect to the same destination. If the requirements are satisfied, then, the two edges can be divided into three different edges and a Steiner point, on which one of the new edges corresponds to the overlapped area of the flows f_i and f_j. However, if the optimal Steiner location overlaps an obstacle the simple assignment is impossible. The proposed solution is to generate, at most, 6 possible Steiner locations: 4 correspond to points assigned in the same manufacturing layer, i.e., on left, right, above and below of the obstacle obstructing the Steiner assignment; and 2 correspond to the points in the exact (x, y) coordinates of the optimal Steiner point, but located one layer above (x, y, z+1) or one layer below (x, y, z-1), if possible, as presented in Fig. 8 (a). The paths through all the possible Steiner points are computed and the shortest path, i.e., three edges and the Steiner point, is selected. If two paths have the same wirelength, the preferred path is the one that maximizes the overlapped length between f_i and f_j

Algorithm 1 Multiport Selection

input: Terminal *A*, Terminal *B*, **List**<Nodes> *grid*

```
1.  Queue queue := empty //empty set ordered by cost
2.  for(Port pa in A) do
3.      for(Port pb in B) do                    // add one entry for the
4.          queue.add(new QueueEntry(           // path between each
5.              grid.getNodeLocatedAt(pa),      // start port to each
6.              grid.getNodeLocatedAt(pb)))     // end port
7.      for(Node n in grid) do
8.          n.pathCostOnTheWayTo(               //initialize node cost
9.              grid.getNodeLocatedAt(pb)) := POS_INFINITE
10. while(queue.isNotEmpty()) do
11.     node u := queue.remove()
12.     if(u is endNode) return backtrackPathTo(u)
13.     for(Node v in n.neighbours) do
14.         tentativeCost = u.pathCost + dist(u,v)
15.         if(v.pathOnTheWayTo(u.end) > tentativeCost)
16.             v.pathOnTheWayTo(u.end) := tentativeCost
17.             queue.add(new QueueEntry(v,u.end)) //pass the end port
                                                   //to evaluate the cost
18. return null //no path found
```

For the Steiner points of Fig. 8 (a), the paths that minimize the wirelength are presented in Fig. 8 (b)-(d). From the solutions, there is a tradeoff between the V_{cost} of assigning a via and the path that is selected. If (V_{cost} < 1) the preferred path is the one in Fig. 8 (b), that requires three vias in order to avoid the obstacle. If (V_{cost} > 1) one of the paths (c) or (d) is selected, since both the paths' length and total overlapped length are the same. The output of the MP selection and Steiner point assignment procedures is illustrated in Fig. 9, for the port-to-port optimal rectilinear forest of Fig. 3 (b), considering 4 rectangular obstacles shown in gray.

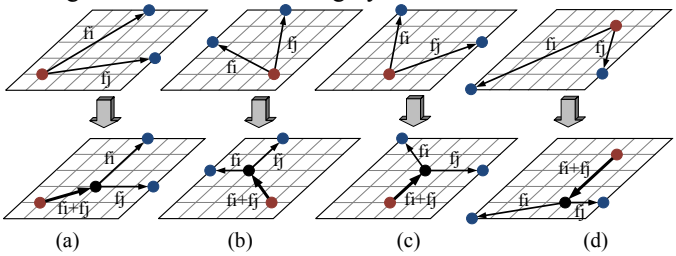

Fig. 7. Two edges with common source and different sinks: (a)(b) the two sinks are in the same quadrant (c)(d) the two sinks are in adjacent quadrants.

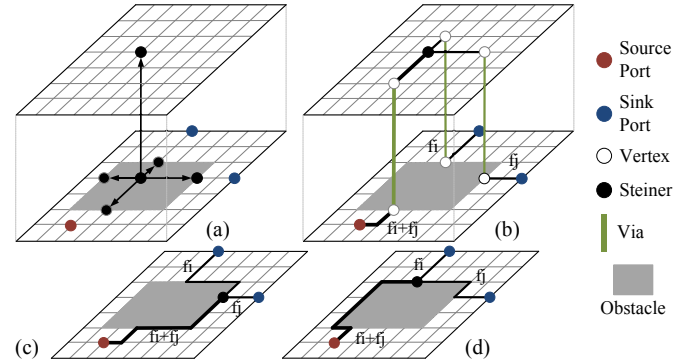

Fig. 8. The optimal Steiner location is impossible to assign: (a) New Steiner points, 5 available. (b) Path length: 12 + 3*V_{cost}, overlapped: 4 + 1*V_{cost}, (c) Path length: 15, overlapped: 7, (d) Path length: 15, overlapped: 7.

VI. EM AND IR-DROP-AWARE INTERCONNECT WIDTH

The effective wire's width w that satisfies the EM for the root mean square current I_{eq} assigned to the interconnect in the WP, is computed during the detailed routing step using (4), where, $J_{max}(T_{ref})$ and $h_{process}$ are constants tabulated for the technology design process. $J_{max}(T_{ref})$ is the maximum allowed current density for the reference temperature, T_{ref}, used in the determination of I_{eq}; and $h_{process}$ the nominal layer height. Summarizing, a higher temperature for the same current density I_{eq} will require an increase in the interconnect's width in order to maintain the same median time to failure [2, 3].

$$w_{EM} = \frac{I_{eq}}{J_{\max}(T_{ref}).h_{process}} \quad (4)$$

However, while the EM constraint may be fulfilled, due to the inherent resistance of the interconnects, undesirable voltage drops across the networks are still possible. The inequality in (5) determines the maximum assignable length l_{max} for a interconnect (source to sink), in respect to a fixed maximum tolerable IR-drop voltage V_{max}, which provides a safe length margin to reduce voltage drops, where $r_0(T_{ref})$ is the conductor sheet resistance [7].

$$l_{eff} \le l_{max} \sim \frac{V_{max}.w_{EM}}{I_{eq}.r_0(T_{ref})} \quad (5)$$

This way, to reduce the IR-drop effect is required that the lenght of the IR-drop-sensitive lines is kept as short as possible, this is ensured both in the implemented WP as in the path finding algorithm, that searches for the shortest paths available in the MP floorplan. However, if the effective length l_{eff} of the assigned path still surpasses l_{max}, the wire must be re-widened according to (6) to decrease the resistance of the conductor per unit square.

$$w_{IRdrop} = \frac{I_{eq}.l_{eff}.r_0(T_{ref})}{V_{max}} \quad (6)$$

When both w_{EM} and w_{IRdrop} values lead to an effective wire width w_{eff} below the minimum width manufacturable, $w_{min\_process}$, this value is used instead, as summarized in (7).

$$w_{eff} = \max\{w_{EM}, w_{IRdrop}, w_{min\_process}\} \quad (7)$$

VII. EXPERIMENTAL RESULTS

The framework of the proposed methodology has been coded in JAVA and is running on an Intel® Core™ i7-3610 CPU 2.3 GHz with 8 GB of RAM.

A. Benchmark

A set of 8 test cases were adopted, where one is the example of Fig. 3 and the other 7 are randomly generated examples, with the number of terminals ranging from 7 to 100, and for the test cases including MP terminals, the number of ports ranging from 2 to 16, as detailed in Table I. Balanced positive/negative current values were injected in order to satisfy the Kirchhoff's current laws.

Due to the total inexistence of MP analog routing approaches in the state-of-the-art, and furthermore, considering EM, a comparison with similar tools is not possible. To use the existent SP EM-aware routers in the proposed MP test cases would require the introduction of expert knowledge in the setup process, particularly to select the most appropriated port among the available ports. Since in the current test cases a terminal geometry has any number of ports in random dispositions, and also, on different fabrication layers, the approach taken was to transform each MP structure in a SP structure, by randomly fixing one of the ports, and block the access to the remaining. As it can be seen by the similarities in the wiring topologies obtained for both the SP and MP runs, WP is relatively independent of the MP problem, validating the usage of the geometrical center of the terminal's ports in the MP case. However, by taking advantage of the MP an average reduction of 25% in the rectilinear wire area is achieved, without a significantly increase in the execution time, given the efficiency of the path finding algorithm implemented.

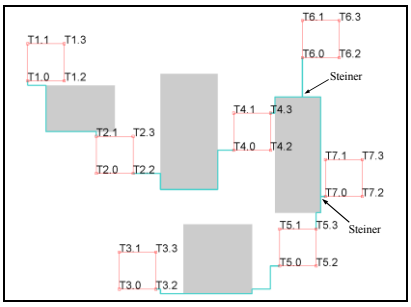

Fig. 9. Multiport selection and Steiner points assigned for the multiport topology of Fig. 3 (b), considering 4 obstacles.

TABLE I. EXPERIMENTAL RESULTS FOR THE SP VS. MP ROUTING APPROACH

Test Case		TC7	TC10	TC15	TC25	TC35	TC50	TC75	TC100
#Terminals		7	10	15	25	35	50	75	100
#Sources / #Sinks		3 / 4	4 / 6	7 / 8	14 / 11	18 / 17	23 / 27	29 / 46	55 / 45
#Ports[1]		[4]	[2-6]	[2-8]	[2-8]	[2-16]	[2-16]	[2-16]	[2-16]
#Obstacles		4	5	6	10	15	15	20	75
#Layers / V_{cost}[2]		4 / 5	4 / 5	4 / 5	4 / 5	4 / 5	4 / 5	4 / 5	4 / 5
SP / MT	SP EA-WT[3]	-	29844	23436	84502	162695	287191	901182	1316301
	Rect. Area[4]	-	29162	23454	81266	163725	292269	906416	1343422
	Steiner points	-	5	8	20	25	40	84	94
	Runtime [s]	-	< 0.01	0.02	0.12	0.10	0.26	0.28	2.27
MP / MT	MP EA-WT[5]	14200	26418	21185	86601	153567	292707	892346	1326902
	MP Area[6]	10820	18544	14949	67280	112700	216686	752994	1197635
	Steiner points	2	5	5	13	10	20	75	89
	Runtime [s]	< 0.01	< 0.01	0.02	0.14	0.12	0.38	0.86	3.74
Improvement (%)		-	36%	36%	17%	31%	25%	17%	11%

[1] – Range of ports; [2] – Cost of a via; [3] – Routing area of the EM-aware WT, considering SP/MT; [4] – Rectilinear area of the terminal-to-terminal connectivity attained in the WP, considering SP/MT; [5] - Routing area of the EM-aware WT considering MPs; [6] – Rectilinear area using the MP selection algorithm of section IV.

B. Folded Cascode Operational Amplifier

The proposed methodology was used to automate the routing a folded cascade operational amplifier for the UMC 130nm CMOS design process, whose netlist (shown in Fig. 10) contains 15 different nets. The devices sizes and the set of currents/voltages attached to each terminal were obtained in a prior sizing task using the AIDA's circuit synthesizer, and the Layout Generator's Placer was used to generate the floorplan.

The developed routing steps were executed for each of the 15 MP/MT nets, and the numerical results of the obtained port-to-port optimal rectilinear forests for 7 nets are presented in Table II. Then, the detailed routing procedure reviewed in section II was used to automatically obtain a layout validated in Calibre® DRC and LVS, which is presented in Fig. 11.

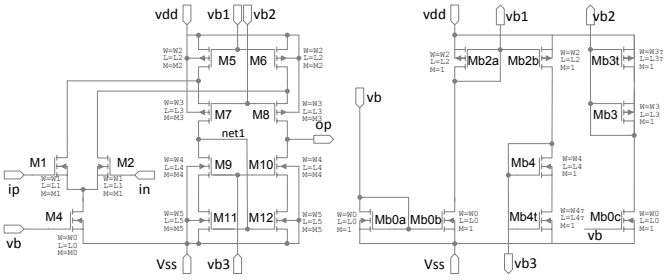

Fig. 10. Circuit Schematic.

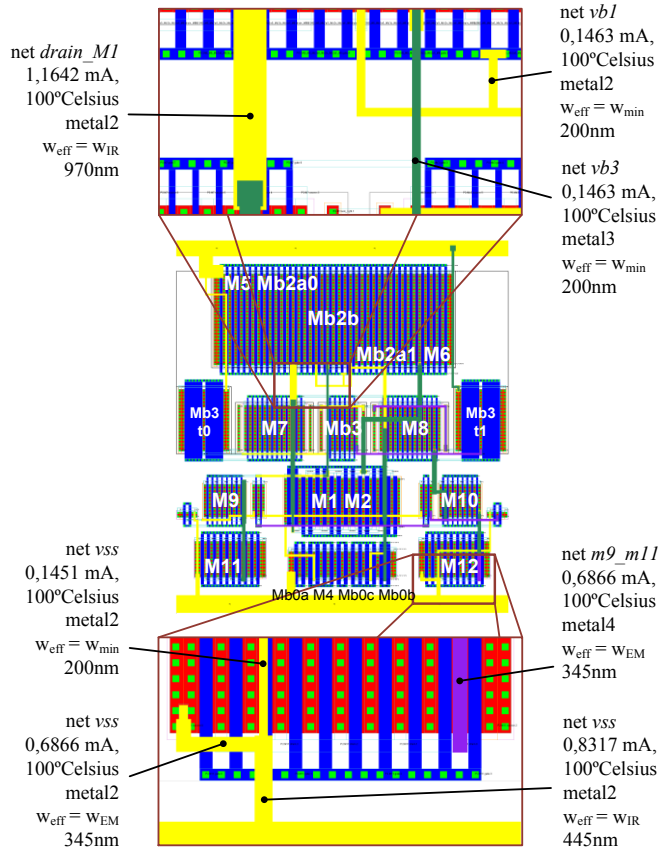

Fig. 11. Automatically generated routing for the Folded Cascode OpAmp.

TABLE II. RESULTS OBTAINED BY USING THE EM-AWARE MP/MT ROUTING APPROACH IN THE TWO-STAGE OPERATIONAL AMPLIFIER

Net	vdd	vss	vb1	vb3	net1	diffpair	op
#Terminals	13	9	8	9	4	4	2
#Ports[1]	[2 – 24]	[4 – 16]	[1 – 24]	[2 - 8]	[4 – 8]	[3 – 6]	[4 – 6]
MP EA-WP Area[2]	6,544173	7,412137	1,748870	2,021533	1,792770	2,152099	1,792770
MP-Selection[3]	1,512127	2,106730	1,748870	1,983807	1,191994	1,634567	1,191994

[1] – Range of ports; 2 - Routing area of the EM-aware WT considering MPs; [3] – Rectilinear area using the MP selection algorithm of section IV.

As observed in Fig. 11, for current intensive nets (e.g., *vss* or *drain_M1*), computing the wire width required to maintain the same MTF for all wires of the WT using the current/temperature values obtained from the sizing procedure, resulted, in some cases, in wires almost five times wider than the minimum allowed by the process. For these interconnects a proper current-flow and EM- and IR-drop-reliability is mandatory, as the circuit's performance is heavily compromised if the minimum wire width is applied instead, which often occur when using routing methodologies without current considerations or even in the manual design, especially during redesign cycles where some currents may change without the corresponding update in the layout. As dealing with a multitude of different currents manually is time-consuming and error-prone, it is not only hard to manually sketch a current-correct WT, but also, any change in the floorplan or in the current-correct tree may discard all the previous routing.

VIII. CONCLUSION

The effects of EM and IR-Drop are becoming increasingly more relevant and must be taken into account in the design of the interconnects of AMS ICs. In this paper, a MP/MT EM-aware routing methodology with IR-Drop avoidance for the automatic generation of analog IC layouts was presented. It intends to bypass the limitations of the available approaches, where simplistic 'dot-models' are assumed for the terminals, and force the inclusion of expert knowledge in the selection of ports, for a proper SP/MT regime. The implemented design flow solves the WP, MP selection, path rectilinearization and Steiner point assignment to minimize the total wiring area under the EM and IR-Drop constraints. At cell-level, complicated terminals' geometries may have any number of ports located on multiple fabrication layers that need to be considered, experimental results show the advantages of using the developed MP terminal approach to entwine the stages of the automatic Routers with realistic devices' geometries.

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