Panel: Emerging vs. Established Technologies, a Two Sphinxes' Riddle at the Crossroads?

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Abstract

Crossroads have always been challenging: they require a decision; in Egyptian and Greek mythology they were often guarded by two sphinxes trying to cheat the traveler with their riddles. The two sphinxes, the knight and the knave, the lady and the tiger, are just few instances of difficult puzzles that have kept logicians and mathematicians busy for the last 5,000 years.

Today, you are walking down Moore's Law road when you come to a crossroads: one road brings you into the land of emerging technologies: 14, 10 and 7 nanometer, FDSOI, FinFET, 3D-IC,… beyond and below; the other road holds you into the land of established technologies: 28, 40, 65, and 90 nanometers, possibly even above, A&M/S, MEMS,...

Choosing the right road is critical to lead your project and your company to success, but making the right decision is increasingly difficult, as it encompasses complex technical and economic considerations. However, unlike the mythological traveler, you won't run into the sphinxes but, rather, into some of our industry best experts; unlike the sphinxes, they will strive to provide you with honest advice about the "road conditions", and you are allowed to ask multiple questions to them to figure out which road is the best for you.

Moderator's Introduction

Prof. Giovanni De Micheli, EPFL, Switzerland

The race toward the ultimate semiconductor technology has been fueled by the goal of achieving a convenient performance/power figure within downscaling.

Currently there are two contending technologies in CMOS that are used for products. Fully-Depleted Silicon-on-Insulator (FDSOI) Field Effect Transistors (FETs) push the limits of the planar transistor geometries and introduce novel means of leakage control through an additional biasing given by a back gate terminal [Beigné]. In particular, Ultra-Thin Body and Box (UTBB) FDSOI is an advanced planar technology that takes advantage of high-κ metal gate and reduced-resistance raised source and drain access. The channel is intrinsic, i.e., without global bulk doping or pocket implants. Shallow Trench Isolation (STI) is used to electrically isolate the devices.

An alternative approach is provided by FIN FETs (also called Trigate FETS) that exploit 3-dimensional geometries to achieve a better control of the channel charge, in order to realize high-performance low-power SoCs [Huang]. In a typical FinFET device, the conducting channel is formed by a thin silicon "fin" connected to larger source/drain regions acting as supporting pillars. The gate is wrapped over the channel and controls the three-side of the fin. In addition to the effect of standard device engineering, such as strained silicon and high-κ metal-gate, the improved gate control of the tri-gate structure can be seen in the steep subthreshold slope, typically around ~70mV/dec.

Silicon NanoWires (SiNW) are expected to push further the scalability of electronic devices, because of their ultimate mono-dimensional semiconductor properties combined with the vast experience and investment in Si technologies. Top-down, i.e., lithography-based SiNW technologies are credible for Very Large Scale Integration (VLSI) circuits because of the accurate control of device size and geometry as well as of the proven capability of Si technology to scale-up to billions of devices per chip. In vertically-stacked nanowire structure, the channel is formed by a collection of nanowires that provides a high on-current and steep subthreshold slope (around 64mV/dec with very low leakage. The control gate is realized in a Gate-All-Around (GAA) fashion and ensures an excellent electrostatic control over the channels. Moreover, SiNW transistors can be realized with two gates, one of which determining electrostatically the polarity of the transistor (nMOS or pMOS) and the other gate turning the transistor on/off [DeMarchi]. As a result, the device is more versatile.

New materials have shown to be effective to realized scaled down devices, and there effectiveness for very-large scale integration is under investigation. Graphene (possibly in conjunction with Si) has been used to craft effective transistor, and Molibdenium bisulphite (MoS2)

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[Radisavljevic] has shown to produce scalable transistors with effective characteristics. Carbon Nano-Tubes (CNTs) have been investigated for over two decades, but the recent embedding of CNT FETs within a regular planar process has given rise to the possibility to realize a simple computer in CNT technology.

Whereas all these technologies can be downscaled below the 10 nanometer limit, at the very end of the scaling roadmap, Tunnel FETs (TFETs) will compete with other technologies because of the intrinsic capability of overcoming Boltzmann's tyranny. Nevertheless, it is reasonable to believe that the materials of choice and scaling limits will eventually be dictated by economic concerns beside the performance/power figures.

Panelists' Position Statements

Rob Aitken, ARM, USA

Crossroads are a recurring metaphor in literature, not just in the story of the sphinx and her riddles. Alice encountered the Cheshire Cat at one, and asked it "Would you tell me, please, which way I ought to go from here?" to which the Cat wisely replied "That depends a good deal on where you want to get to" [Carroll]. The same point should be made here as well: On our journey down Moore's Law Road, it helps to know where exactly it is that we intend to go. The choices open to us are really quite simple. The first is to continue forward, towards the inviting-looking land of Success that is always better than where we are now and always on the horizon. This road looks more challenging every time we stop and pause for breath, but we have been on it for some time now and it has always carried us forward. The second choice is to give up on this road altogether and try another path that is rumored to take us to the same place, but which goes off in a different direction, and from where we stand sometimes appears to be leading directly away from our goal.

The sphinx-worthy riddle of our journey comprises multiple parts. We know that Moore's Law Road stops, but we don't know where. We know that some "More than Moore" technologies will succeed, but we don't know which ones. Finally, we observe that those who have departed from Moore's Law Road in the past have by and large not returned the game being played by those remaining on the road. With this framing, it seems clear that the choices can be summarized as 1) continue on the road, but be careful and observant, and 2) switch to a different road, but be sure you know where you're headed.

With option 1, two points are clear immediately. The first is that while it is always possible to switch to option 2, the longer you delay making the choice, the more you have invested in option 1 and, as a result, the harder it can be to succeed at option 2. The second point is that choosing option 1 is only the first of an ongoing set of choices, and the choices of your fellow travelers influence yours. 20 nanometers is a good example. It is clear now that 20 nanometers is the last node for bulk CMOS. A few years ago there was speculation about what would follow, and the two primary choices were ultra-thin-body SOI and finFET. Most companies have now chosen finFET. That makes their collective choice easier and makes sticking with UTB-SOI harder for anyone who chooses it. New choices emerge at 10 and 7 nanometers: higher mobility materials and devices (e.g. III-V quantum well FETs), improved channels (e.g. horizontal or even vertical nanowires), and so on. Making these choices harder is the knowledge that they are only temporary fixes. Each one moves us forward a node or two, but each will very quickly run its course. Bulk CMOS lasted perhaps 20 generations. Standard finFETs may only last 3. Economically, this emphasizes the need to make choices collectively: 1 or even 2 companies choosing a path on their own cannot create the economies of scale or the supply ecosystem to be successful. As cost and complexity continue to rise, these ecosystems will grow in importance and influence.

In addition to the main choices that go with option 1, there are other opportunities as well. These fall mainly into the "More than Moore" category. 3D-IC and embedded non-volatile memory are two of the most enticing at the moment. Choosing these correctly can allow you to sprint past your competition, but they can also toss you into the ditch. They are high risk, high reward, as are EUV and 450 millimeters, which are also on the horizon. They will arrive sometime, but identifying "sometime" is important. Switching metaphors yet again, a drafting strategy may be desirable: follow the leaders closely and avoid expending extra energy, but be prepared to switch direction quickly if they crash.

Let's return to the second of the original two choices. Before choosing option 2, it's important to remember its asymmetry with option 1. You cannot go back to option 1 from option 2. It's too difficult and too expensive to get back on Moore's Law Road. There are unquestioned opportunities here: the Internet of Things being the most obvious – the silicon associated with Wireless Sensor Networks will end up somewhere much closer to 90 nanometers, than to 10. There are also enticing-looking places that are really swamps: No one is going to build the next generation smart device on a technology that is 2 or 3 nodes behind the leaders. Similarly, using 3D-IC to split logic across multiple dice sounds good until you realize that 30 microns is a tight pitch in the world of through-silicon vias, but a huge distance in logic. On the other hand, established technologies, by virtue of being established, are more stable and better characterized than leading edge nodes, and so much more amenable to process-sensitive enhancements such as AVFS and margin shaving.

Suppliers, be they foundries, IP vendors, or EDA, need to support their customers in whatever choices they make, and so they will create ecosystems where like-minded customers and products can thrive, but this does not make the choice at the crossroads any simpler. In the end, this choice is difficult, but it is not necessarily final. The sphinxes will try to confound us, but if we know where we're headed, we can be confident in our choices.

Antun Domic, Synopsys, USA

Only seldom in the history of semiconductor industry designers of integrated circuits (IC) have been presented with the breadth of choices that manufacturing process technology offers today.

In the emerging technologies camp, revolutionary non-planar CMOS (FinFET, tri-gate) and double patterning give designers unprecedented performance and power envelopes, while at the same time leapfrogging the limitations posed by 193 nanometers immersion lithography, as we wait – Godot-like? – for EUV. More "evolutionary revolutionaries" are considering the merits of FDSOI, whose proponents highlight its performance and power envelope comparable to the one of non-planar CMOS, compatibility with bulk CMOS at the IP-level, and lower costs and risks. In the established technologies camp, the richness of the device options (bipolar, CMOS, DMOS, RF, embedded FLASH memories, supply voltages ranging from 1 up to several hundreds Volts), along with the availability of advanced design automation methodologies, tools, and flows make it possible to achieve results that were not even imaginable when these technologies were first introduced as "emerging" more than a decade ago.

System integration is also offering new opportunities with silicon interposers (2.5D-IC) and stacked die (3D-IC); although possibly not 100% ready for the primetime yet, these new assembly technologies suggest scenarios in which digital, analog and mixed-signal, memories, and MEMS will be unprecedentedly tightly integrated, thus delivering levels of performance and functionality that we could only dream about until not so long ago.

From an EDA vendor perspective, this breadth of choices demands for an even stronger cooperation with our partners and customers: today emerging technologies are tomorrow established ones, and it is very unlikely that our partners and customers will consider changing their design implementation and verification platform depending on the technology node; the solution has to be carefully tailored so that the common denominator is as ample and comprehensive as possible; the need for certain "exotic" features must be weighed to ensure that the expected benefit is not annulled by "non-standard" requisites. Fortunately, the requirements are not completely different; timing, power, area, efficient use of routing resources, embedded analog – or embedded digital – integration… the relative order and the priority may differ, but objectives are, mostly, the same and can be addressed and fulfilled by means of the same "weapons".

One great example are the design for low power techniques that we had devised a decade ago to address the power consumption problem of mobile applications at then emerging manufacturing processes: these techniques can be successfully retro-fit for use with established nodes, revolutionizing embedded digital computing performances thanks to power consumptions as low as 1 micro-Ampere; as a result, today, we can see designs manufactured at 180 nanometers using 12 voltage domains. Another example is routing technology: the very same router can be effectively and successfully applied to emerging technologies with 15 routing layers, where the challenge stems from the raw number and the complexity of design rules that must be complied with, and to established technologies 2 or 3 routing layers, where the challenge stems from the scarcity of the routing resources and the tighter reliability requirements; closing routing at 180 nanometers with 2 routing layers and 100% redundant vias can be as challenging as closing routing at 14 nanometers with 15 routing layers, thousands of design rules, and double patterning.

Crossroads may be a challenge, they may be scary at times; but solving the riddle is certainly easier if we collaborate stronger, understanding each other requirements. EDA is a critical ingredient of advanced design, regardless of the manufacturing process technology, and can help, and accelerate the innovation in our industry.

Manfred Horstmann, GLOBALFOUNDRIES, Germany

The semiconductor Industry and GLOBALFOUNDRIES runs 28 nanometers in volume production, starting to ramp 20/14 nanometer technologies and does development work on 10/7 nanometers. But there are some basic questions:

Will it be Silicon forever? Will be thy "CMOS scaling" replaced by 3d stacking? How to handle the patterning challenges? Are we reaching the economical $$$ limit before the physical limit?

28 nanometers will be for a long time a sweet spot in Foundry Industry for yield/performance and cost reasons. This node will be the work horse and technology features like embedded Flash, HV etc. will be added to make exciting products. 3d packaging will be rolled out on this node, too.

14 nanometers (FINFETs) is the next node and today mainly attractive for absolute high end applications but likely at some point in future 14 nanometers has the potential to be the next "sweet" spot.

FINFETs can be scaled down to 10/7 nanometers but need technical solutions to make patterning less expensive, novel

materials are required but at the very end: If 7 nanometers is ever economical doable remains to be proven.

Robert Hum, Mentor Graphics, USA

There is no doubt that choosing the 'optimal' implementation technology for your next design is critical. It is tempting to jump in with both feet to look at the myriad of tradeoffs between technology nodes: cost, performance, reliability, density, functionality, power, design enablement, tool support, IP availability, what your competitors are doing and so on, because, after all, we are engineers, and technology, especially leading edge technology, is our business. However, this is seldom the most important riddle to solve! Let me relate two personal experiences to demonstrate the point. In 1997, I joined Ikos Systems as VP of Engineering. The company had a leadership position in digital, gate-level, event-based simulation and marketed its hypercube-based supercomputer NSIM worldwide. It had beat out its arch rival Zycad with better technology and a better roadmap. When I arrived on the scene, a second generation of this box was being developed with three new ASIC designs. Our engineers had carefully considered whether to use a new leading edge node or stick with a more tried and true node. They had chosen a leading edge node and the designs were already in fabrication by the time I arrived. The company had bet its future on this next generation machine. To make a long, painful story short, I cancelled the project and embarked on successfully reinventing the company portfolio. Why? Quite simply this: an emerging technology had made gate-level, event-based simulation obsolete! Static timing verification coupled with RTL level simulation was taking over, but IKOS had missed the transition. This is a classic example of "The Innovators Dilemma".

A few years before I joined Ikos, I was with Nortel, the Canadian telecom giant that recently passed quietly away. At one time they literally owned 55% of the digital switching market in North America. What went wrong? Nortel certainly had access to every conceivable technology: lasers, fiber, GaAs, advanced CMOS, BiCMOS, fineline PCB, multi-chip packaging, and so forth? Did Nortel do a bad job assessing whether to use existing technology or emerging technology for its designs? Nope! They got that right. What they missed was the emerging technology associated with data/computer communication, and the fact that synchronous circuit switched telecommunications was being replaced with datagram telecommunications (such Ethernet).

There are other serious examples: Kodak, Motorola, RIM (Blackberry), Nokia, Digital Equipment Corporation, just to name a few. The point is that before you embark on choosing the best technology for your next design; make sure that your design warrants being implemented at all. You should be worried about emerging technology, not only as your implementation medium, but much more importantly, as a competitive threat to your business.

Philippe Magarshack, STMicroelectronics, France

While the industry as a whole is following Intel in implementing FinFETs at 14/16 nanometers, ST has developed an alternative approach with its partners, based on 2D Ultra-thin-Body-BOX (UTBB) Fully-Depleted SOI transistors (FD-SOI).

UTBB FD-SOI is already proven in 28 nanometers where it is already making the promise of "faster, cooler, simpler", a reality. It is recognized that the 28 nanometers node will be cost- and performance-competitive for many applications for many years to come, and FD-SOI will enable 28 nanometers to last even longer.

Milking the full benefit of UTBB FD-SOI implies the usage of Body-Bias, ie tying the back-gate of the transistors (or Body), to a variable Voltage (or Bias). Unlike Bulk or FinFET transistors, UTBB FD-SOI transistors can be biased to +/- VDD or even +/- 3xVDD if required. The immediate effect is that the Vt of the corresponding transistor is effectively shifted by 85mV/V. In CPU cores, this enables the same ARM Cortex dual-A9 to run at 3GHz at 1.4V or at 1GHz at 0.6V. In Analog, this enables switch capacitor filters Ron/Roff ratio to be boosted by 10x vs Bulk. For once, Analog designers are loving advanced CMOS !!!

The 14 nanometers FD-SOI under development is showing cost and low-power advantages over 14/16 nanometers FinFET. The key to success and adoption will be recognition in the IP and design community.

Clearly, taking a different approach (with FD-SOI) than the "rest-of-the-world" comes with many challenges, but the possible rewards are equally great. The jury is still out, but the success of this unique strategy will be measured in the coming years.

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