An Approach to Realistic Fault Prediction and Layout Design for Testability in Analog Circuits

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Abstract

This paper presents an approach towards realistic fault prediction in analog circuits. It exploits the Inductive Fault Analysis (IFA) methodology to generate explicit models able to give the probability of occurrence of faults associated with devices in an analog cell. This information intends to facilitate the integration of design and test phases in the development of an IC since it provides a realistic fault list for simulation before going to the final layout, and also makes possible layout optimization towards what we can call layout level design for testability.

1.- Introduction

Inductive Fault Analysis (IFA) deals with the statistical defect distribution in a fabrication process providing defect generation and analysis, defect-to-fault translation and fault classification and grading. The use of IFA for analog circuits has been mainly aimed at predicting yield, facilitating fault simulation and testability analysis, and to layout optimization [1-7].

From the point of view of testability improvement, layout optimization can be seen as the process of generate layouts with a reduced number of difficult to detect faults in order to optimize the fault coverage figure. This process needs four main issues: circuit layout, IFA run, fault simulation and fault coverage analysis, and new circuit layout. All these subjects require considerable effort and can be very time consuming. The cost of this can be extreme in the case of analog and mixed-signal IC's due to the complexity of analog layout and also to the lack of efficient design automation tools.

A solution to reduce the cost of fault simulation was proposed in [8] referred to as Local Layout Realistic Fault Mapping (L^2RFM). It studies the relationship between typical analog layout structures and specific defects/fault occurrence to derive realistic fault assumptions prior to the final layout. However, this approach is very limited because it is unable to deal with the diversity and disparity of cells which can appear in any analog layout depending on the concrete application and the global circuit performance.

The work in this paper is also aimed to predict a realistic fault list before going to the final layout of a circuit, but the approach is quite different from that in [8]. Here, a methodology is proposed to generate explicit formulas modelling the probability of occurrence of specific faults in a device structure as a function of its geometrical parameters. Information from the statistical defect distribution in a given fabrication process is used to find the relationship between device structures (transistor layout shapes) and fault occurrence. The work is addressed by two main subjects: i) test cost reduction, since a realistic fault list can be predicted prior to the final cell layout helping to reduce the fault simulation time and to generate efficient test patterns; ii) layout level design for testability, since some rules will be provided for generating robust layouts with a reduced number of difficult to detect faults. In addition, the automation of defect-insensitive layout generation is envisaged.

In this first phase, the work contemplates device structures leaving the investigation about routing considerations for a second phase. Only CMOS devices have been considered but the methodology is equally applicable to bipolar and BiCMOS.

The paper is organized as follows. Section 2 presents the method employed to develop explicit models for the probability of occurrence of faults in different transistor structures, as well as layout rules that are derived from the analysis of the obtained results. Section 3 applies the derived models to the layout of a fully-differential opamp and compares the predicted fault incidence with data obtained

from IFA of the same layout. Finally, Section 4 summarizes the main conclusions of this work.

2.- Modelling realistic faults in analog cells

The procedure we followed to model derivation is illustrated in Fig. 1. First, a layout containing 237 different transistor structures was generated in an 1.2µm CMOS technology. Transistor sizes were varied in the ranges 2.4µm ≤ W ≤ 307.2µm and 1.2µm≤ L ≤ 307.2µm, and two different transistor shapes (rectangular, and interdigit) were used, with aspect ratio between 0.1 and 10. Figure 2 shows a sample of these structures.

An Inductive Fault Analysis was run on the layout using VLASIC to scatter 24 defect-types on 10^6 circuits; as result, a number of 25496 circuits were reported to contain faults. The more likely faults included in the list provided by the IFA were shorts and opens produced by different types of defects. This list was processed taking into account the number of circuits containing the fault in order to get a measurement of the type and of the probability of faults for each cell (transistor). A multiple regression analysis with main effects and interactions was then performed with the commercial statistical package SAS [9] to obtain an optimal approximation for the probability of faults as a function of transistor characteristics (i.e. width (W), length (L) and number (N) of gates for split transistors). This model aims to:

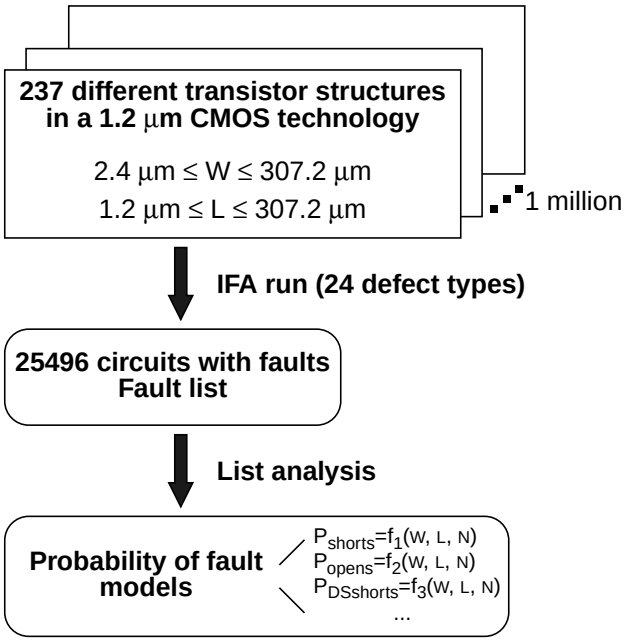

Fig. 1: Model derivation flow

1.- Model how each characteristic (W, L, N) affects the probability of faults, giving us information as to which shape is more suitable and robust from the IFA point of view. Also, rules for a better layout generation can be derived.

2.- Predict the probability of faults for a given W, L and N before going to the final layout, and therefore, measure the quality of the layout during the design phase.

In order to obtain different levels of modelling, different groups of faults have been considered. The complete set of short and open faults are considered in Level 1. In Level 2 all short and open faults are grouped and modelled separately. Finally, Level 3 corresponds to a more detailed modelling where the different types of shorts and opens are separately considered. The predicted models obtained using SAS for each group are given in Table 1, together with the corresponding adjusted R-square which indicates the statistical significance of the fitted model (values of R close to 1 indicate good fitting of the model to the experimental data, while values close to 0 will indicate poor fitting). Note that the obtained probability function is different in each case. On the other hand, Level 3 models for GDS shorts (gate-drain-source shorts) and G opens (gate opens) could not be derived due to their low likelihood which was manifested in the low R value given by SAS.

The evolution of the probability of faults as given by the Level 1 model is illustrated in Fig. 3. Plots in Fig. 3a correspond to transistors with L=10µm and W ranging from 2.4 to 300µm, while plots in Fig. 3b correspond to transistors with W=250µm and L ranging from 1.2 to a 100µm. One of the results we can get from Fig. 3 is the relative high influence of N, which is the number of transis-

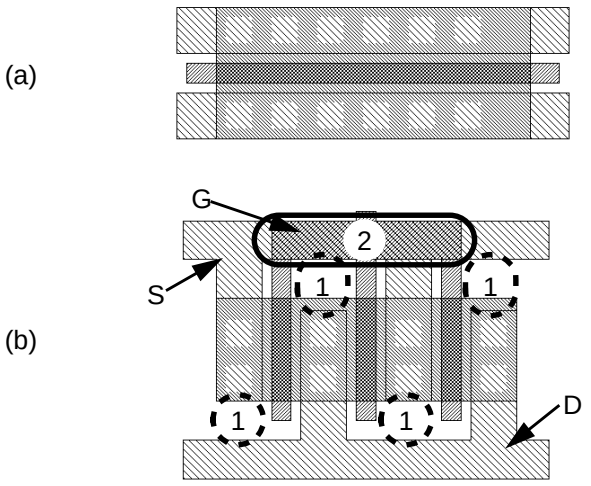

Fig. 2: Different transistor shapes: (a) rectangular, (b) interdigit.

Table 1: Models for the probability of fault

Model Level	*Fault*	*Predicted Probability Model*	*Adj. R-square*
Level 1	All	$\mathbf{PROB^{0.4}}$=0.0631+0.0002·L+ +0.0056·N+0.0005·W+0.0001· ·L·N-13·10^{-7}·L·W-14·10^{-6}·N·W	0.8791
Level 2	Shorts	$\mathbf{PROB^{0.3}}$=0.126+0.0004·L+ +0.0074·N+0.0006·W+0.0001· ·L·N-19·10^{-7}·L·W-21·10^{-6}·N·W	0.8709
	Opens	$\mathbf{PROB^{0.3}}$=0.0649+0.0001·L+ +0.0022·N+0.0001·W+0.0001· ·L·N-62·10^{-8}·L·W-61·10^{-7}·N·W	0.6830
Level 3	DS shorts	$\mathbf{LOG_{10}(PROB)}$=-3.318- 0.006·L+0.0734·N+0.0015·W- -0.002·L·N+235·10^{-7}·L·W- -13·10^{-5}·N·W	0.4026
	GD shorts	$\mathbf{PROB^{0.5}}$=0.0169+0.0002·L+ +0.0006·N+0.0002·W-49·10^{-8}·L·N- -79·10^{-8}·L·W-3·10^{-6}·N·W	0.9403
	GS shorts	$\mathbf{PROB^{0.6}}$=0.0077+0.0001·L+ +0.001·N+0.0001·W+0.0001· ·L·N-63·10^{-8}·LW-27·10^{-7}·N·W	0.9513
	GDS shorts	Not much statistical evidence	0.1653
	D opens	$\mathbf{PROB^{0.1}}$=0.400+0.0002·L+ +0.0014·N+0.0001·W+0.0002· ·L·N-81·10^{-8}·L·W-18·10^{-7}·N·W	0.4873
	S opens	$\mathbf{PROB^{0.1}}$=0.391+0.0002·L+ +0.0034·N+0.0002·W+0.0002· ·L·N-91·10^{-8}·L·W-11·10^{-6}·N·W	0.5073
	G opens	Not much statistical evidence	0.1819

tors in what a wide transistor is split in the interdigit structure. As consequence, we can conclude that the transistor structure with less incidence of fault is the rectangular (N=1), although in general it is not recommended for wide transistors due to its poor aspect ratio. On the other hand, interdigit structures (N≥2) have most incidence of potential faults.

It is important to remark that the above results correspond to a specific CMOS technology and a concrete style in generating transistor layouts (although this style is the most common). However, the methodology herein proposed can be applied to other technologies and cell structures, giving in each case the corresponding probability functions, which can be obtained once and used afterward as many times as necessary.

To illustrate some of the layout rules which can be derived from the above models let us consider the case of the interdigit layout structure. In Fig. 4 the probability for short faults as predicted by the models in Table 1 is plotted versus transistor W, L and N. Note that for this structure, gate-source shorts are more probable than gate-drain and drain-source shorts except for high values of N where drain-source shorts dominate. This can be explained looking at the areas identified in Fig. 2b (it corresponds to the particular case of N=3); in this transistor structure we can see that: i) the gate and source terminals run one over the other in the area labelled 2 and hence this area will increase with L and N, as consequence gate-source shorts due to pinhole defects between metal and poly will increase with L and N; ii) drain-source shorts are due to extra metal in areas labelled 1, and therefore, they will increase with N. From these results two rules for better layout of interdigit transistors can be derived: a) running source metal over gate poly (as is usually done by many module generators) should be avoided for large transistors, b) N should be the lowest as possible, that is, a wide transistor should be split into the lowest number of transistors whenever the other design requirements allow it.

3.- Example of application

As an application example, the fully-differential operational amplifier in Fig. 5 is considered. The layout of the

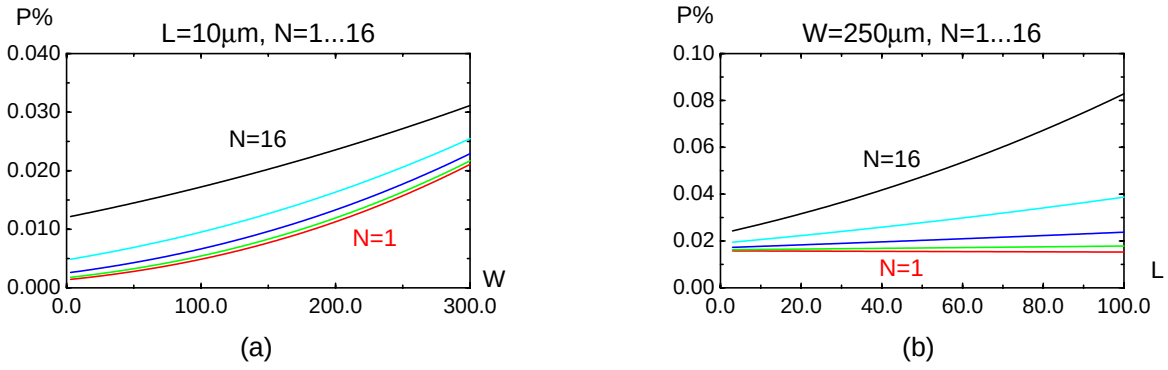

Fig. 3: Probability of faults given by the Level 1 model for transistors with: (a) L=10µm, (b) W=250µm.

amplifier has been optimized from its performance point of view; that is, transistor structures with the less capacitive parasitics, some symmetries and adequate orientations have been chosen. The final layout is shown in Fig. 6. The probability of faults in this layout (not including interconnections) has been predicted by the Level 1 Model in Table 1 resulting in a 0.11%.

In order to validate the derived models, the same type of IFA has been run for the complete layout of the opamp. Of a total of 1786 given faults, only 464 (~26%) correspond to the routing area while 1322 (~74%) appeared in the device area. The result of this IFA analysis revealed a total probability of faults in this layout of 0.1375%, which is very close to the predicted by the Level 1 Model. On the other hand, analysing separately each of the fault types the data in Table 2 is generated, where the probabilities predicted by the corresponding models appear in the first row, while those given by the IFA of the opamp layout are in the second row. Notice that the discrepancies between predicted and measured data are low.

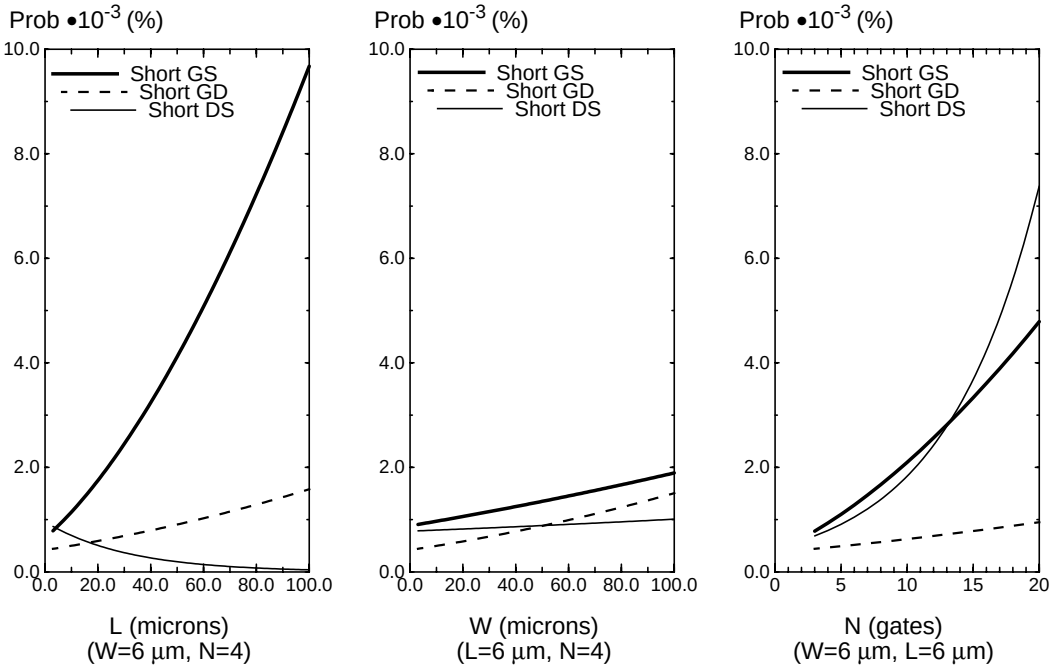

Fig. 4: Predicted probabilities of shorts for interdigit transistors

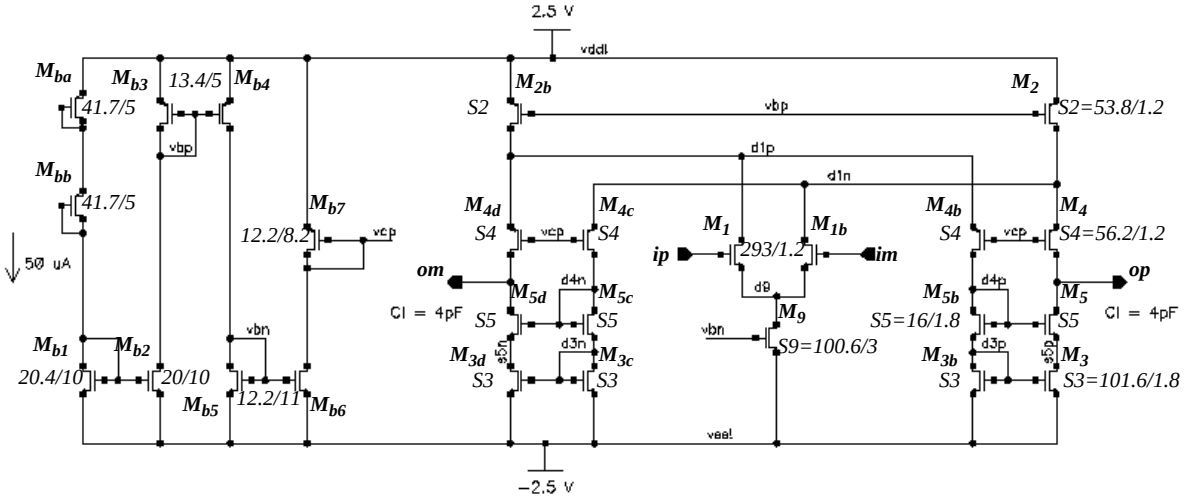

Fig. 5: Fully-differential operational amplifier

Table 2: Predicted and measured probability of faults in an opamp (%)

Model Level	*Fault*	*Predicted*	*Measured*
Level 1	All	0.11	0.1375
Level 2	Shorts	0.10	0.1071
	Opens	0.006	0.0056
Level 3	DS shorts	0.02	0.0615
	GD+GS shorts	0.07	0.0617
	GDS shorts	---	0.0030
	D+S opens	0.006	0.0055
	G opens	---	0.0001

4.- Conclusions

The relationship between layout style and defect incidence in different device structures has been studied using IFA methodology. From this study models have been developed able to predict realistic fault lists in analog cells before going to final layout, and hence, making possible the incorporation in the design phase of an IC of additional considerations targeted to defect-insensitive layout generation or, at least, to layout with a reduced number of difficult to detect faults. The models can be derived once for a given technology and applied afterward as many times as necessary during design phases. Models have been developed for single transistors (NMOS & PMOS) and have been verified comparing results with the IFA fault list for a fully-differential Opamp. Results from the application example allow us to conclude that: a) For analog cells, faults in active areas could be dominant versus faults in routing area, b) Rectangular transistor structures have lower incidence of faults than interdigit structures, c) For some usual interdigit structures GS-shorts are more probable than GD and DS shorts, except for high N (number of gates in an interdigit transistor) where DS-shorts dominate. The faithfulness of the first results obtained encourages us to further research. Currently we are extending the study to typical transistor structures in analog circuits such as differential pairs, current mirrors and cascode transistors. Also, the application of these fault models to drive the automatic generation of analog cell layout is being integrated in our tool GELSA [10].

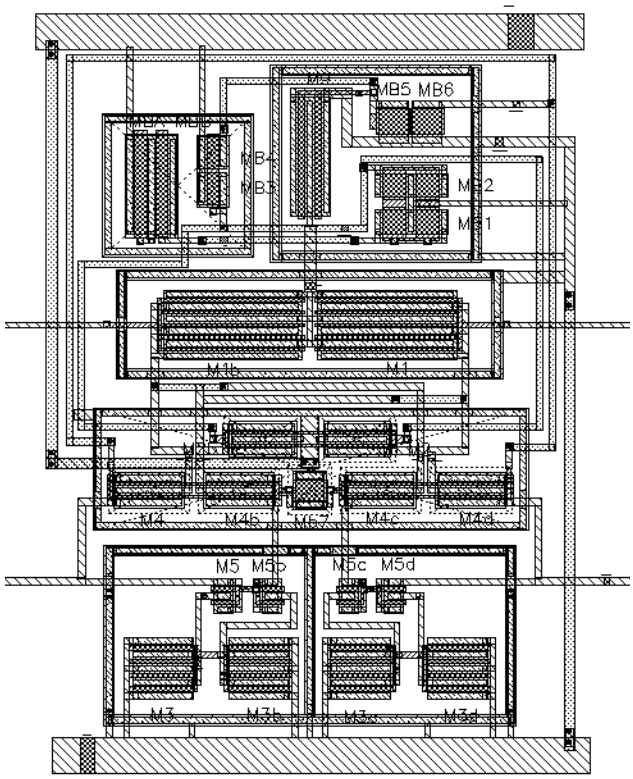

Fig. 6: Layout of the fully-differential opamp

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