Analog Test Design with IDD Measurements for the Detection of Parametric and Catastrophic Faults*

Walter M. Lindermeir   Thomas J. Vogels   Helmut E. Graeb

Institute of Electronic Design Automation
Technical University of Munich
Arcisstr. 21, 80333 Munich, Germany

Abstract

Earlier approaches dealt with the detection of catastrophic faults based on IDD monitoring. Consideration of the more subtle parametric faults and the ADC quantization noise, however, is essential for high-quality analog testing. The paper presents a new design method for analog test of parametric ***and*** *catastrophic faults by IDD monitoring. ADC quantization noise is systematically considered throughout the method. Results prove its effectiveness.*

1 Introduction

Since analog testing is expensive for various reasons, e. g. necessary equipment, evaluation of the applicability of power supply current (IDD) measurements to analog integrated circuits testing is enticing. Testing techniques based on IDD measurements have already proven to be a boon for testing digital integrated circuits. Especially measurements of current flow in the quiescent state (IDDQ measurements) of digital CMOS circuits are important in raising test reliability and fault coverage [1, 2]. Furthermore wafer probe testing disallows specification testing and calls for simple alternatives [3, 4, 5, 6]. Firstly, the operating environment vastly differs from the testing environment [7]. Secondly, only a limited number of types of measurements are possible with a reasonable accuracy. The test objective and the (automatic) test equipment must be matched.

Until now manufacturing defects, e. g. drain to gate shorts or unconnected terminals, that constitute hard or *catastrophic* faults, have been the main point of interest. In [3] the correlation between changes of the power supply current due to catastrophic faults and DC input stimuli were the central point of interest. [8], [6], and [4] use the spectrum of the power supply current for testing. Observing the discrete spectrum instead of the transient signal in the time domain obviates the need to store a large amount of data and facilitates decision taking.

The possibility of a second type of fault is to be addressed when testing analog integrated circuits: soft or *parametric* faults. Global deviations of the manufacturing process entail a statistical distribution of the circuit parameters and thus variations of the system performances. While a *design for manufacturability* [9, 10] may reduce the yield loss, the remaining yield loss is not negligible and the obligation to determine tests for the detection of parametric faults persists. Compared to catastrophic faults which happen due to excessive deviations, parametric faults are by far more difficult to detect [18] and thus pose a challenge to the analog test design.

Fault detection may not necessarily be based on specification tests: power supply current measurements in the frequency domain are alternatives. [3] notices the possibility to find parametric faults when employing IDD measurements, graphing the relationship between the "leakiness" of a p-n junction and fault coverage. The statistics of the parameters were not considered. [5, 6] took the tolerances of the circuit parameters into consideration, yet were only concerned with the detection of catastrophic faults.

This paper presents a novel methodology enabling a comprehensive test design aimed at go/no-go testing with respect to both, parametric as well as catastrophic faults. A key feature of the approach is that the specifications that are usually guaranteed to the customer build the basis for the test decision, while the decision criteria are evaluated based on the spec-

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trum of the power supply current of the device under test. The statistics inherent in the manufacturing process and the measurement noise are systematically taken into account in order to achieve a robust test design. For one, the Monte-Carlo simulations will reflect the effects of the manufacturing process on the circuit performances and the power supply current. For two, the test quality is evaluated with respect to the measurement noise that is intrinsic to the analog-digital conversion.

We detail the implications of choosing IDD measurements in Section 2 and proceed in Section 3 with calculating the measurement noise affecting their significance. After the introduction of the parametric fault model in Section 4 we outline in Section 5 how to arrive at a decision rule to discriminate between "good" and "faulty" circuits. Section 6 explains how catastrophic faults are covered. The experimental results in Section 7 show for the first time that a comprehensive test design with respect to parametric and catastrophic faults can be achieved by using IDD measurements. A novel feature is the systematic consideration of measurement noise yielding the required resolution of the ADC for a desired high test quality. Section 8 concludes the paper.

2 Set-up for IDD spectral measurements

There are two basic incompatibilities between digital and analog integrated circuits that interfere with an unadapted use of IDD measurements for fault detection. In the first place, we may observe a difference in the order of several magnitudes between an impeccable and a faulty digital circuit, yet for an analog IC this difference falls into a range of possibly less than one magnitude. In the second place, IDDQ testing assumes the current reading to increase for a faulty digital IC, but the sign of change is important for an analog IC and one might just as well observe a decrease [3].

While these two factors already make it challenging to detect catastrophic faults, they impede detection of parametric faults. Therefore the input signal must be carefully chosen so that the changes of IDD are expository for faults. Like [5] we resort to a transient waveform as input stimulus, cf. Fig. 1. It is an approximation of a rectangular wave with finite slopes and should be readily available in the test environment. The signal used to excite the IC is rich in energy in the (odd-numbered) harmonics. It is expected that more than one harmonic of the IDD spectrum bears significant information about the circuit.

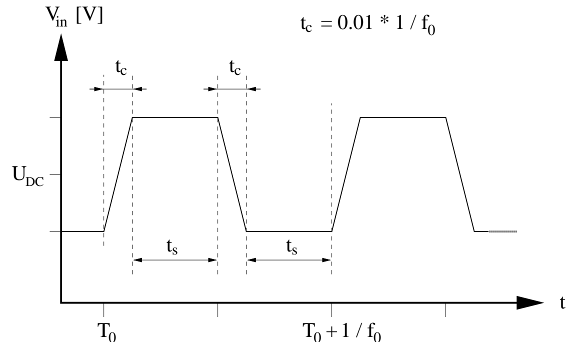

Figure 1: **The trapezoid input signal**

Settling for a periodical pulse and one amplitude, we can still vary the basic frequency f_0 and the DC offset U_{DC} of the input stimulus. From a large number of possible combinations (f_0, U_{DC}) a preliminary subset is automatically chosen with the help of a factor analysis based on the singular value decomposition of the sensitivity matrix, and it is this subset that we will later deal with when running the discrimination analysis to determine test criteria.

To obtain the set of measurements the following steps are to be taken: After the input signal has been applied to the circuit for a few periods, it may be assumed that the circuit is in a steady state. Then the power supply current is sampled and digitized for one period (cf. the next paragraph). Here we may either probe for the IDD of the whole circuit or only part thereof. The discrete Fourier transform of this data set is calculated next. The RMS value, the fundamental, and the first few harmonics are extracted and fill the set of primary measurements. We use only the magnitude of the coefficients to avoid susceptibility to time, i. e. phase shifts.

3 Measurement noise inherent to the analog-digital conversion

The measurement set-up includes the analog signal generator, possibly a digital signal generator and a digital capture facility (cf. Fig. 2) [13]. While [13] was concerned with testing the analog-digital converter as an example of a mixed-signal circuit, the relationships derived there equally hold when using the ADC for instrumentation.

The quality of the analog to digital conversion is customarily determined as follows: Assume the data

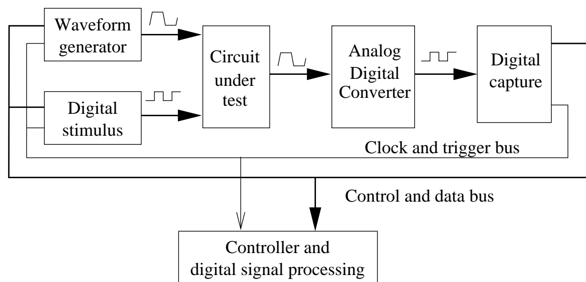

Figure 2: **Measurement setup with ADC**

word to have m [bits], the input range of current readings to be R [A], and the conversion function to be linear over the input range, then the mean error q is half of one quantization interval, i. e.

$$q = \frac{R}{2^{(m+1)}} \quad [\text{A}]. \tag{1}$$

The size of m is a measure of the complexity of the analog-digital converter (ADC). It is predetermined by the available test equipment or is chosen based upon a table provided by our method relating the number of bits (m) to the expected test quality (cf. Table 3).

Since the RMS value of the power supply current of an analog IC is large compared to the changes invoked by the input stimulus, the input range R should only cover the dynamic range of the IDD. This can be achieved by taking all measurements with respect to the mean value. The described set-up makes the whole range of the ADC available to the measurement of the transient waveform.

Moving to the spectral error estimation we see the rate of conversion expressed as a multiple of the base frequency of the input signal. This ratio equals the number of samples taken during one period, N. A discrete Fourier transform will yield as many samples in the frequency domain as there are in the time domain.

If we assume the quantization error to be evenly distributed between $-\frac{q}{2}$ and $+\frac{q}{2}$, we calculate the square of its standard deviation to be $\sigma^2 = \frac{(q/2)^2}{3}$ (cf. [14]). If we further assume, that the power of the noise stemming from the quantization error can be seen across the full spectrum, the noise floor is (cf. [13]):

$$n^2 = \frac{\sigma^2}{N} = \frac{q^2}{12 \cdot N} \quad [\text{A}^2]. \tag{2}$$

The consideration of the measurement error is mandatory for the discrimination analysis to be practically applicable [11]. The level n of the quantization noise also guides the selection of the harmonics included in the primary set of measurements. Only those Fourier coefficients whose mean values rise considerably above the noise floor are handed to the next phase of the test design.

4 Modeling of parametric faults

The manufacturing process is inherently stochastic. This is reflected on the circuit level by *statistical parameters* deviating from their nominal values. For example, the substrate doping or the oxide thickness fluctuate among a set of manufactured ICs. The statistical variations of the parameters lead to variations of the circuit performances.

A parametric fault now occurs when a combination of parameter deviations induces a violation of one or more of the IC specifications. Since this fault model is based on circuit specifications and not on geometrically defined bounds for the parameter values, we take reference to the manufacturer's obligation to guarantee circuit performances. Simulations are run in order to evaluate the impact of parameter deviations on the specified performances and on the "test" performances. The later comprise the Fourier coefficients from IDD measurements, our primary measurements.

The fluctuations of the statistical parameters must be clearly visible in these measurements. A combination of the factor analysis mentioned in Section 2, to provide a set of predictive input stimuli, and discrimination analysis, to find the minimum number of measurements, proved to be successful for the circuit under test in Section 7.

5 Designing test criteria

Having the results of a set of Monte-Carlo simulations at hand one is left with the task of determining decision rules to allocate sample elements to either the subset of good or the subset of faulty circuits. To obtain robust results we use linear discrimination analysis [15, 5, 11]. A circuit is finally accepted as "good" if the corresponding sample element satisfies the allocation rule. The goal is to find the allocation rule that minimizes the possibility of misallocation.

The process of finding an appropriate allocation rule must be repeated for each specification. The allocation rules basically consist of a linear combination of the primary measurements and an accompanying threshold. The weights of the linear combination are

a result of the discrimination analysis, as well as the threshold, which can be adjusted with preference to either the yield or the fault coverage.

These percentages are the two major indices of the quality of the resulting test design. The *fault coverage* is calculated as the ratio of correctly as faulty qualified circuits and the total number of faulty circuits. It is indirect proportional to the number of test escapes. The *yield coverage* is calculated as the ratio of correctly as good qualified circuits and the total number of good circuits. This accounts for the good circuits that are wrongly rejected by the designed test criteria. The closer these two quality indices approach 100%, the higher is the quality of the resulting test.

We will contrast in Section 7 the final test quality in terms of the yield and fault coverage that can be achieved for each specification with the resolution of the test equipment in terms of the number m of bits of the ADC. For the first time this relationship is established.

6 Consideration of catastrophic faults

Since the test design is primarily aimed at detecting the very subtle parametric faults, we confidently turn to the detection of catastrophic faults, which are usually considered to be much more easily testable [18]. In the previous section we included the statistical parameters in our circuit simulations to model parametric faults. In this section all the parameters are left at their nominal value, but to model catastrophic faults the net list is altered to accommodate the most common transistor defects: gate to drain short, gate to source short, open source contact, and open drain contact [16]. Only one of these faults is included at a time.

A catastrophic fault may be discernible by the loss of functionality or a degraded performance. To compare our results with specification testing, two sets of simulation results are assembled. On the one hand, specification tests are run to verify whether specifications are violated in the presence of a circuit fault and thus whether the fault can be discovered by means of specification testing. On the other hand, alternative tests with IDD measurements are run to evaluate the possibility of disclosing the fault via the testing method suggested in this paper.

From these results we can deduce how a parametric test design compares to specification testing when trying to detect catastrophic faults. E. g. for our circuit example we can show that all faults that lead to a violation of any of the specifications can be detected via IDD spectrum testing. In accordance to [11], catastrophic faults can be very well detected by application of parametric test criteria which are based on most sensitive measurements.

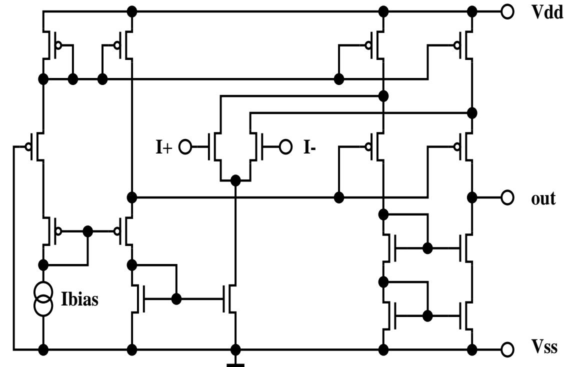

Figure 3: **Operational amplifier as circuit under test**

Table 1: **Circuit performances and their specification bounds**

GBW	SR_+	SR_-	ΔV_{out}
> 3.0 MHz	> 3.5 V/μs	> 3.5 V/μs	> 3.0 V

7 Experimental results

As circuit under test we chose the operational amplifier whose schematic is shown in Fig. 3. Its four specifications are given in Table 1. Three types of specifications –DC, AC, and transient– are covered. The temperature at which all specifications had to be guaranteed was 100°C. For the simulation of the IDD measurements we set the ambient temperature in the circuit model to 30°C. The amplitude of the input signal was kept at 1 V.

The combinations of base frequency and DC offset of the input stimuli can be derived from Table 2. It is a subset of stimuli that was selected according to Section 2. Since the table has eight different entries and we considered eight coefficients obtained by the DFT, namely the DC value, the fundamental, and the first six harmonics, we had a reservoir of sixty-four primary measurements.

Since the quantization error is systematically considered in the test design, we may include the comparably large number of coefficients in our set of mea-

Table 2: **Set of test input stimuli considered for the test design**

DC offset U_{DC} [V]	Frequency f_0 [kHz]			
1.5	1.00			300
2.5	1.00	2.59	44.8	300
3.5	1.00			300

surements. Those harmonics that cannot be determined with sufficient accuracy are removed by the algorithm and can have no detrimental effect on the test quality or robustness.

Following the circuit analysis described in [17] we determined the worst-case points for each specification. The worst-case point is the closest point in the space of statistical parameters (geometrically "close" with respect to parameter correlations and variances) at which the circuit performance reaches the bound set by its specification.

For each specification we ran Monte-Carlo simulations centered around the worst-case point (with a sample size of 200), which together with Monte-Carlo simulations centered at the nominal point (with again a sample size of 200), constituted the training sample for the corresponding discrimination analysis. The verification was accomplished with a set of Monte-Carlo simulations with a sample size of 500.

According to Eq. (2) we calculated the measurement error for different word sizes of the analog-digital converter. For each word size we reduced the number of measurements used by obeying the rule given at the end of Section 3 and by examining subsequent runs of the discrimination analysis (Section 5) where the number of measurements used was varied. The later implies that for each word size and for each specification there is a minimum number of measurements where test quality can be no more improved by increasing this number.

Fig. 4 depicts graphically the situation at such a point. In the case of a 10 bit ADC and regarding specification "SR_+" the usual trade-off between yield and fault coverage can be satisfactorily solved, i. e. the test quality peaks at 100% for the optimum test threshold.

Table 3 provides the details where we employ a generic value calculated as the quadratic mean of the yield and fault coverage to gauge the test quality. Table 4 lists the total number of catastrophic faults, the number of faults detected by specification testing, and the number of faults detected by the testing method

Table 3: **Word size of the ADC versus test quality**

# of Bits	GBW	SR_+	SR_-	ΔV_{out}	total
8	99.5%	85.7%	99.9%	96.5%	81.9%
10	99.6%	100%	100%	98.5%	98.3%
12	99.7%	100%	100%	99.9%	99.7%
14	100%	100%	100%	100%	100%
16	100%	100%	100%	100%	100%

Table 4: **Results for catastrophic faults**

	Nr.	Perc.
Total number of faults considered	46	100%
Specification testing	46	100%
IDD measurements	46	100%

described above. In Table 3 and 4 it becomes apparent that our method yields outstanding results with respect to parametric as well as catastrophic faults.

8 Conclusions

We have shown that IDD measurements are a wieldy instrument to detect both, parametric and catastrophic faults. If the set of measurements is based upon the power supply spectrum, the circuit under test can be readily checked against all given specifications and a list of catastrophic faults. The

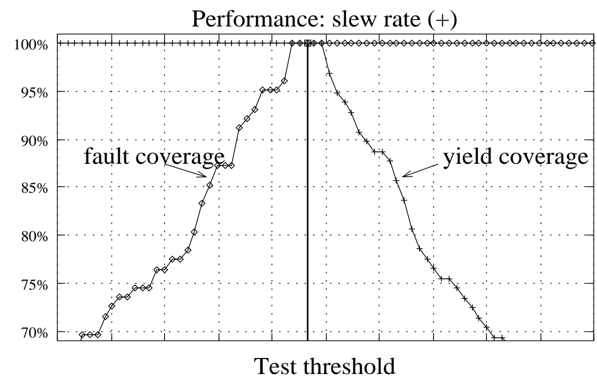

Figure 4: **Yield and fault coverage for specification "SR_+" versus test threshold**

amount of on-line calculation needed can be kept low. The detectability of parametric faults, expressed in a high fault and yield coverage, depends on the quality of the ADC. However, it is possible to construct a robust testing procedure using discrimination analysis based upon Fourier coefficients as the set of measurements. A reasonable yield and fault coverage can be obtained, underlining the importance of IDD measurements for mixed-signal testing.

References

[1] Phil Nigh and Wojciech Maly. Test generation for current testing. *IEEE Design & Test of Computers*, pages 26–38, February 1990.

[2] J. Soden, C. Hawkins, R. Gulati, and W. Mao. IDDQ testing: A review. *Journal of Electronic Testing*, 3(4):291–304, 1992.

[3] D. Camplin, I. Bell, G. Taylor, and B. Bannister. Can supply current monitoring be applied to the testing of analog as well as digital portion of mixed ASICs. In *European Conference on Design Automation (EDAC)*, pages 538–542, 1992.

[4] J. S. Beasley, H. Ramamurthy, J. Ramirez-Angulo, and M. DeYong. Fault detection in VLSI circuits using IDD spectrum analysis. *European Conference on Circuit Theory and Design (ECCTD)*, pages 659–664, 1993.

[5] Zhihua Wang, Georges Gielen, and Willy Sansen. Testing of analog circuits based on power–supply current monitoring and discrimination analysis. In *IEEE Asian Test Symposium (ATS)*, pages 126–131, November 1994.

[6] G. Gielen, Z. Wang, and W. Sansen. Fault detection and input stimulus determination for the testing of analog integrated circuits based on power-supply current monitoring. In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 495–498, November 1994.

[7] R. C. Aitken, K. M. Butler, R. L. Campbell, B. K. Koenemann, W. Maly, W. Needham, and Y. Zorian. Deep-submicron test. *IEEE Design & Test of Computers*, pages 102–108, fall 1996.

[8] D. Papakostas and A. Hatzopoulos. Analogue fault identification based on power supply current spectrum. *Electronics Letters*, 29(1):118–119, 1993.

[9] P. Fieler and N. Loverro. Defects tail off with six-sigma manufacturing. *IEEE Circuits and Devices Magazine*, 7(5):18–20,48, September 1991.

[10] M. Soma. Challenges in analog and mixed–signal fault models. *IEEE Circuits and Devices Magazine*, pages 16–19, January 1996.

[11] Walter M. Lindermeir. Design of robust test criteria in analog testing. In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 604–611, November 1996.

[12] W.M. Lindermeir, H.E. Graeb, and K.J. Antreich. Design based analog testing by characteristic observation inference. In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 620–626, November 1995.

[13] Joseph A. Mielke. Frequency domain testing of ADCs. *IEEE Design & Test of Computers*, pages 64–69, spring 1996.

[14] Athanasios Papoulis. *Probability, Random Variables and Stochastic Processes*. McGraw-Hill, 1991.

[15] B. R. Epstein, M. Czigler, and S. R. Miller. Fault detection and classification in linear integrated circuits: An application of discrimination analysis and hypothesis testing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems CAD*, 12:102–113, 1993.

[16] L. Milor and V. Visvanathan. Detection of catastrophic faults in analog integrated circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems CAD*, 8:114–130, 1989.

[17] K. Antreich, H. Graeb, and C. Wieser. Circuit analysis and optimization driven by worst-case distances. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems CAD*, 13:57–71, 1994.

[18] L. Milor and A. L. Sangiovanni-Vincentelli. Minimizing production test time to detect faults in analog circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems CAD*, 13:796–813, 1994.