Optimized Implementations of the Multi-Configuration DFT Technique for Analog Circuits

M. Renovell, F. Azaïs and Y. Bertrand
Laboratoire d'Informatique Robotique Microélectronique de Montpellier LIRMM-UMII
Université de Montpellier II : Sciences et Techniques du Languedoc
UMR C5506 CNRS - 161 Rue Ada 34392 Montpellier Cédex 5 FRANCE
Tel:(33)467418523 Fax:(33)467418500 Email: renovell@lirmm.fr

Abstract: *The paper describes an approach to optimize the application of the multi-configuration DFT technique for analog circuits. This technique allows to emulate the circuit in a number of new test configurations targeting the maximum fault coverage. The brute force application of the multi-configuration is shown to produce a very significant improvement of the original poor testability. An optimized approach is proposed to apply this DFT technique in a more refined way. The optimization problem consists in choosing among the various permitted test configurations, a set that leads to the best testability/cost trade-off. This set is selected according to ordered requirements: (i) the fundamental requirement of maintaining the maximum fault coverage and (ii) non-fundamental requirements of satisfying some user-defined cost functions such as test time, silicon overhead or performance degradation. Results are given that exhibit very interesting features in terms of either test procedure simplicity or DFT penalty reduction.*

1. Introduction

A number of Design For Testability (DFT) techniques have been presented in literature to make the test of analog circuits easier. Among them, techniques based on a Divide-and-Conquer approach are very popular in that sense that they propose a natural partitioning of the device under test into simpler functional blocks. In the context of analog circuits, the use of mux function allows to directly implement such a partitioning [1,2]. In this case, the complex problem of testing the complete circuit may be replaced by the simpler problem of separately testing the internal functional blocks. To access a given Block Under Test (BUT), another approach may be to reconfigure the circuit in order to facilitate the signal propagation through the other blocks. Several techniques have been proposed in case of opamp-based circuits [3,4,5].

In particular, the multi-configuration [6] proposes to modify opamps in order to emulate them in a follower mode. This ensures the full controllability/observability of any BUT by making all the other blocks transparent. Moreover, the multi-configuration has been shown to be also applicable at finer scale on the very inside of the BUT, whatever its structural complexity. For instance, the BUT may consist in a number of opamp-based stages connected in a non-cascaded way (feedback links may exist).

The present paper deals with the test of such a complex block regardless its accessibility. The global objective is to optimize the DFT in order to ensure a maximum testability with a minimum penalty. More precisely, we want to profit the advantage of the multi-configuration that creates new test configurations implementing new circuit functionalities. The optimization problem consists in choosing among the various test configurations a set that leads to the best testability/cost trade-off. Basically the first thing to do is to ensure the full testability. So, the fundamental and imperative requirement is to reach the maximum fault coverage. In general, several configuration sets are found that fulfill this requirement. At this point, we have the opportunity to introduce a user-defined cost function to continue the optimization process. As an example, two different objectives are targeted in this paper, either to limit the test complexity or to reduce the DFT impact on the circuit.

The paper is organized as follows. Section 2 proposes a metric to evaluate the analog circuit testability, based on the study of fault detectability in the frequency domain. This metric is refined by the introduction of the ω-detectability concept to express how easily a fault can be detected. In section 3, we describe the multi-configuration technique and demonstrate its efficiency in terms of testability improvement. The main contribution of the paper is presented in section 4. The optimized application of the multi-configuration is detailed using the fundamental requirement and two examples of user-defined cost functions. Finally, section 5 gives some concluding remarks.

2. Analog circuit testability evaluation

Most published testability evaluation methods for analog circuits are based on measurements of the degree of solvability of the fault diagnosis equations [7,8,9,10]. If diagnosis evaluation is not the objective, a different approach has been proposed by Slamani and Kaminska [11]. This approach is based on the analysis of the circuit in the frequency domain and uses the fault observability concept. The fault observability of a component x_i is defined as the sensitivity of the output measured parameter

T with respect to the variations of component x_i. The fault observability is then a function of frequency and, as stated in [12], if the sensitivity at a given test frequency is high enough, then the fault produces a measurable change on the output value and can be detected.

In this paper, we propose to use a similar approach to evaluate the testability of an analog circuit: for a given fault list, we perform the analysis of the fault-free and faulty frequency responses. This analysis is conducted using HSPICE simulations, and we determine the relative deviation of each faulty response with respect to the nominal one. Then, instead of using the fault observability parameter, we define a new binary parameter, called the fault detectability parameter.

Definition 1: a fault f_j is detectable (*i.e.* $Det_{fj} = True$), if it exists at least one frequency ω_f for which the relative deviation of the frequency response $\Delta T/T(\omega)$ is higher than a given relative tolerance ε (this tolerance allows to take into account possible fluctuations in the process environment).

Using this fault detectability parameter, it is now easy to determine the maximum fault coverage that can be achieved for the circuit, as the ratio between the number of detectable faults over the total number of faults taken into consideration.

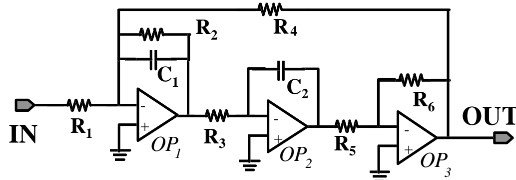


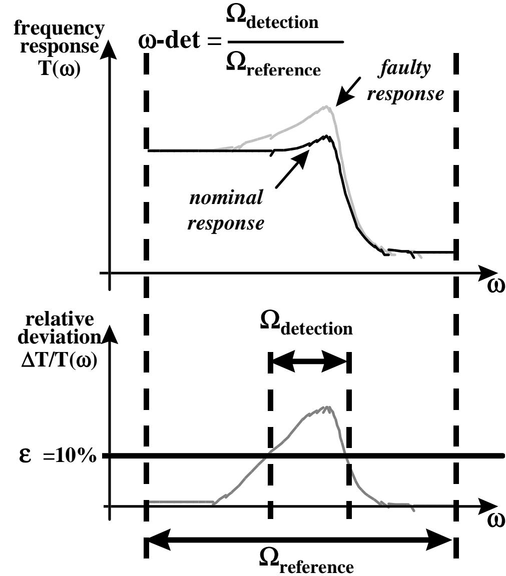
Figure 1: Biquadratic filter

For the sake of clarity, this approach is illustrated on the very simple example of the biquadratic filter depicted in figure 1. As an example, we have chosen to study the detection of soft faults on passive components, and more especially the 20% deviations from the nominal value for all resistors and capacitors. The tolerance ε is arbitrarily fixed at 10%. Fault simulation results show that only the faults on resistors R_1 and R_4 are detectable. This corresponds to a poor testability with a fault coverage $FC_{filter} = 25\%$.

Definition 1 corresponds to a boolean concept of detectability or non-detectability. In order to obtain a more refined evaluation of the circuit testability, we introduce a new parameter called the ***ω-detectability***. This parameter is defined for each fault and takes into account how easily the fault can be detected: in addition to the fault detectability parameter, we consider the frequency region where the fault is detectable and we define the detectability region $\Omega_{detection}$.

Definition 2: The ω-detectability of fault f_j is equal to the detectability region $\Omega_{detection}$ of fault f_j, normalized by the reference frequency region $\Omega_{reference}$ (cf. figure 2).

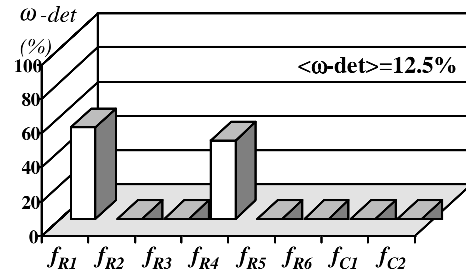
The reference frequency region $\Omega_{reference}$ is chosen in such a way that it contains the mean useful information about the frequency response (say, about two orders of magnitude in the passband and two orders of magnitude in the stopband). In fact, because only the relative variation of ω-detectability will be exploited, the absolute value of $\Omega_{reference}$ is not critical.



2: The ω-detectability concept

In other words, the ω-detectability of fault f_j represents the probability of detecting the fault when applying a random frequency sine signal as a test stimulus. This parameter is then representative of the testability of fault f_j and can be very useful for automatic test generation procedures based on a frequency approach such as [12] and [13].

With this new parameter, we can now evaluate more precisely the testability of the biquadratic filter: for each deviation fault, we compute the associated ω-detectability. Results are presented in graph 1.



Graph 1: ω-det graph for the biquadratic filter

Looking at this ω-detectability graph, it can be seen that the 20% deviations on passive components R_2, R_3, R_5, R_6, C_1 and C_2 are not ω-detectable. On the contrary, the 20% deviations on R_1 and R_4 are partially ω-detectable. The average ω-detectability rate for the complete fault list

is then *<ω-det>=12.5%* and can be considered as a rough image of the filter testability. This value is quite low and we plan to show that a great improvement can be achieved using a DFT technique.

3. Analog testability improvement

To improve the testability of an analog circuit, we have prospected an issue based on the reconfiguration concept: the idea is to create new test configurations in which the circuit functionality is modified [6]. These test configurations may be useless in a functional point of view, but efficient in terms of testability enhancement. This corresponds to a widening of the functional space, and, it is of course expected that the new functional space exhibits better testability properties than the initial functional space.

3.1 Multi-configuration principle

The basic element of our DFT technique is the configurable opamp. The principle is illustrated in figure 3. Depending on the logic value applied on its selection line, the configurable opamp can be emulated in two distinct modes. In the normal mode (*i.e. sel=0*), the configurable opamp works as a classical one. In the follower mode (*i.e. sel=1*), the opamp is configured as a follower so that any signal applied on the additional test input is propagated to the output without any modification, assuming of course that the opamp bandwidth limitation is not reached. Different implementations of this configurable opamp have been proposed, based either on the addition of switches around the opamp [14], or on the duplication of the opamp input stage [15].

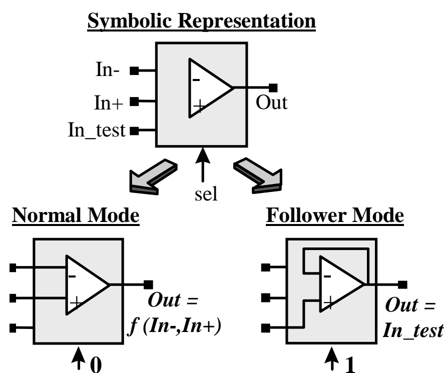


Figure 3: Configurable opamp principle

The reconfiguration-based DFT technique we propose implements the systematic replacement of classical opamps by configurable opamps, as illustrated in figure 4. The additional *In_test* inputs are connected so that we create a chain of configurable opamps from the primary input to the primary output. So, depending on the logic values applied on the selection lines sel_i, one can choose to configure some opamps into their follower mode while others operate in normal mode. It is then possible to activate the circuit in various configurations in which the circuit functionality is altered.

The circuit configuration is determined by the set of logic values applied on the three selection lines; we call this set the configuration vector $CV=(sel_1\ sel_2\ sel_3)$. The DFT-modified biquadratic filter can then be emulated in $2^3=8$ distinct configurations: in addition to the functional configuration C_0, 7 new test configurations are permitted, as listed in table 1.

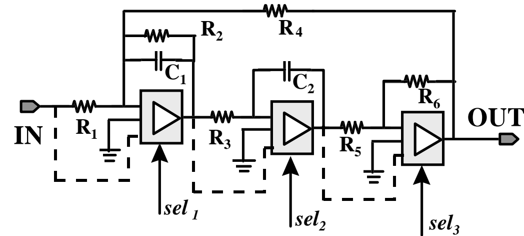


Figure 4: DFT-modified biquadratic filter

Note that it exists a particular configuration C_7, called the transparent configuration in which the circuit performs the identity function: all the configurable opamps are turned into their follower mode and any signal applied on the circuit input is directly propagated to the output. This configuration obviously does not permit the detection of the faults on passive components, but is used to test faults inside opamps [5]. Because only faults on passive components are under consideration, only configurations C_0 to C_6 will be used in the remaining of the paper.

Conf	Vector	Description
C_0	000	Funct. Conf
C_1	001	New Test Conf
C_2	010	New Test Conf
C_3	011	New Test Conf
C_4	100	New Test Conf
C_5	101	New Test Conf
C_6	110	New Test Conf
C_7	111	Transp. Conf

Table 1: Configuration table

3.2 Testability improvement evaluation

To evaluate the testability improvement introduced by the DFT technique, we study fault detection in each possible configuration, using the same procedure as in the previous section. Results of fault detectability are given in figure 5, in terms of a fault detectability matrix (d_{ij}). Line i corresponds to the test configuration C_i and column j to the fault f_j. The matrix coefficient d_{ij} is a boolean that is true ("1") if fault f_j is detectable in configuration C_i. Note that this coefficient corresponds to the detectability definition given in section 2.

This fault detectability matrix clearly points out that our DFT technique permits a great improvement of the filter testability, since all the non-detectable faults in the functional configuration C_0 are detectable in at least one of the new test configurations. So, as expected, by widening the functional space of the analog circuit, we get an

increase of fault coverage and it becomes possible to achieve the maximum fault coverage $FC_{DFT\text{-}mod.\,filter}$=**100%**.

	f_{R1}	f_{R2}	f_{R3}	f_{R4}	f_{R5}	f_{R6}	f_{C1}	f_{C2}
C_0	1	0	0	1	0	0	0	0
C_1	0	0	1	0	1	1	0	1
C_2	1	1	0	1	1	1	1	0
C_3	0	0	0	0	1	1	0	0
C_4	1	1	1	1	1	0	0	0
C_5	0	0	1	0	0	0	0	1
C_6	1	1	0	1	0	0	0	0

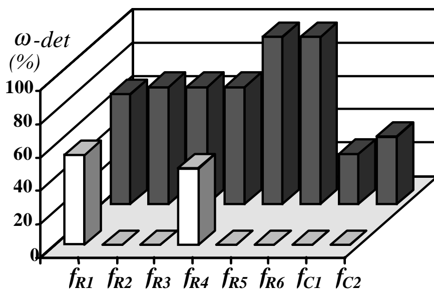
Figure 5: Fault detectability matrix

In the same way we have determined the ω-detectability associated to each fault for the initial filter, we compute the ω-detectability associated to each fault for the DFT-modified filter in the different configurations. Results are reported in table 2.

Conf	f_{R1}	f_{R2}	f_{R3}	f_{R4}	f_{R5}	f_{R6}	f_{C1}	f_{C2}
C_0	54	0	0	46	0	0	0	0
C_1	0	0	30	0	30	30	0	30
C_2	30	30	0	30	30	30	30	0
C_3	0	0	0	0	100	100	0	0
C_4	14	70	70	70	70	0	0	0
C_5	0	0	40	0	0	0	0	40
C_6	66	40	0	40	0	0	0	0

Table 2: ω-detectability table

For any fault, it exists at least a test configuration that enhances the ω-detectability. To qualify the global testability improvement at the circuit level, a fault is assumed to be tested in the best case, i.e. the test configuration in which the fault exhibits the higher ω--detectability value (black boxes). The corresponding results are summarized in graph 2 where the ω-detectability reported for the DFT-modified filter corresponds to the maximum ω-detectability value obtained for configurations C_0 to C_6.



Graph 2: ω-det for the DFT-modified filter

This graph clearly illustrates the testability improvement brought by the reconfiguration-based DFT technique. Indeed, whatever the faulty component, the ω-detectability is always higher when using the new test configurations than in the functional one. So, not only the DFT technique permits to detect faults that are non-detectable for the initial filter but also introduces a widening of the detectability region associated to each fault. As a consequence, the average ω-detectability rate increases from 12.5% for the initial filter up to 68.3% for the DFT-modified filter. This improvement is of prime importance with regard to the test stimulus generation issue.

4. DFT technique optimization

It has been pointed out in the previous sections that the multi-configuration technique greatly improves the circuit testability by means of new test configurations. Up to now, this technique has been applied in a very systematic way considering all the 2^n possible configurations, and this can be viewed as a brute force application. Now, the purpose of this section is to propose a more refined solution by optimizing the application of the multi-configuration technique.

It is clear that a more refined solution must mandatorily maintain the maximum fault coverage. This 1st-order requirement is a fundamental requirement for any optimization approach. The proposed optimization process then consists in first, identifying all the possible solutions that satisfy the fundamental requirement, and second, choosing one of these possible solutions according to some 2nd-order and 3rd-order requirements. These non-fundamental requirements can be defined independently of the fundamental one.

4.1 Fundamental requirement

The first step of the process consists in identifying all the possible solutions that satisfy the fundamental requirement. In other words, we have to determine all the combinations of test configurations that cover all the detectable faults. This is a classical coverage problem formulated by means of a boolean expression ξ :

$$\xi = \prod_{f_j} \left(\sum_{C_i} d_{ij} * C_i \right)$$

where d_{ij} is the boolean coefficient of the detectability matrix (section 3).

For the biquadratic filter, considering the fault detectability matrix given in figure 5, it comes:

$$\xi = \underbrace{(C_0 + C_2 + C_4 + C_6)}_{f_{R1}}\underbrace{(C_2 + C_4 + C_6)}_{f_{R2}}\underbrace{(C_1 + C_4 + C_5)}_{f_{R3}}\underbrace{(C_0 + C_2 + C_4 + C_6)}_{f_{R4}}$$
$$\underbrace{(C_1 + C_2 + C_3 + C_4)}_{f_{R5}}\underbrace{(C_1 + C_2 + C_3)}_{f_{R6}}\underbrace{(C_2)}_{f_{C1}}\underbrace{(C_1 + C_5)}_{f_{C2}}$$

As illustrated above, each factor corresponds to a given fault. The ξ expression is satisfied if all the faults are detected according to the logic AND of all the factors. Each factor implements the logic OR of all the configurations that permits to detect the corresponding fault. As an example, the first factor expresses that fault f_{R1} can be detected using either configuration C_0, C_2, C_4 or C_6 .

It appears in the ξ expression that fault (f_{C1}) is detectable in one and only one configuration (C_2). This corresponds to the f_{C1} column with a single "1" in the detectability matrix, and the C_2 configuration is then called an ***essential configuration***. To satisfy the initial fundamental requirement (maximum fault coverage), such a configuration must mandatorily appear in the final configuration set. So, the first step of the optimization procedure consists in identifying essential configurations. For instance, $\xi_{ess.} = (C_2)$ for the biquadratic filter under study.

The objective in now to complete this set with non-essential configurations that cover faults that are non-detectable in the essential configuration. This classical coverage problem can be formulated in a simplified form, using a reduced fault detectability matrix. As illustrated in figure 6, this reduced matrix is obtained by skipping all the faults covered by the essential configuration.

Essential configuration: C_2

$f_{R1}, f_{R2}, f_{R4}, f_{R5}, f_{R6}, f_{C1}\}$ ⇨

$$\begin{array}{c} \\ C_0 \\ C_1 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \end{array} \begin{array}{c} f_{R3} \quad f_{C2} \\ \begin{bmatrix} 0 & 0 \\ 1 & 1 \\ 0 & 0 \\ 1 & 0 \\ 1 & 1 \\ 0 & 0 \end{bmatrix} \end{array}$$

Figure 6: Reduced fault det. matrix

Starting with this new matrix, we can derive the complementary boolean expression $\xi_{compl.}$, in the same way as for the previous ξ expression :

$\xi_{compl.} = (C_1 + C_4 + C_5).(C_1 + C_5)$.

Finally the ξ expression may be written as :

$\xi = \xi_{ess.}.\xi_{compl.} = (C_2).(C_1 + C_4 + C_5).(C_1 + C_5)$.

Developing this expression, we obtain the classical ***sum of product*** form:

$$\xi = C_1.C_2 + C_1.C_2.C_5 + C_1.C_2.C_4 + C_2.C_4.C_5 + C_2.C_5$$

In this sum of product expression, the logic OR function indicates that different solutions are permitted. According to the initial requirement, each of these solutions (product terms) ensures the maximum FC. The choice of a given solution is now part of an optimization process performed according to a 2nd-order requirement.

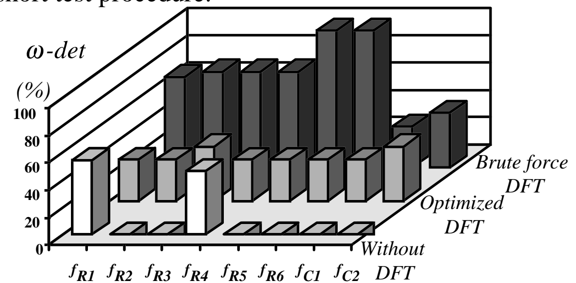
4.2 Configuration number optimization

This section considers an example of 2nd-order requirement related to the number of configurations: we want to select the minimum number of test configurations in order to simplify the test procedure complexity. Indeed, the smaller the number of configurations, the shorter the test procedure and test time. Furthermore, if BIST is under consideration, configurations are generated on-chip, and the minimization of the configuration number then simplifies the required test circuitry.

Considering this 2nd-order constraint, we note that the ξ expression directly translates the number of configurations. Consequently, it is just necessary to choose the product term that contains the minimum number of literals. So, for the biquadratic filter we obtain two possible minimal test configuration sets, namely $\{C_1, C_2\}$ and $\{C_2, C_5\}$. These two sets are completely equivalent, since they ensure the maximum fault coverage and present the same number of configurations.

Considering that we still have two possibilities for the choice of a minimal set, a 3rd-order requirement can be defined. Actually, we suggest to use ω-detectability results to guide the last choice. Indeed, we have seen in the previous section that the average ω-detectability rate indicates how easily the circuit can be tested. We then propose to select the test configuration set that leads to the higher average ω-detectability rate. According to table 2, the solution $\{C_1, C_2\}$ gives <ω-det>=30% and solution $\{C_2, C_5\}$ gives <ω-det>=32.5%. Using the 3rd-order requirement, the optimal test configuration set for the biquadratic filter is $S_{opt} = \{C_2, C_5\}$, and results in terms of ω-detectability are given in graph 3.

Graph 3 reports the ω-detectability of each fault in the initial circuit without DFT (white), in the modified circuit with a brute force DFT application (black) and in the modified circuit with the optimized application (grey). It appears that the fundamental requirement is respected for the two modified circuits since all the faults are partially ω-detectable. Note that only 2 configurations are permitted in the optimized solution while all the 8 configurations are permitted in the brute force application, leading to a lower average ω-detectability rate. This is the cost to be paid for a short test procedure.



Graph 3: ω-detectability for the optimized DFT

4.3 Configurable opamp optimization

This section considers another example of 2nd-order constraint related to the number of configurable opamps. Indeed, the proposed DFT technique consists in replacing the original opamps by configurable opamps. Due to their additional switches, the configurable opamps have an impact on both the circuit area and the nominal performances. Our objective is now to try to reduce the number of original opamps that need to be replaced by configurable opamps. In fact, we are looking for a ***partial DFT*** solution in order to obtain the best cost/performance trade-off. This ***partial DFT*** implies to select, among the possible test configuration sets that respect the

fundamental requirement, a set that minimizes the number of configurable opamps.

The starting point is again all the possible test configuration sets given by the boolean expression:

$\xi = C_1.C_2 + C_1.C_2.C_5 + C_1.C_2.C_4 + C_2.C_4.C_5 + C_2.C_5$

However, this expression is not convenient to deal with the problem of configurable opamp optimization, since only configurations are represented in the different product terms and opamps do not appear explicitly. So, we have to perform a mapping between configurations and opamps. This mapping can be realized through the configuration vectors.

Indeed, let us consider a given configuration and its associated configuration vector. For instance, configuration C_5 is activated by the vector (*1 0 1*), each bit corresponding to a given opamp (see table 1). In this configuration, opamps OP_1 and OP_3 are turned into their follower mode while opamp OP_2 operates as a classical opamp. It is then mandatory to use configurable opamps for OP_1 and OP_3, but not for OP_2. So, the mapping we propose consists in replacing a configuration, by the product of the opamps operating in follower mode: for instance C_5 is replaced by $OP_1.OP_3$. The complete correspondence for the mapping is given in table 3.

Conf	Conf Op
C_0	-
C_1	Op1
C_2	Op2
C_3	Op1 Op2
C_4	Op3
C_5	Op1 Op3
C_6	Op2 OP3

Table 3: Mapping table

Substituting the configurations for the opamps into expression ξ , it comes:

$$\xi = C_1.C_2 + C_1.C_2.C_5 + C_1.C_2.C_4 + C_2.C_4.C_5 + C_2.C_5$$

$$\xi^* = OP_1.OP_2 + OP_1.OP_2.OP_3 + OP_1.OP_2.OP_3 + OP_1.OP_2.OP_3 + OP_1.OP_2.OP_3$$

The ξ^* expression now directly expresses the number of configurable opamps. Consequently, it is just necessary to choose the product term that contains the minimum number of literals. So, the optimal solution for the biquadratic filter is to modify opamps OP_1 and OP_2 into configurable opamps and to keep opamp OP_3 as a classical opamp. This implementation is illustrated in figure 7.

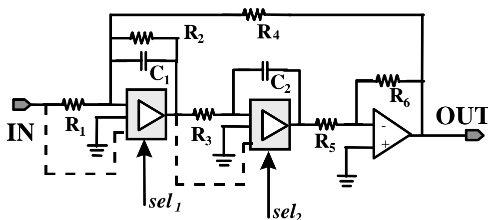


Figure 7: Partial DFT implementation

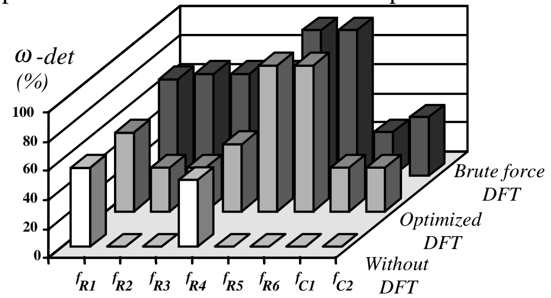
The resulting circuit respects the 2nd-order requirement since it includes only 2 configurable opamps. The two opamps allow to emulate 4 distinct test configurations. Of course the previous C_1 (10-) and C_2 (01-) configurations are included into these 4 test configurations, and consequently, the fundamental requirement is also respected. Note that the two previous requirements do not imply any limitation concerning the number of permitted test configurations.

Considering that we still have the choice of using or not configurations C_0 and C_3, a 3rd-order requirement can be defined. As previously, we suggest to use ω-detectability results to guide the last option. Table 4 shows that the maximum average ω-detectability rate is obtained by using the 4 test configurations.

Conf	f_{R1}	f_{R2}	f_{R3}	f_{R4}	f_{R5}	f_{R6}	f_{C1}	f_{C2}
C_0 (00-)	54	0	0	46	0	0	0	0
C_1 (10-)	0	0	30	0	30	30	0	30
C_2 (01-)	30	30	0	30	30	30	30	0
C_3 (11-)	0	0	0	0	100	100	0	0

Table 4: ω-detectability table

Full and partial DFT solutions are compared in graph 4 in terms of ω-detectability results. Both of these solutions permit to reach the maximum fault coverage since all the faults are partially ω-detectable. However, using the optimized implementation, the average ω-detectability rate is reduced from 68.3% to 52.5%. This is the price to be paid for implementing a DFT solution with a reduced impact on both silicon area and circuit performances.



Graph 4: ω-det for the partial DFT

5. Discussion and Conclusion

In this paper, an optimization approach is proposed for optimal application of the multi-configuration DFT technique for analog circuits. Two metrics are firstly proposed for the testability evaluation of an analog block. The first metric corresponds to the "boolean" concept of fault detectability or non-detectability while the second one corresponds to a more "analog" concept of fault testability indicating how easy detectable a given fault is.

The multi-configuration technique applied on a circuit example is found to produce a very significant improvement of the original poor testability. An optimized approach is then proposed to apply this DFT technique in a

more refined way by considering in details the different test configurations. From the exhaustive set of test configurations, we propose to select a subset according to some ordered requirements:

- the first and fundamental requirement consists in ensuring that the subset of selected configurations makes all the faults under consideration detectable,
- the non-fundamental requirements consist in satisfying user-defined cost functions such as test time, silicon overhead or performance degradation.

A very simple example of circuit has been used to illustrate the proposed optimization technique. In the original biquadratic filter, only 25% of the considered faults are detectable. After application of the multi-configuration technique, all the faults are detectable by means of the 2^3 different test configurations. These 2^3 test configurations present some redundancy with regards to fault detectability in such a way that configuration optimization can take place.

Using a classical approach for coverage problem solving, it is shown that different sets of 2 or 3 test configurations allow to reach the maximum fault coverage of 100%. Any of these sets satisfying the fundamental requirement, an optimal choice is performed using a user-defined cost function. The first example of cost function concerns test time through the number of emulated configuration during the test phase; the minimal solution includes only 2 test configurations that cover all the considered faults. The second example of cost function concerns silicon and performance impact through the number of modified opamps; the minimal solution necessitates only 2 configurable opamps and all the fault are detectable using the 4 corresponding test configurations. As a result, this partial DFT implementation presents very interesting features when compared to the brute force application.

This small example demonstrates the validity of the proposed optimization approach. Its viability through consideration of more complex analog circuits is currently under development in our lab. It is clear that the bottleneck of the approach stands in the fault detectability matrix construction that implies extensive fault simulation. A possible solution under study consists in using structural information to select a first subset of configurations that will be candidate for the simulation process.

6. References

[1] K. Wagner and T. Williams, "Design For Testability of Mixed-Signal Integrated Circuits", *Proc. Int. Test Conference*, pp. 823-828, 1988.

[2] P. Fasang, D. Mullins and T. Wong, "Design For Testability for Mixed Analog/Digital ASICs", *Proc. IEEE Custom Integrated Circuits Conference*, paper 16.5, 1988.

[3] M. Soma, "A Design-For-Test Methodology for Active Analog Filters", Proc. Int. Test Conference, pp. 566-573, 1990.

[4] D. Vazquez, A. Rueda, J.L. Huertas and A.M. Richardson, "Practical DFT Strategy for Fault Diagnosis in Active Analog Filters", Electronics Letters, Vol. 31, No. 15, pp. 1221-1221, July 1995.

[5] M. Renovell, F. Azaïs and Y. Bertrand, "A Design-For-Test Technique for Multi-Stage Analog Circuits", Proc. Asian Test Symp., pp. 113-119, 1995.

[6] M. Renovell, F. Azaïs and Y. Bertrand, "The Multi-Configuration: A DFT Technique for Analog Circuits", Proc. IEEE VLSI Test Symp., pp. 54-59, 1996.

[7] N. Sen and R. Saek, "Fault Diagnosis for Linear System via Multifrequency Measurement", IEEE Trans. on Circuits and Systems, Vol. CAS-26, pp. 456-457, July 1979.

[8] G. Iuculano, A. Liberatore, S. Manetti and M. Marini, "Multifrequency Measurement of Testability with Application for Large Linear Analog Systems", IEEE Trans. on Circuits and Systems, Vol. CAS-33, June 1986.

[9] R. Carnassi, M. Catelani, G. Iuculano, A. Liberatore, S. Manetti and M. Marini, "Analog Network Testability Measurement: A Symbolic Formulation Approach", IEEE Trans. Instrum. and Meas., Vol. 40, No. 6, pp. 930-935, December 1991.

[10] J. Hemink, B. Meijer and H. Kerkhoff, "Testability Analysis of Analog Systems", IEEE Trans. on Computer Aided Design, Vol. 9, No. 6, pp. 573-583, June 1990.

[11] M. Slamani and B. Kaminska, "Multifrequency Testability Analysis for Analog Circuits", Proc. IEEE VLSI Test Symp., pp. 54-59, 1994.

[12] N. Nagi, A. Chatterjee, A. Balivada and J.A. Abraham, "Fault-Based Automatic Test Generator for Linear Analog Circuits", Proc. Int. Conf. on Computer Aided Design, pp. 88-91, 1993.

[13] S. Mir, M. Lubaszewski, V. Kolarik and B. Courtois, "Automatic Test Generation for Maximal Diagnosis of Linear Analog Circuits", Proc. European Design & Test Conf., pp. 254-58, 1996.

[14] M. Renovell, F. Azaïs and Y. Bertrand, "A DFT Technique to Fully Access Embedded Modules in Analog Circuits Under Test ", Proc. IEEE Int. Mixed-Signal Testing Workshop, pp. 172-177, 1995.

[15] D. Vazquez, A. Rueda and J.L. Huertas, "A DFT Methodology for Fault Diagnosis in Active Analog Filters", Proc. IEEE Int. Mixed-Signal Testing Workshop, pp. 124-129, 1995.