Switch-Level Fault Coverage Analysis for Switched-Capacitor Systems

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ABSTRACT

An approach to test optimization in switched-capacitor systems based on fault simulation at switch-level is presented in this paper. The advantage of fault simulation at this granularity level is that it facilitates test integration as early as possible in the design of these systems. Due to their mixed-signal nature, both catastrophic and parametric faults must indeed be considered for test optimization. Adequate switch-level fault models are presented. Test stimuli and test measures can be selected as a function of fault coverage. The impact of design parameters such as switch resistance on fault coverage is studied and design parts of poor testability are located.

INTRODUCTION

The task of testing complex analog and mixed-signal parts in VLSI circuits is rapidly becoming a critical problem during the life-time of these circuits, including prototype, production and maintenance [1]. This is because analog testing has not yet reached the maturity of digital testing. There are no formal approaches that can be exploited to minimize analog testing time and no fault coverage evaluation tools are available [2].

The design of testable analog and mixed-signal VLSI circuits is becoming a must. A testable system lowers integrated circuit (IC) cost by reducing testing time during production, can have an increased field reliability by reducing the chance of early life failures, and can have higher availability by increasing fault coverage and facilitating fault diagnosis. Testability can be increased by taking into account analog design-for-testability (DFT) rules and guidelines, techniques to provide access to deeply embedded analog blocks, or techniques such as built-in self-test (BIST). As for digital circuits, test strategies should be taken into account as early as possible in the design process. During late design stages, circuit redesign for enhancing testability may be very costly.

In this paper, we analyze fault coverage in switched-capacitor systems at switch-level through the use of adequate fault models. With respect to previous works, the advantage of evaluating fault coverage at this granularity level is that integration of design and test is considered as early as possible in the design of these systems, and an increase in fault simulation speed of several orders of magnitude is achieved. Besides, we demonstrate in this work how fault coverage figures obtained at switch-level are used for tasks such as: (a) selection of the most adequate test stimuli, (b) determination of circuit parts with poor testability or with unnecessary components, (c) selection of the most adequate test measures and test thresholds, (d) comparison of alternative test approaches, and (e) quantification of impact on fault coverage of design parameters.

Previous works dealing with analog fault simulation and testability analysis are first reviewed. Next, our switch-level fault simulation approach and the fault modeling technique are presented. Fault coverage figures are used to analyze testability for the case of a switched-capacitor filter. Finally, some conclusions are provided.

TESTABILITY EVALUATION

The computation of fault coverage by means of fault simulation has usually been used as a single figure of merit for test exhaustiveness in digital circuits. Fault coverage is defined as a proportion between the number of faults than can be detected (given a certain fault list and a set of input test signals or patterns) and the total number of faults that can occur. Testing has often been considered at gate-level using fault models such as the classical stuck-at model. In the analog domain, fault simulation has been relatively uncommon. One main reason behind this has been a lack of adequate analog fault models which can lead to significative fault coverage figures. The granularity of analog fault simulation has often been limited to transistor-level using catastrophic fault models (like shorts and opens) [3, 4]. Fault simulation and test pattern generation at behavioural-level has only been considered for continuous-time linear analog circuits [5, 6].

In contrast to fault simulation, testability analysis gives a measure of the relative degree of difficulty in testing circuit nodes or key parameters for particular fault models and given test patterns. In the digital domain, this measure has often been based on some mathematical function involving controllability and observability of circuit nodes. In the analog domain, the first published measure of testability is based on determining the solvability of a set of fault diagnosis equations describing relationships between multifrequency measurements and parameters [7]. Algorithms for calculation of this measure have been presented [8, 9]. Other authors use sensitivity values of observable nodes with respect to circuit parameters as a measure of testability with the intention of selecting test frequencies for increasing fault diagnosis [10]. Analog testability analysis has normally been performed at behavioural-level, taking into account functional tests and assuming parametric deviations of circuit components. In [11], fault observability in frequency domain applicable to small-deviation, large-deviation and catastrophic faults is defined as an incremental rather than differential sensitivity at transfer-function level for continuous-time filters.

For switched-capacitor systems, fault simulation has normally been limited to transistor-level. Behavioural fault simulations have only been attempted by modeling the discrete-time circuit as an equivalent continuous-time circuit [12, 13]. However, it is known that these models are not correct for all faults that can occur in circuit

switches. On the other hand, testability analysis for switched-capacitor systems using behavioural-level methods is bound to miss large classes of catastrophic faults occurring in this type of systems. Typical faults such as a switch being stuck-on, stuck-open or shorted cannot be adequately modeled at transfer-function level for discrete-time circuits.

The difficulties for modeling catastrophic faults at behavioural-level for discrete-time circuits has lead us to consider a fault simulation approach for optimizing circuit testing. This approach is shown in Figure 1.

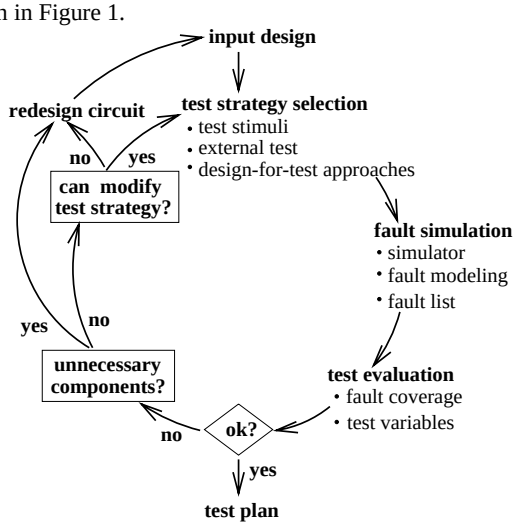


Figure 1: Optimization of circuit testing through fault coverage analysis.

Fault coverage figures provide useful information for test engineers who must place test strategies. This information includes, for example, test stimuli which are suitable for fault detection, faults which can or cannot be observed at a given test node or by a given test measure, and nodes which must be made accessible for testing. Clearly, unfavourable figures of fault coverage can lead to modification of a design. Design areas where potential testability problems may arise can be located and the impact on fault coverage of key design parameters can be studied.

SWITCH-LEVEL FAULT SIMULATION

We use a switch-level fault simulation tool called SWITTEST [14, 15] which can use both SWITCAP2 [16] and HSPICE [17] as core simulators. In this work, switch-level fault simulation is performed using SWITCAP2 (from now on SWITCAP). This is an special purpose simulator which, taking advantage of the algebraic nature of the charge-based equations of switched-capacitor networks, provides simulation algorithms very useful for both linear and mixed analog/digital switched-capacitor circuits. SWITCAP is preferred over HSPICE in the early design stages due to advantages in simulation speed, an ability to perform frequency-domain simulations which are not directly possible by means of HSPICE for switched-capacitor linear circuits, and the use of special purpose functions such as sensitivity and group-delay analysis.

SWITCAP performs switch-level simulations which result in the extraction of valuable first-order circuit characteristics. However, second-order effects such as non-zero ON resistance of switches or finite output resistance of voltage sources play a significant role once faults are present in a switched-capacitor system. An accurate switch-level fault simulation requires modeling also these effects. These fault modeling issues are addressed in the next section.

The validity of SWITCAP fault simulation has been shown in [14] by comparing switch-level fault simulation results obtained with SWITCAP and HSPICE, and by comparing HSPICE switch-level and transistor-level fault simulation results. This has been done for the case of a balanced filter similar to the one used in this work.

FAULT MODELING

A fault list including catastrophic faults in switches, catastrophic and parametric faults in capacitors, and stuck-at faults in logic components and comparators is provided to SWITTEST. Switch ON and OFF resistances and voltage source and operational amplifier output impedances (resistive) are also considered. Each resistor is modeled by means of a bilinear switched-capacitor resistor shown in Figure 2.

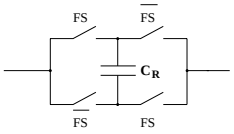


Figure 2: Bilinear switched-capacitor resistor.

These switched-capacitor resistors require a two-phase clock FS with a frequency f' significantly larger than the frequency of the fastest clock in the circuit [14]. The resistance implemented has a value given by

$$R \approx \frac{1}{4\ f'\ C_R} \tag{1}$$

and the fault models used are shown in Figure 3.

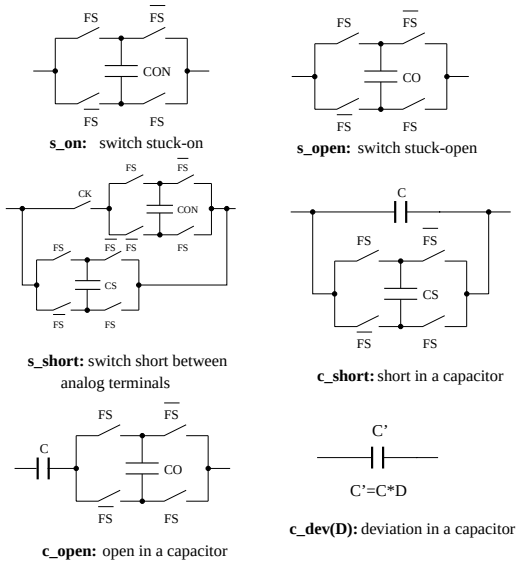
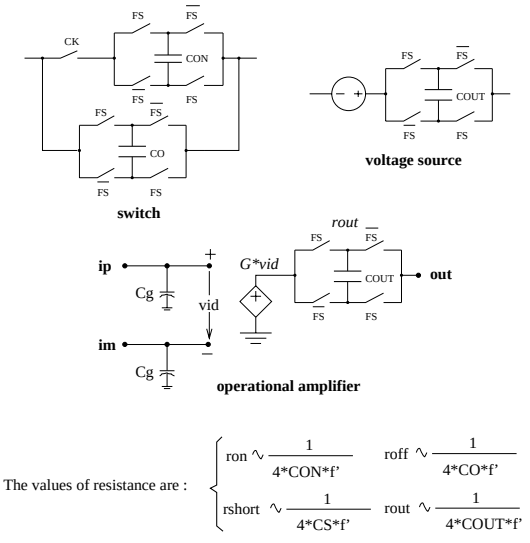


Figure 3: Fault models.

Catastrophic faults include switch stuck-on and switch stuck-open faults, shorts between the analog terminals of a switch and shorts and opens in capacitors. Short faults are represented as a resistive impedance between the shorted lines. Switch stuck-on faults are modeled by substituting the faulty switch by a resistor modeling the ON resistance of the switch, and switch stuck-open faults by substituting the faulty switch by a resistor modeling the OFF resistance of the switch. An open fault in a capacitor is modeled as a resistor in series with the capacitor. Parametric faults include deviations on circuit capacitors (*c_dev(D)*, where D indicates a relative deviation from the nominal value).

The list of faults considered correspond to an example set of faults which can be accurately simulated at switch-level. Obviously, no claim is made that these faults correspond to a realistic set of potential faults, just a set of faults which allow taking early decisions about the test of a design. A realistic fault set can only be extracted when a layout of the design has been produced and this is only towards the end of the design process.

To adequately model fault effects at switch-level, non-faulty components must also be modeled as shown in Figure 4. Switched-capacitor resistors are added to each switch in the design in order to model its ON and OFF resistance values. An output resistance is added at the output of each voltage source and operational amplifier to model a resistive output impedance. A parasitic capacitor Cg is considered at each operational amplifier input.



The values of resistance are :

$$ron \sim \frac{1}{4*CON*f'} \qquad roff \sim \frac{1}{4*CO*f'}$$

$$rshort \sim \frac{1}{4*CS*f'} \qquad rout \sim \frac{1}{4*COUT*f'}$$

Figure 4: Models for non-faulty components.

A CASE-STUDY

The fully differential bandpass filter of Figure 5 is considered in this section to illustrate the usefulness of switch-level fault coverage analysis for test optimization. The frequency f of the switched-capacitor clock is 1.088 MHz. The behaviour of the filter is shown in Figure 6 for an input of 1 V differential.

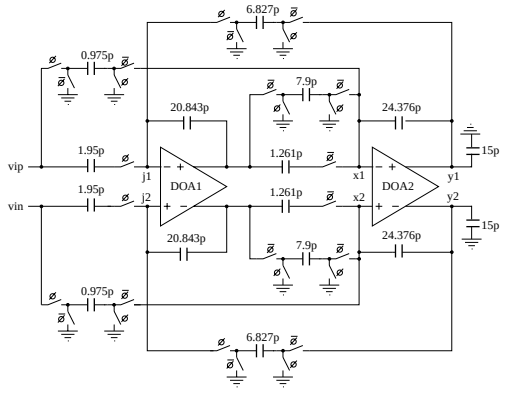


Figure 5: Bandpass filter schematics.

The fault list includes stuck-on, stuck-open and short faults in all switches in the design, and short and open faults in all capacitors. In addition, 200% and 50% deviations are considered in all capacitors. This results in a total of 140 faults. All switches are assumed to have the same ON and OFF resistances (1.8kΩ and 1GΩ, respectively). The output resistance of the input voltage sources is 1.8kΩ, and the output differential impedance of the amplifiers, which have a differential gain of 101db, is 20kΩ. The value of short resistance used is equal to the ON resistance of a switch (1.8kΩ). The resistance of an open fault is the same as the value of switch OFF resistance (1GΩ). The input amplifier capacitor Cg is 100fF. Frequency f' is 11 times larger than frequency f.

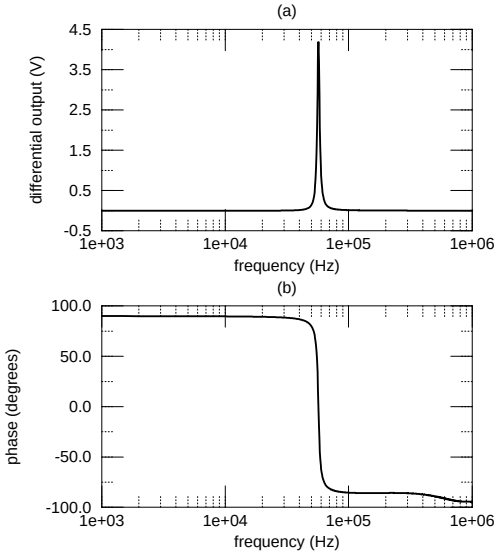


Figure 6: Bandpass filter behaviour: (a) gain (fo=56.915 kΩ) for an 1V differential input, and (b) phase.

Selection of test stimuli

For its evaluation, a test approach must be first characterized as a set of *test variables*. Circuit misbehavior is observed if a test variable exceeds a certain *test threshold*. Fault coverage is then obtained as a function of a test threshold. We consider an example input test signal of 0.4V differential. The test variable is defined as the largest deviation of the differential output of the faulty circuit with respect to the fault-free output, after 300μs to avoid the initial transient. A simulation time of 400μs is used. The printing step in the design specification is adjusted so that the test variable is only measured at the end of phase $\overline{\phi}$.

Figure 7 shows the fault coverage obtained for different signals which include a pulse at 57 kHz and sinusoidal signals at 55 kHz and 57 kHz. In addition, the fault coverage achieved with a frequency sweep (100 points in the frequency band 1kHz–100kHz) is also shown. Each fault simulation includes 140 faults and takes between 3 and 4 hours in an SPARC10 workstation.

Clearly, the larger the test threshold the lower the fault coverage achieved. A single tone with a frequency of 57 kHz (about the central frequency of the filter of 56.915 kHz) is sufficient to obtain the best fault coverage since the frequency sweep does not provide significantly better results. In addition, it is shown that a pulse at 57 kHz provides results as good or better than a sinusoidal signal at 57 kHz. This type of signal may be easier to generate on chip.

Unnecessary components

Fault coverage obviously increases with the magnitude of the input test signal. As shown in Figure 8(a), for an input of 1V differential (which produces an output around 4V differential which does not yet saturate the fault-free circuit), a fault coverage in the upper nineties

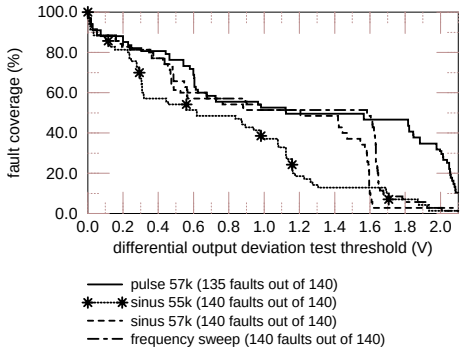
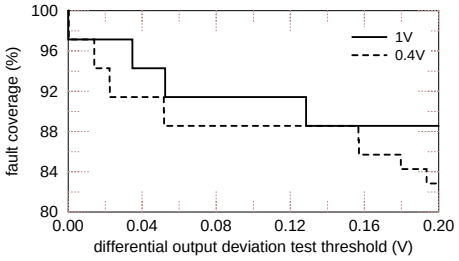


Figure 7: Fault coverage for an input test signal of 0.4V differential.

requires a test threshold below 40 mV, but 100% fault coverage is not possible. Besides, a 40 mV test threshold over a signal of 4V implies a maximum tolerated deviation of 1% in the signal output which may be too tight for some applications.



(a)

differential output deviation			
≈ 0 mV	≈ 35 mV	≈ 52 mV	≈ 128 mV
S1 s_on	S3 s_on	S5 s_on	S7 s_on
S1 s_short	S3 s_short	S5 s_short	S7 s_short
S2 s_on	S4 s_on	S6 s_on	S8 s_on
S2 s_short	S4 s_short	S6 s_short	S8 s_short

(b)

Figure 8: (a) fault coverage for 57 kHz sinusoidal signal of 0.4V and 1V differential, (b) output deviation for the faults which are most difficult to detect with an input of 1V.

As shown in Figure 8(b), the faults which are most difficult to detect correspond to stuck-on and short faults in some circuit switches. The actual switches are indicated in Figure 9. Stuck-on and short faults in switches S3, S4, S5 and S6 are hard to detect. However, these switches are not necessary in this design and they can be eliminated, with no impact in the filter behaviour, with the connection indicated in dashed lines.

Stuck-on and short faults in switches S1 and S2 are undetectable. These switches can be eliminated by simply substituting them by a wire without noticeable impact in filter behaviour. The same substitution can be done for switches S7 and S8 with little impact on circuit behaviour. The resulting behaviour of the circuit without switches S1-S8 is compared in Figure 10 with the behaviour of the original filter. The impact on circuit behaviour is minimum and the noticeable phase deviation only occurs when output signals have a negligible value.

Figure 11(a) shows the fault coverage for the original and modified filter for an input pulse signal of 0.4 V differential at 57 kHz. After elimination of unnecessary switches, the fault list contains a total of 116 faults. A test threshold of 200 mV can then be used to achieve 100% fault coverage for a nominal output signal of 1.6V differential.

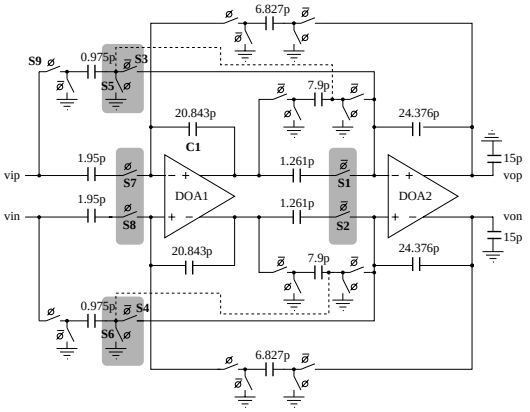


Figure 9: Unnecessary switches in the bandpass filter design.

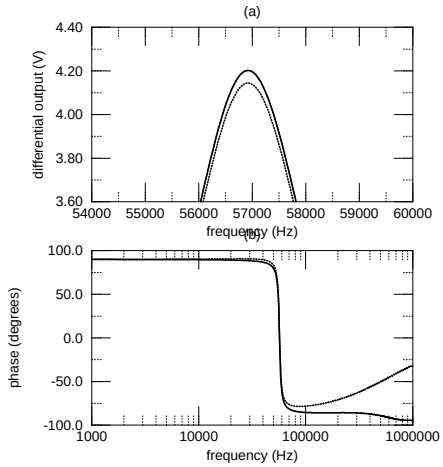


Figure 10: Modified filter versus original filter: (a) effect on the gain for an input of 1V differential, and (b) effect on the phase.

Comparison of test approaches

Several test nodes can be monitored for testing the circuit of Figure 9. By fault simulation, we have seen that exactly the same fault coverage is achieved by monitoring the differential output of the filter than by monitoring the differential output of the first stage. Both nodes have the same observability. The test approach presented in [18] for testing deviations in filter outputs can be used.

Another test approach is based on observing deviations of input common-mode in differential amplifiers. The nominal common-mode at each amplifier inputs is close to analog ground. Figure 11(b) shows the fault coverage achieved when the common-mode in the first stage, second stage and both stages are monitored. Clearly, both stages must be monitored at the same time but the common-mode test threshold must be smaller than 10 mV to reach a fault coverage of 100%. This test strategy, which is suitable for testing continuous-time filters [19], cannot provide sufficient fault coverage for testing all switch stuck-on and short faults.

Impact on fault coverage of design parameters

Figures 12(a) and 12(b) show the impact of variations on differential amplifier output impedance and output resistance of the input voltage sources, respectively. In both cases, fault coverage figures do not depend significantly on these parameters.

On the other hand, Figure 12(c) shows the impact of switch ON resistance. The lower the values of switch resistance the harder the test of switch catastrophic faults.

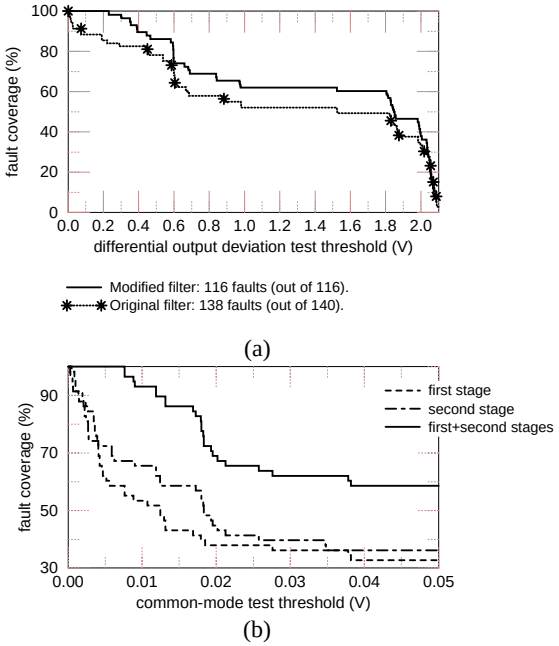


Figure 11: (a) fault coverage for original and modified filter with a pulse of 0.4V differential at 57kHz, and (b) fault coverage by observation of common-mode deviations for a sinusoidal input of 1V differential at 57 kHz.

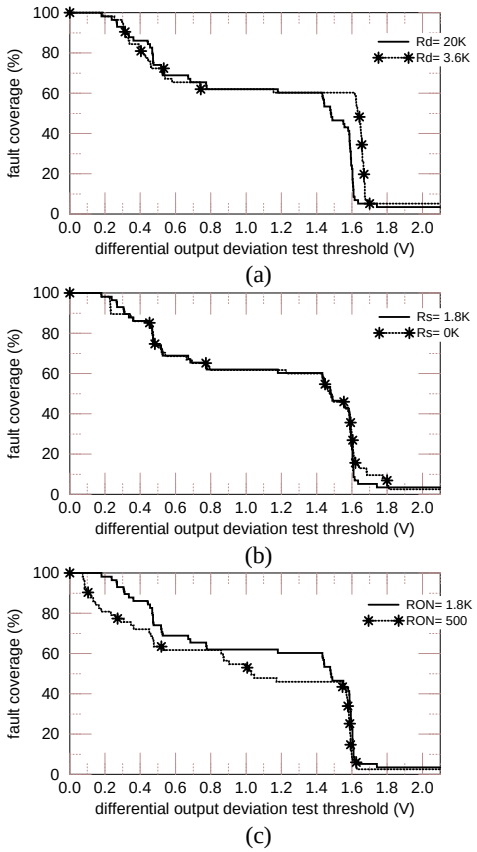


Figure 12: Impact on fault coverage, for a sinusoidal input of 0.4V differential at 57 kHz, of: (a) amplifier output differential resistance, (b) input voltage source output resistance, and (c) switch ON resistance.

CONCLUSIONS

In this paper, an approach to test optimization in switched-capacitor systems based on fault simulation at switch-level has been presented. The validity of the fault models presented has been shown in [14] by comparing fault simulation results at switch- and transistor-levels. The approach has been illustrated for the case of a bandpass differential filter and used for tasks such as selection of the most adequate test stimuli, determination of circuit parts with poor testability or with unnecessary components, selection of the most adequate test measures and test thresholds, comparison of alternative test approaches and, finally, quantification of the impact on fault coverage of design parameters.

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