Hierarchical top-down design of analog sensor interfaces: from system-level specifications down to silicon

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Abstract

The complete application of a hierarchical top-down design methodology to analog sensor interface front-ends is presented: from system-level specifications down to implementation in silicon, including high-level synthesis, analog block generation and layout generation.
A new approach for implementing accurate and fast power/area estimators for the different blocks in the architecture is described. These estimators provide the essential link between the high-level synthesis and the block generation in our hierarchical top-down methodology.
The methodology is illustrated by means of the design of a complex and realistic example. Measurement results are included.

1. Introduction

Advances in integrated circuit processing technologies offer designers the possibility of integrating systems onto a single application specific integrated circuit (ASIC). Although the productivity of the digital designer has been increased considerably, the productivity of the analog designer is still low due to the lack of mature analog CAD tools, particularly for high level design (levels higher than opamp level). At the lower level, more research results have been presented. For example, in [1] an analog module generator (AMGIE) has been introduced. Using a set of detailed design equations, this tool performs a global circuit optimization using simulated annealing. By using embedded transistor models, Hspice accuracy can be obtained in the evaluations of the circuit. The AMGIE system is able to size opamp-level blocks very accurately, within several minutes of CPU time. The system also includes automatic layout generation as was described in [2]. Other presented systems for the sizing of analog circuits are ASTRX/OBLX [3] and Fridge [4]. Both use a simulation based optimization approach.

In [1,5] a design methodology for analog high-level synthesis was introduced. The methodology is optimization based using behavioral models of different blocks in the architecture. The high-level synthesis is used to derive specifications for the different subblocks in the architecture, that can then be used as input to synthesize these blocks with the AMGIE system.

In this paper both the high-level and the low-level approaches are combined in a complete hierarchical, top-down design flow that is illustrated with the real design down to silicon of an analog sensor interface front end. The essential link between the two levels are accurate and fast power/area estimators. Without these estimators, which give an indication (estimate) of the implementation cost (power/area) of a particular set of subblock specifications, the optimization-based high-level synthesis tool could "overspecify" the different subblocks without penalty. In this paper also a new approach for implementing these power/area estimators is described.

As design example a radiation detector interface, which will be described in the next section, is chosen. Section 3 describes the high-level synthesis and the development of accurate and fast power/area estimators. Section 4 explains the sizing of the subblocks and the generation of the layout. Finally section 5 presents the measurements of the fabricated chip. The results are compared to an earlier manual design of the radiation detector interface.

2. Design example: radiation detector interface

Radiation detectors are used in nuclear physics experiments or for on-satellite radiation measurements. Fig. 1 shows a general architecture of a radiation detector interface [6]. Incident particles generate a charge pulse on a reverse biased detector diode, this charge is amplified and filtered in an analog preprocessing chain comprising a charge sensitive amplifier (CSA) and a pulse shaping amplifier (PSA). The charge packets from the detector are integrated on a capacitance in the CSA and then shaped to a semi-Gaussian pulse in the PSA. The PSA is a bandpass filter consisting of a differentiator and a number of *n* integrators. The height of the resulting pulse is proportional to the energy of the incident particle. The output of the analog preprocessing chain is fed into a Peak Detect and Hold

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(PDH) circuit, which functions as an analog memory. From this memory the signal is then fed to an analog to digital convertor (ADC). The digital output can then be processed further by the DSP core. The signal flow in the interface architecture is controlled by a finite state machine (FSM). In the next section we describe the high-level design of this front-end.

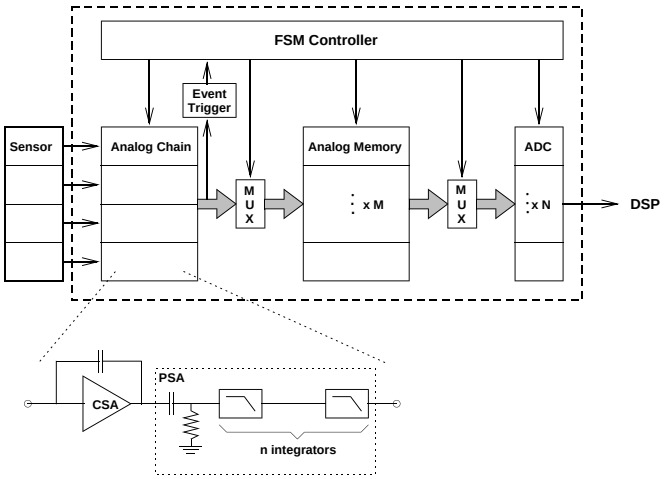

Figure 1: General radiation detector interface architecture

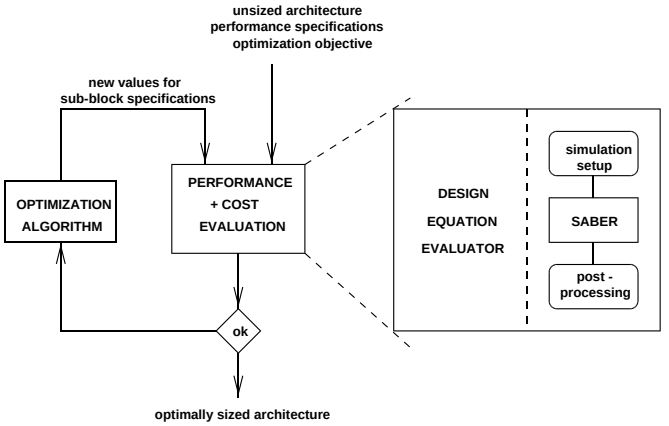

Figure 2: Simulated annealing-based optimization loop

3. Analog high-level synthesis: power and area estimators

A simulated annealing-based optimization loop is used for the high level synthesis [5], as shown in Fig. 2. At each iteration a set of subblock specifications is proposed, the corresponding system performance is simulated using behavioral models for the subblocks, and the estimated implementation cost is calculated (power/area). Using global optimization, the optimal specifications for the different subblocks are derived in this way such that all system specifications are met and the overall power and/or area is minimized.

In order to assess the optimality of different solutions, accurate power and area estimators have been developed for the different blocks in the radiation detector architecture, using a novel approach. A power (area) estimator is a function that returns the (estimated) power (area) needed to implement a block with certain specification values:

$$power = f(specs),\ area = h(specs) \quad (1)$$

The used approach uses a similar but simplified method as the AMGIE system. A set of simplified design equations for performances that are important with respect to power and area, combined with heuristics, are used to derive a first estimate of power and area. This estimate is then used in a local circuit optimization, using more accurate expressions for the different performances of the subblocks, to determine the optimal power/area needed to meet the given specs. Instead of using embedded transistor models like was done in the AMGIE, only simple transistor models are used to speed up the power/area estimator calculations. This approach will now be illustrated for one subblock, the CSA, the architecture of which is shown in Fig. 3. The approach is similar for the other subblocks.

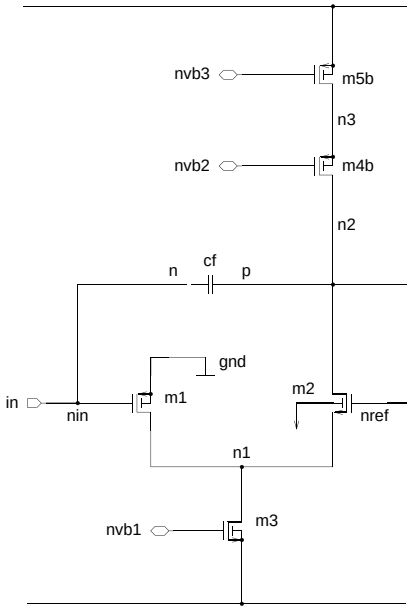

Figure 3: Schematic Charge sensitive amplifier

The most important specifications for the CSA subblock are the total equivalent noise (ENC_{total}) and the speed (rise time t_r). In a good design the major contribution for the noise comes from the input transistor, the other transistors are sized such that their contribution is negligible. In this case, the white noise is given by [6]:

$$ENC_W^2 = K_{SW}\ C_{SW}(n) T_{CSA}\ (C_{in,\,total} + C_f)^2 \frac{1}{gm_{in}} \frac{1}{\tau_P} \quad (2)$$

where $K_{SW} = \frac{2k}{3\pi\ q^2}$ and $C_{SW} = \frac{n!^2\, e^{2n}}{n^{2n-1}} \beta\left(\frac{3}{2}, n - \frac{1}{2}\right)$

β: beta-function

C_f: feedback capacitance (see Fig. 3)

τ_p: peaking time (time to reach peak value of generated pulse)

n: number of PSA integrator sections

The pink noise is given by [6]:

$$ENC_F^2 = \left(\frac{KF}{WL}\right)_{in} \frac{1}{C_{ox}^2} \frac{(C_{in,\,total} + C_f)^2}{q^2 2n} \left(\frac{n!^2\, e^{2n}}{n^{2n}}\right) \quad (3)$$

It can be calculated that for minimal white noise the capacitance of the input transistor should be chosen such that $C_{m,\,in} = \frac{C_{\det} + C_f}{3}$, while for an optimal pink noise contribution, the noise condition $C_{m,\,in} = C_{\det} + C_f$ should be met (where C_{det} is the detector capacitance). This implies that, as far as pink noise is concerned, either W or L can be chosen freely to meet the optimal noise condition. However, taking into account the requirements for the *GBW* and the speed of the CSA, a minimal gate length should be chosen for the input transistor. This insight allows to size the input transistor and to calculate the power drain (by choosing a V_{gs}-V_t of 200mV for the amplifying input transistor). The sizes and current drain for the other transistors can be estimated using the full expression for the noise and some additional equations for the parasitic poles, from which the phase margin and speed performance can be calculated. This set of equations is resolved using a local constraint-driven algorithm from the Matlab optimization toolbox.

The result of this approach is depicted in Fig. 4 and 5. Power and area are plotted as a function of the dominant specifications: total equivalent noise and speed (i.e. rise time) of the CSA. The smaller the admissible noise, the larger the area (see equation (3)). Larger transistors means higher capacitances on the internal nodes, resulting in higher *gm* and thus also higher power to achieve the speed requirements. The power also increases with increasing speed requirements, and the larger widths of the transistors required for higher speed result in an increase in area as can clearly be seen. Given a set of specifications, estimated power/area can be calculated within 1.15 sec on an HP712/100 workstation, which is important if the estimator is to be used in every iteration of the high-level synthesis. For the specifications as listed in table 1 in the experimental results later on, the estimated power consumption of the CSA was 3 mW, which is in the same order of the 2 mW predicted by Hspice.

Similar power/area estimators have been derived for the other blocks in the architecture. These power/area estimators are used during high-level synthesis. As can be seen in Fig. 4 and 5, they model the trade-offs between the most important specs of the different blocks. They also give an estimate for the total power/area of the global implementation of the architecture.

Fig. 6 shows a plot of the system-level trade-offs of the complete radiation detector front-end architecture, which was derived with the high-level synthesis tool and with the power/area estimators of the blocks. High dynamic range (DR) and high speed result in larger power drain.

As an example, table 1 gives the optimal specifications of the CSA-PSA as computed by the high-level synthesis tool starting from system level specifications of a counting rate of 200 kHz and an accuracy of 8 bit.

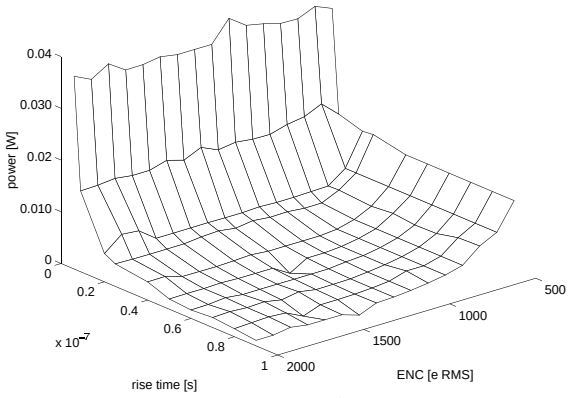

Figure 4: Power estimator for the CSA subblock

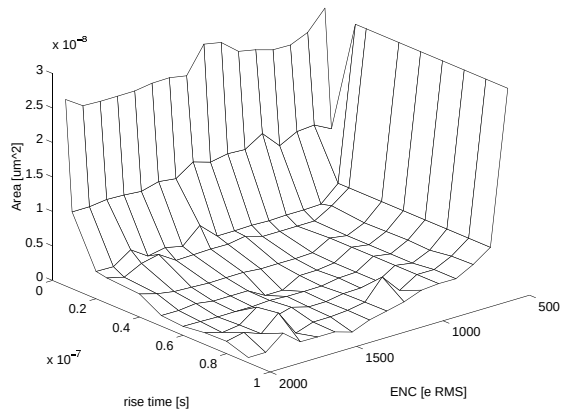

Figure 5: Area estimator for the CSA subblock

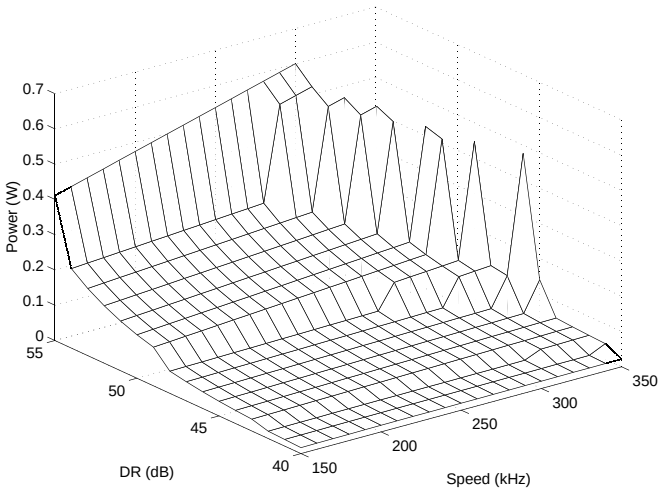

Figure 6: System-level trade-offs between power, speed and accuracy.

Next, the different subblocks have been (automatically) designed by means of the AMGIE system for the block specifications from Table 1, as derived by the high-level synthesis tool.

	Spec.	unit	Manual	Synthesis
Detector capacitance	80	pF	80	80
Peaking Time	1.5	µs	1.1	1.1
Counting rate	200	kHz	200	**294**
Noise	< 1000	e^- EMS	1000	905
Gain	20	mV/fC	20	21
Output Voltage range	2	V	2	2
Power consumption	< 40	mW	40	**7**

Table 1: Performance achieved after simulation: an earlier manual design and the results after synthesis are compared.

4. Sizing and layout generation of the particle detector front-end blocks

Starting from the specification list as given in table 1, the particle detector front-end can be sized using the AMGIE system [1]. This tool is able to design analog functional blocks, such as an operational amplifier or a particle detector front-end, either in an automated or interactive session. The tool converts a unordered set of design equations in an ordered computational path, which is then used in a global optimization loop, to size the circuit. Embedded transistor models result in Hspice accuracy during optimization.

The CSA was implemented using the folded cascode structure as depicted in figure 3. The major constraints are total equivalent noise and speed (i.e. rise time). The noise can be reduced to three equivalent noise sources: (1) the equivalent serial white noise, generated by the thermal channel noise of the transistors, (2) the equivalent pink noise generated by the transistors, and (3) the parallel white input current noise, generated by the detector leakage current (shot noise) and the thermal noise from the biasing circuit of the detector. The different equivalent noise sources are given by [6]:

$$ENC_{PW}^2 = K_{PW} C_{PW}(n)\,\tau_p I_{leak} \qquad (4)$$

$$\text{with} \quad K_{PW} = \frac{1}{2\pi q} \quad \& \quad C_{PW} = \frac{n!^2 e^{2n}}{n^{2n+1}} \beta\left(\frac{1}{2}, n+\frac{1}{2}\right)$$

$$ENC_{SW}^2 = K_{SW} C_{SW}(n) T_{CSA} (C_{\text{int}} + C_f)^2 \frac{1}{\tau_p} \frac{1}{gm_{eq}} \qquad (5)$$

$$\text{with} \quad K_{SW} = \frac{2k}{3\pi q^2} \quad \& \quad C_{SW}(n) = \frac{n!^2 e^{2n}}{n^{2n-1}} \beta\left(\frac{3}{2}, n-\frac{1}{2}\right)$$

$$\text{and} \quad \frac{1}{gm_{eq}} = \frac{gm_{m1} + gm_{m3} + gm_{m5b}}{gm_{m1}^2}$$

$$ENC_{SF}^2 = K_{SF} C_{SF}(n)(C_{\text{int}} + C_f)^2 \left(\frac{KF}{WL}\right)_{eq} \qquad (6)$$

$$\text{with} \quad K_{SF} = \frac{1}{2q^2 C_{ox}^2} \quad \& \quad C_{SF}(n) = \frac{n!^2 e^{2n}}{n^{2n+1}}$$

$$\left(\frac{KF}{WL}\right)_{eq} = \frac{1}{gm_{m1}^2}\left[\left(\frac{KF}{WL}\right)_{m1} gm_{m1}^2 + \left(\frac{KF}{WL}\right)_{m3} gm_{m3}^2 + \left(\frac{KF}{WL}\right)_{m5b} gm_{m5b}^2\right]$$

A second set of equations describing the frequency behavior (parasitic poles on the different nodes, GBW, PM, …) was added. A third set of equations describes the large signal behavior (slewing, settling time, …).

For the second building block, the PSA, a Miller opamp was used. Similar to the CSA, equations were derived, describing the frequency behavior and the large-signal behavior.

To these equations, a set of constraints were added to force the global optimization to find a solution that meets the specifications derived by the high-level synthesis tool. The sizing takes about 20 minutes on an HP712/100 workstation. The results after simulation are given in last column of table 1. None of the specifications were violated. The sizing resulted in a circuit which used 4 times less power compared to a previous manual design, allowing faster counting rates, while still achieving the noise specifications.

After the sizing, the layout of the CSA-PSA was generated using the performance-driven analog layout synthesis tool LAYLA [2], which is also incorporated in the AMGIE sytem. This tool uses global optimization to bound the layout-induced performance degradation within the allowed margins, which guarantees that the resulting layout will meet the specifications by construction.

After the layout was generated, parasitics were extracted and the final performance was verified using Monte-Carlo simulation.

5. Measurements

A microphotograph of the fabricated chip is shown in Fig. 7. The CSA-PSA was processed in a standard CMOS 0.7 µm process. The different measurements are gathered in table 2 and compared to the required specifications. All results are comparable to what had been predicted in the sizing (see table 1). With a power consumption of 10 mW, the chip performs four times better than the manual design, which consumes 40 mW, still obtaining the speed and noise requirements. Fig. 8 depicts the time response as measured

from the processed CSA-PSA. As can be seen on this measurement, the chip is within specification with a peaking time of 1.20 μs.

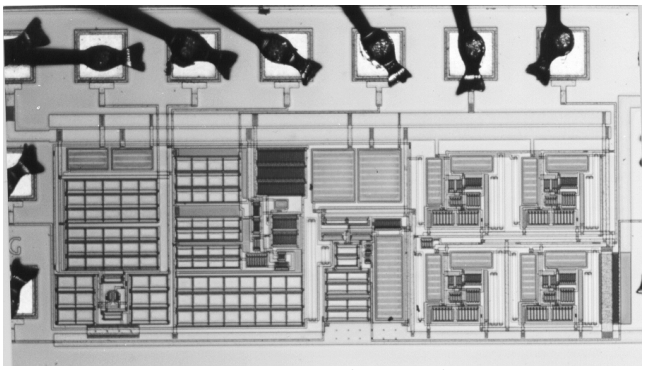

Figure 7: Microphotograph of the manufactured CSA-PSA

	Specification	unit	Measurements
Detector capacitance	80	pF	80
Peaking Time	1.5	μs	1.18
Noise	< 1000	e^- EMS	1100
Gain	20	mV/fC	18
Output Voltage range	2	V	2
Power consumption	< 40	mW	10

Table 2: Measurements of the CSA-PSA: all performances are comparable to what was predicted in the sizing (see table 1).

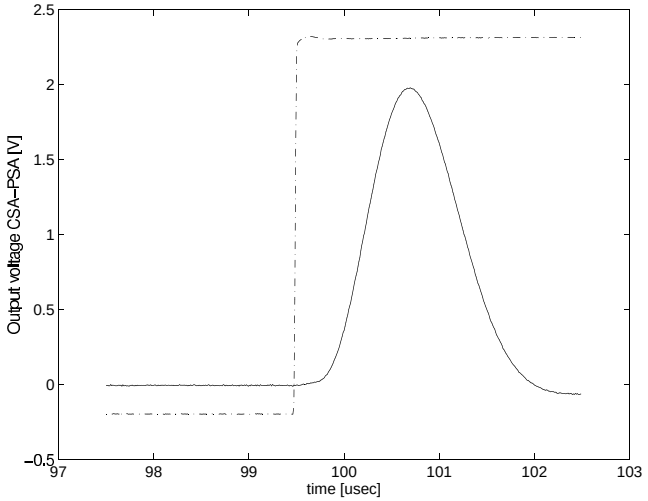

Figure 8: Measured time response of the CSA-PSA to an incident particle

6. Conclusion

A hierarchical top-down design methodology applied to analog sensor interface front ends was presented: from system-level specifications down to implementation in silicon, including high-level synthesis, analog block synthesis and layout generation.

Accurate and fast power/area estimators have been developed that link the high-level synthesis and the block synthesis.

The methodology was illustrated by means of a complex and realistic design example. Measurement results confirm the derived specifications in the high-level synthesis: the chip consumes four times less power than an earlier manual design, still achieving the noise and speed requirements.

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References

[1] G.Gielen et.al., “An analog module generator for mixed analog/digital ASIC design”, *International Journal of circuit Theory and Applications*, pp. 269-283, July-August 1995.

[2] K. Lampaert, G. Gielen and W. Sansen, “A Performance-Driven Placement Tool for Analog Integrated Circuits”, Journal of Solid-State Circuits, pp. 773-781, July 1995.

[3] E. Ochotta, R. Rutenbar and L. Carley, "Analog Circuit Synthesis for Large, Realistic Cells: Designing a Pipelined A/D Converter with ASTRX/OBLX," Proc. IEEE Custom Integrated Circuits Conference, May 1994, pp. 15.4.1-3.

[4] F. Medeiro-Hidalgo, R. Dominguez-Castro, A. Rodriguez-Vazquez and J.L. Huertas, "A Prototype Tool for Optimum Analog Sizing Using Simulated Annealing," ISCAS, pp.1933-1936, 1992.

[5] S. Donnay, G. Gielen, W. Sansen, “High-level synthesis of analog sensor interface front-end,” Proc. ED&TC, 1997, pp. 56-60.

[6] Z. Chang, W. Sansen, “Low-noise wide-band amplifiers in bipolar and CMOS technologies”, Kluwer Academic Publishers, 1991.