Temperature Effect on Delay for Low Voltage Applications

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Abstract

This paper presents one of the first analysis of the temperature dependence of CMOS integrated circuit delay at low voltage. Based on a low voltage extended Sakurai's α-power current law, a detail analysis of the temperature and voltage sensitivity of CMOS structure delay is given. Coupling effects between temperature and voltage are clearly demonstrated. Specific derating factors are defined for the low voltage range (1-3V_{T0}). Experimental validations are obtained on specific ring oscillators integrated on a 0.7μm process by comparing the temperature and voltage evolution of the measured oscillation period to the calculated ones. A low temperature sensitivity operating region has been clearly identified and appears in excellent agreement with the expected calculated values.

1: Introduction

To satisfy low power dissipation constraints imposed by the exploding market of portable applications, designers explore all the useful ways in reducing energy dissipation in today technology circuits. Among the techniques generally used such as the reduction of switched capacitances, designing for low voltage appears as the most efficient way to trade speed and power. For that the V_{DD} supply and the V_{T0} threshold voltages are mutually sized to respect a conservative value of the order of 5 for the ratio V_{DD}/V_{T0} [1]. However with submicronic processes the carrier operation in speed saturation limits the speed performance degradation, allowing V_{DD}/V_{T0} ratio values ranging between 2 and 3.
Moreover for special circuits used in medical or domestic applications, which impose very low power constraints, the use of supply voltage values not too different from V_{T0} is of current practice [2]. Here too the lower limit in reducing threshold values is defined from leakage power dissipation considerations [3]. So designing with very low supply voltage values (below $3V_{T0}$) is becoming more and more attractive.

If the great sensitivity of design performances to V_{DD} and V_{T0} value fluctuations has been identified as one of the major limitations [4,5] of V_{DD} scaling, few attention has been given to characterize their temperature sensitivity in the low voltage domain. If some results on simulations [12] and measurements [6] of speed and power performances of standard cell library and circuits operating at low V_{DD}, have been recently available, no modeling of these parameters and of their sensitivity has been proposed.

In this paper we analyze the combined effects of voltage reduction and temperature variation on speed performances. Based on an extended α-power current representation [7], calibrated for low voltage, we propose a simple model allowing the accurate investigation of the speed performance temperature sensitivity of low voltage designs. This temperature sensitivity is experimentally investigated in the second part. The third part is devoted to the presentation of the extended current model. Application to the speed performance modeling is given in the fourth part. In part five we present validations on specific test structures implemented in a 0.7 μm process. Finally a conclusion is drawn in the last part.

2: Evidence of the temperature effect on speed performance

The complete characterization of CMOS standard cell libraries implies an accurate modeling of the effect of the supply voltage and temperature variations Usually library suppliers represent the cell performance variations to supply voltage and temperature through independent derating factors (Der(V_{DD}), Der(θ)) which allow quick cell performance characterization for any deviation from

well characterized nominal operating conditions. This can be described from :

$$\text{Delay} = \text{Delay(nominal)}.\ \text{Der}(V_{DD}).\ \text{Der}(\theta) \qquad [1]$$

where Delay(nominal) = A+B.C_{load}, A and B coefficients being considered as delay calibration parameters, defined for nominal values of the supply voltage and the temperature. For usual supply voltage standard (V_{DD} value greater than 3 V_{T0}) this model results in a quite good accurate representation of the variations of the circuit operating conditions. In this voltage range this is due to an apparent independence of the temperature sensitivity to the supply voltage. This can be understood easily, considering that in speed saturation operating mode, the current variation is more dominated by the mobility variation than by the threshold voltage one. The relative variation of the measured oscillation period between 298°K and 398°K, for V_{DD} values ranging from 2.5v to 5v, is given in fig.1, considering specific ring oscillators implemented in a 0.7µm process. As shown the temperature sensitivity of the oscillation period appears quite independent of the supply voltage.
The low voltage evolution of the oscillation period in the same temperature range is given in fig. 2. This time the temperature sensitivity of the oscillation period is strongly V_{DD} dependent and exhibits an interesting reversal dependency. As discussed in [6] this evolution is the result, at low V_{DD}, of the increased current sensitivity to the threshold voltage. Both threshold voltage and carrier mobility decrease with increasing temperature. Lower threshold voltage increases the transistor current and lower mobility decreases its value. This results in an opposite variation of the current compensating and then dominating (when V_{DD} approaches V_{T0}) the mobility induced variations. These observations give a clear evidence of the coupled influence at low voltage of the temperature and V_{DD} variations on the current and speed performances of CMOS circuits. As a result, the equation 1 with independent derating factors is no more sufficient to describe these variations with reasonable accuracy. Because speed performances depend on the current available in the different structures we first introduce the current model we used to represent temperature effects at low voltage.

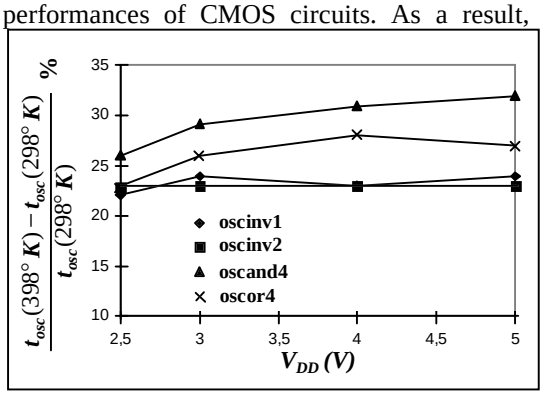

Figure 2: Illustration of the oscillation period temperature sensitivity in the 2.5-5v range.

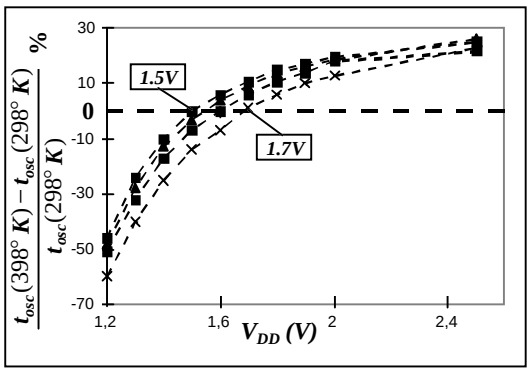

Figure 3: Illustration of the oscillation period temperature sensitivity in the 1.2-2.5v range.

3: Current modeling

3.1: Submicronic modeling

Short channel effects increase considerably the complexity of models for submicronic processes. A very good synthesis together with a nice modeling has been presented in [8] where the current expression in strong inversion is given in terms of design and operating condition parameters such as:

$$I_D = \frac{\mu_0}{R} C_{ox} \frac{W}{L}\left[V_{GS} - V_{TO} - \frac{1+\delta}{2} V_{DS}\right] V_{DS} \qquad [2]$$

where R includes the mobility degradation effects as given in [8] and the other parameters have the usual signification. Temperature sensitivity can be included easily considering mobility and threshold voltage variation such as [9,10]:

$$\mu_0(\theta) = \mu_0(\theta_{nom}) \cdot \left(\frac{\theta_{nom}}{\theta}\right)^{\theta_\mu}$$
$$V_{T0}(\theta) = V_{T0}(\theta_{nom}) - \delta \cdot (\theta - \theta_{nom}) \qquad [3]$$

where θ_μ, δ represent pseudo empirical coefficients which account for the lattice and impurity scattering effects and the temperature evolution of the intrinsic carrier concentration respectively. They are calibrated on the different processes and have values ranging between 1 - 2 and 10^{-3}- 4.10^{-3} V/^{oc} for θ_μ and δ respectively.
If the accuracy of this model is satisfactory for analog applications it is still too complicated for the analytical modeling of performances of digital circuits. The simplified α-power model introduced by Sakurai [7] may present a sufficient accuracy if calibrated in a supply voltage range reduced to low

voltage (1 to 3V_{T0}) and standard voltage (3 to 5V_{T0}) domains.

3.2: Extended α-power model

The simplified model we propose, extends the Sakurai's α-power law including the temperature effects in the mobility (limit speed) and the threshold voltage. As given in [7] MOS transistor current evolution in submicron process can be well represented from:

$$I_{DS} = K \cdot W \cdot (V_{DD} - V_{T0})^{\alpha} \qquad [4]$$

where α and K are parameters calibrated on experimental current variations.

α represents the velocity saturation index and has a value ranging from 2 (long channel) to 1 for deep saturation. K represents the process drivability factor, for α = 1 (standard voltage range for a 0.7µm process) it can be easily shown to be: $K = C_{ox}.v_s$ where $v_s = \mu_o.E_c$ is the carrier limit speed directly connected to the low field mobility [13]. For the low voltage range previously defined these parameters will be calibrated on the $I_{DS}(V_{GS})$ curve for V_{GS} values ranging between 1-3 V_{T0}.

Considering now that the temperature sensitivity of the current is completely defined through the threshold voltage and the mobility evolution we obtain:

$$K(\theta) = K(\theta_{nom}) \cdot \left(\frac{\theta_{nom}}{\theta}\right)^{\theta_k} \qquad [5]$$

$$V_{T0}(\theta) = V_{T0}(\theta_{nom}) - \delta \cdot (\theta - \theta_{nom})$$

Using this model allows simplified analysis of the current sensitivity to both the temperature and the supply voltage. Eq. 4-5 give direct information on the temperature evolution observed in fig. 1 and 2. Increasing the temperature decreases V_{T0} and K parameter through the mobility resulting in opposite effects on the current. In the standard voltage range the threshold voltage evolution has a little effect on the current compared to that of the mobility which dominates the evolution. In the low voltage range, lower the supply voltage is larger the V_{T0} effect on the current is. This explains completely the variations observed in fig. 2 and the dependence between temperature and supply voltage derating coefficients. For very low supply voltage values the V_{T0} effect dominates, reversing the temperature dependence. Hence a specific supply voltage value can be found at which the temperature effects compensate. This value can be obtained easily from eq.4 and 5 canceling the derivative of the current equation with respect to the temperature such as :

$$V_{DD} = V_{T0}(\theta_{nom}) + \frac{\alpha \cdot \delta}{\theta_k} \cdot \theta_{nom} \qquad [6]$$

As we will show later the definition of this temperature insensitive cross point voltage is of great importance for the speed of the structures which will exhibit the same temperature evolution. As an example let us consider a submicronic process with the following values of the parameters: α = 1.5, $\delta = 2.10^{-3}$, θ_k= 1 with θ_{nom} = 298^{oK}, the value of V_{GS} (V_{DD}) for which the current temperature coefficient cancels is V_{T0} + 0.89 v which is nearly 2 V_{T0}.

3.3: Experimental validations

A first bench of validations has been obtained from HSPICE simulated values of the N and P transistor currents for a 0.7µm process using the ATMEL-ES2 foundry supplied model card (level 6). This level is sufficiently accurate to reproduce correctly the current evolution in a large voltage range including subthreshold domain for analog applications. α, δ, θ_k, V_{T0} and K parameters have been calibrated in the low voltage domain (1 to 3 V_{T0}), their corresponding values are given in Table 1.

	V_{TO} (V)	K (µA/µmV)	α	δ (mV/°C)	θ_k
NMOS	0.7	80.2	1.49	2 10^{-3}	1.57
PMOS	1.05	30.3	1.74	1.5 10^{-3}	1

Table 1: characteristic parameters of the 0.7µm process.

In figure 4 we compare the simulated current values (HSPICE level 6) to the calculated ones (NMOS), for different temperature conditions ranging from 298^{oK} to 398^{oK}. As observed the agreement between simulated and calculated values with the proposed model is excellent in the full voltage range, the maximum discrepancy is lower than 5%.

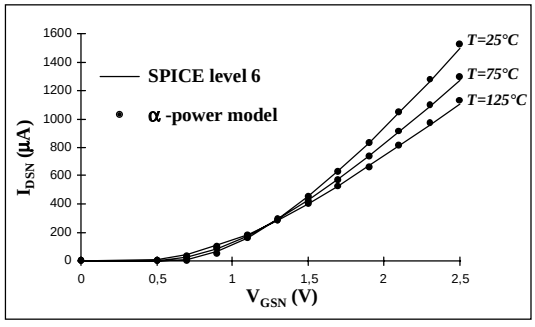

Figure 4: Comparison between the calculated (α-power model) and simulated (HSPICE foundry level 6) current values for the NMOS transistor.

As observed in the figure the crossing point voltage value is obtained at: $V_{GSNCROSS}$ = 1.3v which is not too different from 2 V_{T0} as we calculated directly in the preceding part.

4: Application to delay performance modeling

We consider a simple cell such as an inverter and then extend the results to more complex cells. Delay modeling [14] can be develop into two steps: the study of the step response which constitutes the intrinsic response of the considered element and the extension to the real response to account for environmental phenomena such as input slope effects. Let us first consider the step response of a simple inverter.

4.1: Temperature effect in the step response

Defining the delay at half supply voltage, the step response is associated to the charge/discharge time of the cell output load under the maximum available current [14] resulting in:

$$t_{HLs,LHs} = \frac{C_{ox} \cdot L \cdot V_{DD}}{K_{N,P}(\theta) \cdot (V_{DD} - V_{T0N,P}(\theta))^{\alpha_{N,P}}} \cdot \frac{C_L}{2C_N} \qquad [7]$$

where L is the effective length of the switching transistor, C_L the total output load of the cell, $C_{N,P}$ represent the driving input capacitance of the N,P transistor, respectively, the other parameters being defined in the preceding part.

As shown in this equation the temperature effect is easily entered through the K and V_{T0} temperature dependence previously discussed. The sensitivity analysis of this response can be studied directly from the partial derivatives of this equation with respect to these two key parameters, resulting in eq. 8, where we defined by $S(V_{DD})_\theta$, and $S(\theta)_{VDD}$ the step response sensitivity parameters with respect to the supply voltage (at constant temperature) and the temperature (at constant supply voltage) respectively.

In figures 5 and 6 we represent the variation of the calculated sensitivities for the considered domain of temperature and low supply voltage.

As expected the sensitivity to the voltage (fig.5) increases when approaching the threshold value, this trend is weaker at high temperature due to the decrease of V_{T0}.The sensitivity to the temperature (fig. 6) is nearly temperature independent but exhibits a strong voltage dependence with a sign reversal for low voltage and a temperature insensitive cross point voltage value around $2V_{T0}$ (1.3v on the figure). These variations reflect the trends observed in the simulated current (fig. 4) and almost the experimental evolution of the measured oscillation periods of integrated ring oscillators (fig. 3).

4.2: Application to the definition of derating coefficients

These results give evidence of the impossibility to represent the temperature and voltage dependency of the delay through independent derating factors as usually defined to characterize industrial libraries. Considering the results obtained for the sensitivity of the step response it appears necessary to define a common temperature and voltage dependent derating factor. This derating coefficient (eq. 9) can be obtained directly from eq. 7 where the parameters α, δ and θ_k which represent the saturation index and the temperature coefficient of the threshold voltage and the mobility, respectively, are calibrated on the process.

4.3: Extension to the real delay

As shown in [7,11,14] real delay in CMOS structures must account for the input controlling slope effect. For a reasonable range of loading and controlling conditions the real response of a stage can be evaluated from a linear combination of step responses of the controlling and switching stages [14] such as:

$$t_{HL,LH}(i) = \left(1 - 2\frac{1 - V_{T0N,P}(\theta)/V_{DD}}{1 + \alpha_{N,P}}\right) t_{LHs,HLs}(i-1) + t_{HLs,LHs}(i)$$

$$= A_{N,P}\, t_{LHs,HLs}(i-1) + t_{HLs,LHs}(i)\,. \qquad [10]$$

As shown the $A_{N,P}$ coefficients are temperature and voltage dependent but these dependencies are not correlated, their temperature sensitivity are nearly voltage independent.

$$\frac{\Delta t_{HLs,LHs}}{t_{HLs,LHs}} = S_{N,P}(V_{DD})_\theta \cdot \frac{\Delta V_{DD}}{V_{DD}} = \left(1 - \frac{\alpha_{N,P}}{1 - \dfrac{V_{T0N,P}(\theta_{nom}) - \delta(\theta - \theta_{nom})}{V_{DD}}}\right) \cdot \frac{\Delta V_{DD}}{V_{DD}} \qquad [8]$$

$$\frac{\Delta t_{HLs,LHs}}{t_{HLs,LHs}} = S_{N,P}(\theta)_{VDD} \cdot \frac{\Delta \theta}{\theta} = \left(\theta_{kN,P} - \frac{\alpha_{N,P}\delta_{N,P}}{V_{DD} - V_{T0N,P}(\theta_{nom}) + \delta_{N,P}(\theta - \theta_{nom})} \cdot \theta\right) \cdot \frac{\Delta \theta}{\theta}$$

$$\frac{t_{HLs,LHs}(V_{DD},\theta)}{t_{HLs,LHsnom}} = Der_{HLs,LHs}(V_{DD},\theta) = \left(\frac{V_{DD}}{V_{DDnom}}\right)^{1-\alpha} \left[\frac{1 - V_{T0N,P}(\theta_{nom})/V_{DDnom}}{1 - V_{T0N,P}(\theta_{nom})/V_{DD} + \delta_{N,P}\Delta\theta/V_{DD}}\right]^{\alpha_{N,P}} \left(\frac{\theta}{\theta_{nom}}\right)^{\theta_{kN,P}} \qquad [9]$$

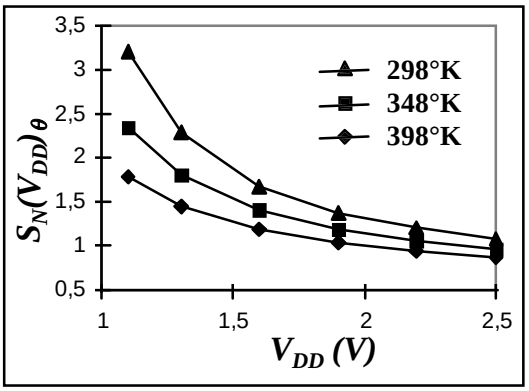

Figure 5: Delay sensitivity to the voltage in the low voltage range for different temperatures.

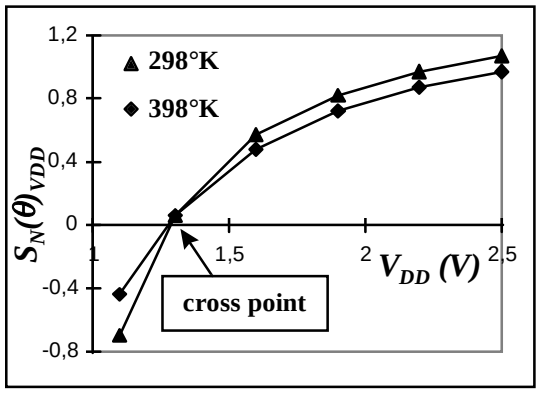

Figure 6: Delay sensitivity to the temperature in the low voltage range for different voltages.

Using the derating coefficients previously defined (eq.9) the inclusion of temperature and voltage effects in the real response (eq.10) is straightforward, we obtain:

$$\frac{t_{HL,LH}(V_{DD},T)}{t_{HL,LHnom}} = (1-R)\frac{A_{N,P}}{A_{N,Pnom}} Der_{LHs,HLs} + RDer_{HLs,LHs} \quad [11]$$

where $R = \frac{t_{HLS;LHSnom}}{t_{HL,LHnom}}$ is the ratio between the structure step and real responses for nominal operating conditions.

It can easily be verified that the value of this coefficient belongs to the 0 - 1 interval, the value 1 corresponding to a pure step response and 0 to a theoretical infinite contribution of the input ramp. From this equation it is possible to extract a simple evolution criterion for the real response: the derating factor belongs always to the interval $\frac{A_N}{A_{Nnom}} Der_{LHS}$, Der_{HLS} for the output falling edge and $\frac{A_P}{A_{Pnom}} Der_{HLS}$, Der_{LHS} for the rising one.

Considering now the delay performance of a full circuit as a sum of real rise and fall delay times it appears then possible to determine a derating factor for the circuit delay performance, around the nominal operating conditions. The total delay derating factor value of the complete circuit will always belong to the interval defined by :

$$\mathrm{DER}_{\min} = \min\left(\frac{A_N}{A_{Nnom}} Der_{LHS}, Der_{LHS}, \frac{A_P}{A_{Pnom}} Der_{HLS}, Der_{HLS}\right)$$

and

$$\mathrm{DER}_{\max} = \max\left(\frac{A_N}{A_{Nnom}} Der_{LHS}, Der_{LHS}, \frac{A_P}{A_{Pnom}} Der_{HLS}, Der_{HLS}\right)$$

As a result, the complete circuit delay performance will obey the law:

$$\boldsymbol{t_{total}(V_{DD},T)} = \left[(1-\boldsymbol{b})\boldsymbol{DER}\min + \boldsymbol{bDER}\max\right]\boldsymbol{t_{tota}}_{\ln}\boldsymbol{om} \quad [12]$$

where the b coefficient (values ranging between 0-1) characterizes the quality of the design in terms of performance dominated by N or P transistors as it can be found in specific circuits such as SRAM (N dominated) [6].

These equations allow not only an accurate determination at the cell level of the evolution of the delay performance but give also a good indication of the evolution interval of a complete circuit implemented in the considered process.

5: Experimental validations

Validation of these results has been obtained on a set of 4 ring oscillators constituted of arrays of 109 inverter stages with different configuration ratios (W_P/W_N = 1 for oscinv1, W_P/W_N = 3 for oscinv2), arrays of 54, 4 input AND, OR (oscand4, oscor4). We select these different configurations in order to exhaust the expected N or P dominated sensitivity. In fig.7 the derating factors measured on the 4 ring oscillators at 298°K has been plotted for V_{DD} values ranging from 2.5 to 1.2v. Has expected, each ring oscillator has it's low voltage behavior included in the calculated min-max interval.

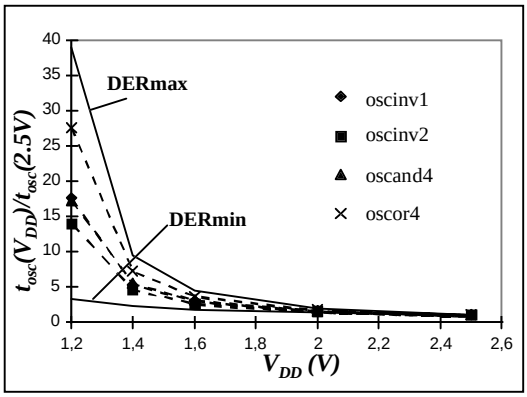

Figure 7: voltage evolution of the measured oscillation periods in the low voltage range.

The comparison between the calculated and the measured derating factor on oscinv2 in the same range of V_{DD} values, at 298°K and 398°K is given in fig.8. As we can observe on this plot the agreement is very good and confirms the validity of the proposed approach in modeling the supply voltage and temperature effects on performances in the low voltage range.

To conclude on these results we represent in fig.9 the evolution of both V_{DD} derating (298°K) and θ sensitivity in the two V_{DD} domains we considered, using the values obtained on oscinv2 as a reference:

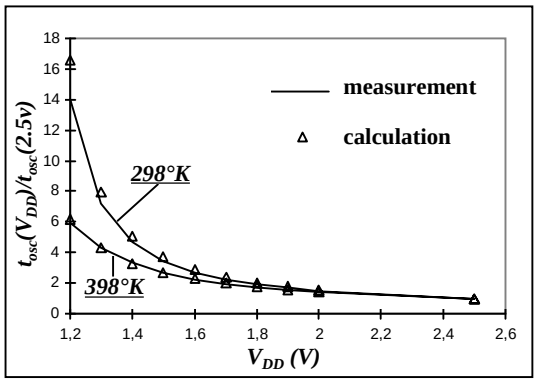

Figure 8: Comparison between the calculated and measured derating factors on oscinv2.

- Standard supply voltage domain for $V_{DD} > 3V_{T0}$ temperature effects are quite independent of the supply voltage value, in this case two well identified temperature and voltage derating factors can be used,

- Low voltage domain for $V_{DD} < 3V_{T0}$ where temperature effects are voltage dependent two zones can be considered:

- the intermediate range for $2V_{T0} < V_{DD} < 3V_{T0}$ where the temperature sensitivity decreases significantly with a reasonable performance degradation cost, this is an interesting operating domain for low temperature insensitive voltage applications,

- the lower range for $V_{DD} < 2V_{T0}$, where the sensitivity to V_{DD} becomes exponential and the sensitivity to the temperature is reversed. This defines a range of very low voltage applications where the delay performance must not be considered of fundamental importance.

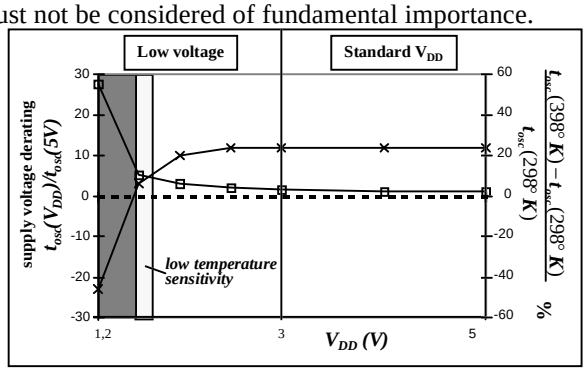

Figure 9: Illustration of the different voltage domains to be considered in defining derating factors.

6: Conclusion

We proposed here a detailed analysis of the temperature sensitivity of CMOS structures in the low voltage application range. We show that in the low voltage range temperature and V_{DD} effects can not be separated as it can be done in the standard voltage domain. A realistic model of the delay performance of CMOS structures based on an α-power current law calibrated for low voltage ($V_{DD} < 3V_{T0}$) is used to define derating factors allowing direct evaluation of the circuit delay evolution around the nominal operating point. This has been validated by comparing the calculated and measured oscillation period evolution of specific ring oscillators. We show clearly that for supply voltage values between 2 and $3V_{T0}$ the sensitivity of the delay to the temperature decreases strongly and cancels at the compensation point of the temperature effects on mobility and threshold voltage. For a 0.7μm process we verified that the voltage range 1.5-1.7v corresponds to the temperature insensitive operating zone, in good agreement with the value $2V_{T0}$ deduced from the model. The definition of this biasing domain is of great interest for temperature insensitive low power applications. This approach constitutes one of the first attempts to model temperature effects in low voltage applications showing up the insufficiency of the usual standard modeling.

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